Spartan-6 FPGA Packaging and Pinouts

Advance Product Specification

UG385 (v1.0) June 24, 2009

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/09	1.0	Initial Xilinx release.

Table of Contents

Chapter 4: Mechanical Drawings

Chapter 5: Thermal Specifications

Chapter 6: Package Marking

About This Guide

This guide describes Spartan®-6 device pinouts and package specifications; it also includes pinout diagrams and thermal data.

Organization of This Guide

This document is comprised of the following chapters:

- Chapter 1, "Packaging Overview"

  Provides an introduction to the Spartan-6 family with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- Chapter 2, "Pinout Tables"

  Provides pinout information for all Spartan-6 devices and packages.
- Chapter 3, "Pinout and SelectIO Bank Diagrams"

  Provides pinout diagrams for all Spartan-6 FPGA package/device combinations.
- Chapter 4, "Mechanical Drawings"

  Provides mechanical drawings of Spartan-6 FPGA packages.
- Chapter 5, "Thermal Specifications"

  Provides thermal data associated with Spartan-6 FPGA packages. Discusses Spartan-6 FPGA power management strategy and thermal management options.
- Chapter 6, "Package Marking"

  Provides example and description of the marking on top of the package (topmark).

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/6.

- Spartan-6 Family Overview

  This overview outlines the features and product selection of the Spartan-6 family.
- Spartan-6 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and switching characteristic specifications for the Spartan-6 family.
- Spartan-6 FPGA Configuration User Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

- Spartan-6 FPGA SelectIO Resources User Guide

  This guide describes the SelectIO™ resources available in all Spartan-6 devices.

- Spartan-6 FPGA Clocking Resources User Guide

  This guide describes the clocking resources available in all Spartan-6 devices, including the DCMs and PLLs.

- Spartan-6 FPGA Configurable Logic Block User Guide

  This guide describes the capabilities of the configurable logic blocks (CLBs) available in all Spartan-6 devices.

- Spartan-6 FPGA Block RAM Resources User Guide

  This guide describes the Spartan-6 device block RAM capabilities.

- Spartan-6 FPGA DSP48A1 Slice User Guide

  This guide describes the architecture of the DSP48A1 slice in Spartan-6 FPGAs and provides configuration examples.

- Spartan-6 FPGA Memory Controller User Guide

  This guide describes the Spartan-6 FPGA memory controller block, a dedicated embedded multi-port memory controller that greatly simplifies interfacing Spartan-6 FPGAs to the most popular memory standards.

- Spartan-6 FPGA GTP Transceiver User Guide

  This guide describes the GTP transceivers available in the Spartan-6 LXT FPGAs.

- Spartan-6 FPGA PCB Design Guide

  This guide provides information on PCB design for Spartan-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, visit the following Xilinx website:

http://www.xilinx.com/support

XILINX®

Chapter 1

Packaging Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions

Introduction

This section describes the pinouts for Spartan®-6 devices in various packages.

Spartan-6 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os. Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All of the Spartan-6 LX devices supported in a particular package are pinout compatible. All of the Spartan-6 LXT devices supported in a particular package are pinout compatible. The Spartan-6 LX devices are not pin compatible with the Spartan-6 LXT devices. Pins that are not available in some of the devices are listed in the "No Connects" column of each table.

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see *Spartan-6 FPGA SelectIO Resources User Guide*). Global pins and power/ground pins, are listed at the end of each table. Table 1-5 provides definitions for all pin types.

For information on package electrical characteristics and how the characteristics are measured, refer to UG112: *Device Package User Guide* found on the Xilinx website.

Designers targeting a part/package combination not currently supported in software should contact Xilinx technical support before starting board layout.

For the latest Spartan-6 FPGA pinout and package information, check the Xilinx website for updates to this document.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the package specifications and the maximum number of user I/Os possible in Spartan-6 FPGA packages.

Table 1-1: **Spartan-6 FPGA Packages**

Package Specifications	Packages								
	CPG196	TQG144[1]	CSG225	FT(G)256[2]	CSG324	FG(G)484[2]	CSG484	FG(G)676[2]	FG(G)900[2]
Package Type	Chip Scale	Quad Flat Pack	Chip Scale	BGA	Chip Scale	BGA	Chip Scale	BGA	BGA
Pitch (mm)	0.5	0.5	0.8	1.00	0.8	1.00	1.00	1.00	1.00
Size (mm)	8 x 8	22 x 22[1]	13 x 13	17 x 17	15 x 15	23 x 23	19 x 19	27 x 27	31 x 31
Maximum I/Os	100	102	160	186	232	338	330	498	570

Notes:

1. The footprint for the TQG144 package (22 x 22 mm) is larger than the package body (20 x 20 mm).
2. These devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

The number of I/Os per package includes all user I/Os *except* the dedicated pins listed in Table 1-2 and the GTP serial transceiver I/O channels for the devices listed in Table 1-3.

Table 1-2: **Spartan-6 FPGA Dedicated Configuration Pins**

SUSPEND	PROGRAM_B_2	TDI	TMS	VFS[1]	VBATT[1]
DONE_2	CMPCS_B_2	TDO	TCK	RFUSE[1]	

Notes:

1. Only available in XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T devices.

Table 1-3: **Number of Serial Transceivers (GTs) I/O Channels/Device**

I/O Channels	Device				
	LX25T	LX45T	LX75T[1]	LX100T[2]	LX150T[2]
MGTRXP	2	4	4 or 8	4 or 8	4 or 8
MGTRXN	2	4	4 or 8	4 or 8	4 or 8
MGTTXP	2	4	4 or 8	4 or 8	4 or 8
MGTTXN	2	4	4 or 8	4 or 8	4 or 8

Notes:

1. The XC6SLX75T has 4 GTP I/O channels in the FG(G)484 and CSG484 packages and 8 GTP I/O channels in the FG(G)676 package.
2. The XC6SLX100T and the XC6SLX150T have 4 GTP I/O channels in the FG(G)484 and CSG484 packages and 8 GTP I/O channels in the FG(G)676 and FG(G)900 packages.

Table 1-4 shows the number of available I/Os and the number of differential pairs for each Spartan-6 device/package combination.

Table 1-4: **Available I/O Pin/Device/Package Combinations**

Spartan-6 Device	User I/O Pins	Spartan-6 FPGA Package								
		CPG196	TQG144	CSG225	FT(G)256	CSG324	FG(G)484	CSG484	FG(G)676	FG(G)900
XC6SLX4	Available User I/Os	100	102	120	–	–	–	–	–	–
	Differential Pairs	50	51	60	–	–	–	–	–	–
XC6SLX9	Available User I/Os	100	102	160	186	200	–	–	–	–
	Differential Pairs	50	51	80	93	100	–	–	–	–
XC6SLX16	Available User I/Os	100	–	160	186	232	–	–	–	–
	Differential Pairs	50	–	80	93	116	–	–	–	–
XC6SLX25	Available User I/Os	–	–	–	186	226	266	–	–	–
	Differential Pairs	–	–	–	93	113	133	–	–	–
XC6SLX45	Available User I/Os	–	–	–	–	218	316	310	358	–
	Differential Pairs	–	–	–	–	109	158	155	179	–
XC6SLX75	Available User I/Os	–	–	–	–	–	TBD	310	400	–
	Differential Pairs	–	–	–	–	–	TBD	155	200	–
XC6SLX100	Available User I/Os	–	–	–	–	–	326	320	480	–
	Differential Pairs	–	–	–	–	–	163	160	240	–
XC6SLX150	Available User I/Os	–	–	–	–	–	338	330	498	570
	Differential Pairs	–	–	–	–	–	169	165	249	285
XC6SLX25T	Available User I/Os	–	–	–	–	190	250	–	–	–
	Differential Pairs	–	–	–	–	95	125	–	–	–
XC6SLX45T	Available User I/Os	–	–	–	–	190	296	290	–	–
	Differential Pairs	–	–	–	–	95	148	145	–	–
XC6SLX75T	Available User I/Os	–	–	–	–	–	TBD	290	320	–
	Differential Pairs	–	–	–	–	–	TBD	145	160	–
XC6SLX100T	Available User I/Os	–	–	–	–	–	296	290	376	490
	Differential Pairs	–	–	–	–	–	148	145	188	245
XC6SLX150T	Available User I/Os	–	–	–	–	–	296	290	396	530
	Differential Pairs	–	–	–	–	–	148	145	198	265

Pin Definitions

Table 1-5 lists the pin definitions used in Spartan-6 FPGA packages.

Table 1-5: **Spartan-6 FPGA Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/ Output	All user I/O pins are capable of differential signaling and can implement pairs. Each user I/O is labeled IO_LXXY_#, where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = [P | N] for the positive/negative sides of the differential pair. # indicates the bank number.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled IO_LXXY_ZZZ_#, where ZZZ represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Dn	Input	In SelectMAP mode, D0 through D15 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained.
D0_DIN_MISO_MISO1	Input	In Parallel (SelectMAP and BPI) modes, D0 is the LSB of the data bus. In Bit-serial modes, DIN is the single-data input. In SPI mode, MISO is the Master Input/Slave Output. In SPI x2 or x4 modes, MISO1 is the second bit of the SPI bus.
D1_MISO2, D2_MISO3	Input	In Parallel modes, D1 and D2 are lower-order bits of the data bus. In SPI x4 mode, MISO2 and MISO3 are two MSBs of the SPI bus.
An	Output	Address A0–A25 BPI address output. These pins become user I/O after configuration.
AWAKE	Output	Status output pin for the power-saving Suspend mode. SUSPEND is a dedicated pin and AWAKE is a multi-function pin. Unless Suspend mode is enabled in the application, AWAKE is available as user I/O.
MOSI_CSI_B_MISO0	Input/ Output	In SPI modes, Master Output/Slave Input (MOSI) connects from the FPGA to the SPI flash slave data input to send read commands and starting addresses. In SelectMAP mode, CSI_B is the active-low chip-select signal. In SPI x2 or x4 modes, MISO0 is the first bit of the SPI bus.
FCS_B	Output	BPI flash chip select.
FOE_B	Output	BPI flash output enable.
FWE_B	Output	BPI flash write enable.
LDC	Output	Low during configuration. BPI Flash byte selection.
HDC	Output	High during configuration. BPI Flash byte selection.
CSO_B	Output	In Parallel modes, parallel daisy-chain chip select. In SPI mode, SPI flash chip select.

Table 1-5: **Spartan-6 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
IRDY1/2, TRDY1/2	Output	Used with LogiCORE IP for PCI designs. An instantiation of the Xilinx core requires the use of either IRDY1 and TRDY1 or IRDY2 and TRDY2. See the core documentation for more details. These pins are available as user I/O when not being used for PCI designs.
DOUT_BUSY	Output	In SelectMAP mode, BUSY indicates the device status. In Bit-serial modes, DOUT gives configuration data to down-stream devices in a daisy chain.
RDWR_B_VREF	Input	In SelectMAP mode, this is the active-low write-enable signal. After configuration and if needed, RDWR_B can become a V_{REF} in bank 2.
HSWAPEN	Input	When Low, enables I/O pullups before and during configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. Can be used after configuration (optional) to indicate POST_CRC status.
SCPn	Input	System control pins SCP0-SCP7. Used for SUSPEND multi-pin wake-up feature.
CMP_MOSI, CMP_MISO, CMP_CLK	N/A	Reserved for future use. Use these pins as general-purpose I/O.
M0, M1	Input	Configuration mode selection. M0 = Parallel (Low) or Serial (High). M1 = Master (Low) or Slave (High).
CCLK	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
USERCCLK	Input	Optional user configuration clock input in Master modes.
GCLK	Input	These clock pins connect to global clock buffers. These pins become regular user I/Os when not needed for clocks.
VREF_#	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank). When used as a reference voltage within a bank, all V_{REF} pins within that bank must be connected.
Multi-Function Memory Controller Pins		
M#DQn	Input/ Output	Memory controller data D[0:15] in bank #.
M#LDQS	Input/ Output	Memory controller lower data strobe in bank #.
M#LDQSN	Input/ Output	Memory controller lower data strobe N in bank #.
M#UDQS	Input/ Output	Memory controller upper data strobe in bank #.

Table 1-5: **Spartan-6 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
M#UDQSN	Input/ Output	Memory controller upper data strobe N in bank #.
M#An	Output	Memory controller address A[0:14] in bank #.
M#BAn	Output	Memory controller bank address BA[0:2] in bank #.
M#LDM	Output	Memory controller lower data mask in bank #.
M#UDM	Output	Memory controller upper data mask in bank #.
M#CLK	Output	Memory controller clock in bank #.
M#CLKN	Output	Memory controller active-Low clock in bank #.
M#CASN	Output	Memory controller active-Low column address strobe in bank #.
M#RASN	Output	Memory controller active-Low row address strobe in bank #.
M#ODT	Output	Memory controller on-die termination control for external memory in bank #.
M#WE	Output	Memory controller write enable in bank #.
M#CKE	Output	Memory controller clock enable in bank #.
M#RESET	Output	Memory controller reset in bank #.
Dedicated Pins (1)		
DONE_2	Input/ Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
PROGRAM_B_2	Input	Active Low asynchronous reset to configuration logic. This pin has a default weak pull-up resistor.
SUSPEND	Input	Control input pin for the power-saving Suspend mode. SUSPEND is a dedicated pin and AWAKE is a multi-function pin. Must be enabled by configuration option.
TCK	Input	JTAG Boundary-scan clock.
TDI	Input	JTAG Boundary-scan data input.
TDO	Output	JTAG Boundary-scan data output.
TMS	Input	JTAG Boundary-scan mode select.
Reserved Pins		
NC	N/A	When found in a table or text file, an NC indicates that this pin is not connected in the specific device/package combination. However, in some devices in the same package, another pin name is used to describe this pin.
CMPCS_B	Input	Reserved. Must connect High.

Table 1-5: **Spartan-6 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
Other Pins		
GND	N/A	Ground.
VBATT	N/A	Decryptor key memory backup supply. When not used, tie this pin to V_{CC} or GND. Only available in the XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T devices.
VCCAUX	N/A	Power-supply pins for auxiliary circuits.
VCCINT	N/A	Power-supply pins for the internal core logic.
VCCO_#	N/A	Power-supply pins for the output drivers (per bank).
VFS	Input	Decryptor key EFUSE power supply pin for programming. Only available in the XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T devices.
RFUSE	Input	Decryptor key EFUSE resistor for programming. Only available in the XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T devices.
RocketIO Serial Transceiver Pins (GTPA1_DUAL Primitive)		
MGTAVCC	N/A	Power-supply pin for transceiver mixed-signal circuitry.
MGTAVTTTX, MGTAVTTRX	N/A	Power-supply pin for TX and RX circuitry.
MGTAVTTRCAL	N/A	Power-supply pin for the resistor calibration circuit.
MGTAVCCPLL0 MGTAVCCPLL1	N/A	Power-supply pin for PLL.
MGTREFCLK0/1P	Input	Positive differential reference clock.
MGTREFCLK0/1N	Input	Negative differential reference clock.
MGTRREF	Input	Precision reference resistor pin for internal calibration termination.
MGTRXP[0:1]	Input	Positive differential receive port.
MGTRXN[0:1]	Input	Negative differential receive port.
MGTTXP[0:1]	Output	Positive differential transmit port.
MGTTXN[0:1]	Output	Negative differential transmit port.

Notes:

1. Dedicated pins without a bank number (JTAG and SUSPEND) are powered by V_{CCAUX}.

XILINX®

Chapter 2

Pinout Tables

Summary

This chapter includes the pinout information tables for the following packages:

- Table 2-1, CPG196 Package—LX4, LX9, and LX16, on page 18
  Data is not currently available on devices in this package.
- Table 2-2, TQG144 Package—LX4 and LX9, on page 18
  Data on the LX4 is not currently available.
- Table 2-3, CSG225 Package—LX4, LX9, and LX16, on page 23
  Data on the LX4 is not currently available.
- Table 2-4, FT(G)256 Package—LX9, LX16, and LX25, on page 30
- Table 2-5, CSG324 Package—LX9, LX16, LX25, and LX45, on page 38
- Table 2-6, CSG324 Package—LX25T and LX45T, on page 48
- Table 2-7, FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150, on page 58
  Data on the LX75 is not currently available.
- Table 2-8, FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T, on page 73
  Data on the LX75T is not currently available.
- Table 2-9, CSG484 Package—LX45, LX75, LX100, and LX150, on page 88
  Data is not currently available on devices in this package.
- Table 2-10, CSG484 Package—LX45T, LX75T, LX100T, and LX150T, on page 88
  Data is not currently available on devices in this package.
- Table 2-11, FG(G)676 Package—LX45, on page 88
- Table 2-12, FG(G)676 Package—LX75, LX100, and LX150, on page 109
  Data on the LX75 is not currently available.
- Table 2-13, FG(G)676 Package—LX75T, LX100T, and LX150T, on page 130
  Data on the LX75T is not currently available.
- Table 2-14, FG(G)900 Package—LX150, on page 151
  Data is not currently available on devices in this package.
- Table 2-15, FG(G)900 Package—LX100T and LX150T, on page 151
  Data is not currently available on devices in this package.

CPG196 Package—LX4, LX9, and LX16

Table 2-1: **CPG196 Package—LX4, LX9, and LX16**

Bank	Pin Description	Pin Number	No Connect (NC)
Data is not currently available on devices in this package.			

TQG144 Package—LX4 and LX9

Data on the LX4 is not currently available.

Table 2-2: **TQG144 Package—LX4 and LX9**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	P144	
0	IO_L1N_VREF_0	P143	
0	IO_L2P_0	P142	
0	IO_L2N_0	P141	
0	IO_L3P_0	P140	
0	IO_L3N_0	P139	
0	IO_L4P_0	P138	
0	IO_L4N_0	P137	
0	IO_L34P_GCLK19_0	P134	
0	IO_L34N_GCLK18_0	P133	
0	IO_L35P_GCLK17_0	P132	
0	IO_L35N_GCLK16_0	P131	
0	IO_L36P_GCLK15_0	P127	
0	IO_L36N_GCLK14_0	P126	
0	IO_L37P_GCLK13_0	P124	
0	IO_L37N_GCLK12_0	P123	
0	IO_L62P_0	P121	
0	IO_L62N_VREF_0	P120	
0	IO_L63P_SCP7_0	P119	
0	IO_L63N_SCP6_0	P118	
0	IO_L64P_SCP5_0	P117	
0	IO_L64N_SCP4_0	P116	
0	IO_L65P_SCP3_0	P115	
0	IO_L65N_SCP2_0	P114	
0	IO_L66P_SCP1_0	P112	

Table 2-2: **TQG144 Package—LX4 and LX9 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L66N_SCP0_0	P111	
NA	TCK	P109	
NA	TDI	P110	
NA	TMS	P107	
NA	TDO	P106	
1	IO_L1P_1	P105	
1	IO_L1N_VREF_1	P104	
1	IO_L32P_1	P102	
1	IO_L32N_1	P101	
1	IO_L33P_1	P100	
1	IO_L33N_1	P99	
1	IO_L34P_1	P98	
1	IO_L34N_1	P97	
1	IO_L40P_GCLK11_1	P95	
1	IO_L40N_GCLK10_1	P94	
1	IO_L41P_GCLK9_IRDY1_1	P93	
1	IO_L41N_GCLK8_1	P92	
1	IO_L42P_GCLK7_1	P88	
1	IO_L42N_GCLK6_TRDY1_1	P87	
1	IO_L43P_GCLK5_1	P85	
1	IO_L43N_GCLK4_1	P84	
1	IO_L45P_1	P83	
1	IO_L45N_1	P82	
1	IO_L46P_1	P81	
1	IO_L46N_1	P80	
1	IO_L47P_1	P79	
1	IO_L47N_1	P78	
1	IO_L74P_AWAKE_1	P75	
1	IO_L74N_DOUT_BUSY_1	P74	
NA	SUSPEND	P73	
2	CMPCS_B_2	P72	
2	DONE_2	P71	
2	IO_L1P_CCLK_2	P70	

Table 2-2: **TQG144 Package—LX4 and LX9 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L1N_M0_CMPMISO_2	P69	
2	IO_L2P_CMPCLK_2	P67	
2	IO_L2N_CMPMOSI_2	P66	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P65	
2	IO_L3N_MOSI_CSI_B_MISO0_2	P64	
2	IO_L12P_D1_MISO2_2	P62	
2	IO_L12N_D2_MISO3_2	P61	
2	IO_L13P_M1_2	P60	
2	IO_L13N_D10_2	P59	
2	IO_L14P_D11_2	P58	
2	IO_L14N_D12_2	P57	
2	IO_L30P_GCLK1_D13_2	P56	
2	IO_L30N_GCLK0_USERCCLK_2	P55	
2	IO_L31P_GCLK31_D14_2	P51	
2	IO_L31N_GCLK30_D15_2	P50	
2	IO_L48P_D7_2	P48	
2	IO_L48N_RDWR_B_VREF_2	P47	
2	IO_L49P_D3_2	P46	
2	IO_L49N_D4_2	P45	
2	IO_L62P_D5_2	P44	
2	IO_L62N_D6_2	P43	
2	IO_L64P_D8_2	P41	
2	IO_L64N_D9_2	P40	
2	IO_L65P_INIT_B_2	P39	
2	IO_L65N_CSO_B_2	P38	
2	PROGRAM_B_2	P37	
3	IO_L1P_3	P35	
3	IO_L1N_VREF_3	P34	
3	IO_L2P_3	P33	
3	IO_L2N_3	P32	
3	IO_L36P_3	P30	
3	IO_L36N_3	P29	
3	IO_L37P_3	P27	

Table 2-2: **TQG144 Package—LX4 and LX9 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L37N_3	P26	
3	IO_L41P_GCLK27_3	P24	
3	IO_L41N_GCLK26_3	P23	
3	IO_L42P_GCLK25_TRDY2_3	P22	
3	IO_L42N_GCLK24_3	P21	
3	IO_L43P_GCLK23_3	P17	
3	IO_L43N_GCLK22_IRDY2_3	P16	
3	IO_L44P_GCLK21_3	P15	
3	IO_L44N_GCLK20_3	P14	
3	IO_L49P_3	P12	
3	IO_L49N_3	P11	
3	IO_L50P_3	P10	
3	IO_L50N_3	P9	
3	IO_L51P_3	P8	
3	IO_L51N_3	P7	
3	IO_L52P_3	P6	
3	IO_L52N_3	P5	
3	IO_L83P_3	P2	
3	IO_L83N_VREF_3	P1	
NA	GND	P108	
NA	GND	P113	
NA	GND	P13	
NA	GND	P130	
NA	GND	P136	
NA	GND	P25	
NA	GND	P3	
NA	GND	P49	
NA	GND	P54	
NA	GND	P68	
NA	GND	P77	
NA	GND	P91	
NA	GND	P96	
NA	VCCAUX	P129	

Table 2-2: **TQG144 Package—LX4 and LX9 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	P20	
NA	VCCAUX	P36	
NA	VCCAUX	P53	
NA	VCCAUX	P90	
NA	VCCINT	P128	
NA	VCCINT	P19	
NA	VCCINT	P28	
NA	VCCINT	P52	
NA	VCCINT	P89	
0	VCCO_0	P122	
0	VCCO_0	P125	
0	VCCO_0	P135	
1	VCCO_1	P103	
1	VCCO_1	P76	
1	VCCO_1	P86	
2	VCCO_2	P42	
2	VCCO_2	P63	
3	VCCO_3	P18	
3	VCCO_3	P31	
3	VCCO_3	P4	

CSG225 Package—LX4, LX9, and LX16

Data on the LX4 is not currently available.

Table 2-3: **CSG225 Package—LX4, LX9, and LX16**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	
0	IO_L1N_VREF_0	A2	
0	IO_L2P_0	B3	
0	IO_L2N_0	A3	
0	IO_L3P_0	D5	
0	IO_L3N_0	C5	
0	IO_L4P_0	C4	
0	IO_L4N_0	A4	
0	IO_L5P_0	E6	
0	IO_L5N_0	D6	
0	IO_L6P_0	B5	
0	IO_L6N_0	A5	
0	IO_L7P_0	D7	
0	IO_L7N_0	C7	
0	IO_L33P_0	C6	
0	IO_L33N_0	A6	
0	IO_L34P_GCLK19_0	E7	
0	IO_L34N_GCLK18_0	D8	
0	IO_L35P_GCLK17_0	B7	
0	IO_L35N_GCLK16_0	A7	
0	IO_L36P_GCLK15_0	C8	
0	IO_L36N_GCLK14_0	A8	
0	IO_L37P_GCLK13_0	B9	
0	IO_L37N_GCLK12_0	A9	
0	IO_L38P_0	F8	
0	IO_L38N_VREF_0	E8	
0	IO_L39P_0	D10	
0	IO_L39N_0	C9	
0	IO_L40P_0	F10	
0	IO_L40N_0	E9	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L62P_0	C10	
0	IO_L62N_VREF_0	A10	
0	IO_L63P_SCP7_0	B11	
0	IO_L63N_SCP6_0	A11	
0	IO_L64P_SCP5_0	D11	
0	IO_L64N_SCP4_0	C11	
0	IO_L65P_SCP3_0	B13	
0	IO_L65N_SCP2_0	A13	
0	IO_L66P_SCP1_0	C12	
0	IO_L66N_SCP0_0	A12	
NA	TCK	A14	
NA	TDI	E10	
NA	TMS	E13	
NA	TDO	D12	
1	IO_L1P_A25_1	B14	
1	IO_L1N_A24_VREF_1	B15	
1	IO_L30P_A21_M1RESET_1	G11	
1	IO_L30N_A20_M1A11_1	G12	
1	IO_L31P_A19_M1CKE_1	F11	
1	IO_L31N_A18_M1A12_1	F12	
1	IO_L32P_A17_M1A8_1	H10	
1	IO_L32N_A16_M1A9_1	H11	
1	IO_L33P_A15_M1A10_1	C14	
1	IO_L33N_A14_M1A4_1	C15	
1	IO_L34P_A13_M1WE_1	H12	
1	IO_L34N_A12_M1BA2_1	G13	
1	IO_L35P_A11_M1A7_1	D13	
1	IO_L35N_A10_M1A2_1	D15	
1	IO_L36P_A9_M1BA0_1	J11	
1	IO_L36N_A8_M1BA1_1	J13	
1	IO_L37P_A7_M1A0_1	E14	
1	IO_L37N_A6_M1A1_1	E15	
1	IO_L38P_A5_M1CLK_1	K10	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L38N_A4_M1CLKN_1	K11	
1	IO_L39P_M1A3_1	F13	
1	IO_L39N_M1ODT_1	F15	
1	IO_L40P_GCLK11_M1A5_1	K12	
1	IO_L40N_GCLK10_M1A6_1	L12	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	G14	
1	IO_L41N_GCLK8_M1CASN_1	G15	
1	IO_L42P_GCLK7_M1UDM_1	H13	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	H15	
1	IO_L43P_GCLK5_M1DQ4_1	J14	
1	IO_L43N_GCLK4_M1DQ5_1	J15	
1	IO_L44P_A3_M1DQ6_1	K13	
1	IO_L44N_A2_M1DQ7_1	K15	
1	IO_L45P_A1_M1LDQS_1	L14	
1	IO_L45N_A0_M1LDQSN_1	L15	
1	IO_L46P_FCS_B_M1DQ2_1	M13	
1	IO_L46N_FOE_B_M1DQ3_1	M15	
1	IO_L47P_FWE_B_M1DQ0_1	N14	
1	IO_L47N_LDC_M1DQ1_1	N15	
1	IO_L74P_AWAKE_1	P14	
1	IO_L74N_DOUT_BUSY_1	P15	
NA	SUSPEND	L13	
2	CMPCS_B_2	L10	
2	DONE_2	R14	
2	IO_L1P_CCLK_2	N12	
2	IO_L1N_M0_CMPMISO_2	R12	
2	IO_L2P_CMPCLK_2	P13	
2	IO_L2N_CMPMOSI_2	R13	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P11	
2	IO_L3N_MOSI_CSI_B_MISO0_2	R11	
2	IO_L12P_D1_MISO2_2	M11	
2	IO_L12N_D2_MISO3_2	N11	
2	IO_L13P_M1_2	N10	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L13N_D10_2	R10	
2	IO_L14P_D11_2	L9	
2	IO_L14N_D12_2	M10	
2	IO_L15P_2	M9	
2	IO_L15N_2	N9	
2	IO_L16P_2	P9	
2	IO_L16N_VREF_2	R9	
2	IO_L29P_GCLK3_2	N8	
2	IO_L29N_GCLK2_2	R8	
2	IO_L30P_GCLK1_D13_2	M8	
2	IO_L30N_GCLK0_USERCCLK_2	N7	
2	IO_L31P_GCLK31_D14_2	K8	
2	IO_L31N_GCLK30_D15_2	L8	
2	IO_L32P_GCLK29_2	P7	
2	IO_L32N_GCLK28_2	R7	
2	IO_L47P_2	L7	
2	IO_L47N_2	M6	
2	IO_L48P_D7_2	N6	
2	IO_L48N_RDWR_B_VREF_2	R6	
2	IO_L49P_D3_2	P5	
2	IO_L49N_D4_2	R5	
2	IO_L62P_D5_2	L6	
2	IO_L62N_D6_2	L5	
2	IO_L63P_2	N4	
2	IO_L63N_2	R4	
2	IO_L64P_D8_2	M5	
2	IO_L64N_D9_2	N5	
2	IO_L65P_INIT_B_2	P3	
2	IO_L65N_CSO_B_2	R3	
2	PROGRAM_B_2	R2	
3	IO_L1P_3	M4	
3	IO_L1N_VREF_3	L3	
3	IO_L2P_3	P2	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L2N_3	P1	
3	IO_L37P_M3DQ0_3	N2	
3	IO_L37N_M3DQ1_3	N1	
3	IO_L38P_M3DQ2_3	M3	
3	IO_L38N_M3DQ3_3	M1	
3	IO_L39P_M3LDQS_3	L2	
3	IO_L39N_M3LDQSN_3	L1	
3	IO_L40P_M3DQ6_3	K3	
3	IO_L40N_M3DQ7_3	K1	
3	IO_L41P_GCLK27_M3DQ4_3	J2	
3	IO_L41N_GCLK26_M3DQ5_3	J1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	H3	
3	IO_L42N_GCLK24_M3LDM_3	H1	
3	IO_L43P_GCLK23_M3RASN_3	K4	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	J3	
3	IO_L44P_GCLK21_M3A5_3	G2	
3	IO_L44N_GCLK20_M3A6_3	G1	
3	IO_L45P_M3A3_3	K5	
3	IO_L45N_M3ODT_3	J4	
3	IO_L46P_M3CLK_3	F3	
3	IO_L46N_M3CLKN_3	F1	
3	IO_L47P_M3A0_3	J5	
3	IO_L47N_M3A1_3	H4	
3	IO_L48P_M3BA0_3	G5	
3	IO_L48N_M3BA1_3	G3	
3	IO_L49P_M3A7_3	H6	
3	IO_L49N_M3A2_3	H5	
3	IO_L50P_M3WE_3	F5	
3	IO_L50N_M3BA2_3	F4	
3	IO_L51P_M3A10_3	E5	
3	IO_L51N_M3A4_3	E4	
3	IO_L52P_M3A8_3	E2	
3	IO_L52N_M3A9_3	E1	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L53P_M3CKE_3	D4	
3	IO_L53N_M3A12_3	E3	
3	IO_L54P_M3RESET_3	D3	
3	IO_L54N_M3A11_3	D1	
3	IO_L83P_3	C2	
3	IO_L83N_VREF_3	C1	
NA	GND	A1	
NA	GND	A15	
NA	GND	B10	
NA	GND	B6	
NA	GND	C13	
NA	GND	C3	
NA	GND	E11	
NA	GND	F14	
NA	GND	F2	
NA	GND	F6	
NA	GND	G7	
NA	GND	G9	
NA	GND	H8	
NA	GND	J7	
NA	GND	J9	
NA	GND	K14	
NA	GND	K2	
NA	GND	K6	
NA	GND	L11	
NA	GND	N13	
NA	GND	N3	
NA	GND	P10	
NA	GND	P6	
NA	GND	R1	
NA	GND	R15	
NA	VCCAUX	B1	
NA	VCCAUX	E12	

Table 2-3: **CSG225 Package—LX4, LX9, and LX16 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	F7	
NA	VCCAUX	G10	
NA	VCCAUX	J6	
NA	VCCAUX	K9	
NA	VCCAUX	L4	
NA	VCCAUX	M12	
NA	VCCINT	F9	
NA	VCCINT	G6	
NA	VCCINT	G8	
NA	VCCINT	H7	
NA	VCCINT	H9	
NA	VCCINT	J10	
NA	VCCINT	J8	
NA	VCCINT	K7	
0	VCCO_0	B12	
0	VCCO_0	B4	
0	VCCO_0	B8	
0	VCCO_0	D9	
1	VCCO_1	D14	
1	VCCO_1	H14	
1	VCCO_1	J12	
1	VCCO_1	M14	
2	VCCO_2	M7	
2	VCCO_2	P12	
2	VCCO_2	P4	
2	VCCO_2	P8	
3	VCCO_3	D2	
3	VCCO_3	G4	
3	VCCO_3	H2	
3	VCCO_3	M2	

FT(G)256 Package—LX9, LX16, and LX25

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	C4	
0	IO_L1N_VREF_0	A4	
0	IO_L2P_0	B5	
0	IO_L2N_0	A5	
0	IO_L3P_0	D5	
0	IO_L3N_0	C5	
0	IO_L4P_0	B6	
0	IO_L4N_0	A6	
0	IO_L5P_0	F7	
0	IO_L5N_0	E6	
0	IO_L6P_0	C7	
0	IO_L6N_0	A7	
0	IO_L7P_0	D6	
0	IO_L7N_0	C6	
0	IO_L33P_0	B8	
0	IO_L33N_0	A8	
0	IO_L34P_GCLK19_0	C9	
0	IO_L34N_GCLK18_0	A9	
0	IO_L35P_GCLK17_0	B10	
0	IO_L35N_GCLK16_0	A10	
0	IO_L36P_GCLK15_0	E7	
0	IO_L36N_GCLK14_0	E8	
0	IO_L37P_GCLK13_0	E10	
0	IO_L37N_GCLK12_0	C10	
0	IO_L38P_0	D8	
0	IO_L38N_VREF_0	C8	
0	IO_L39P_0	C11	
0	IO_L39N_0	A11	
0	IO_L40P_0	F9	
0	IO_L40N_0	D9	
0	IO_L62P_0	B12	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L62N_VREF_0	A12	
0	IO_L63P_SCP7_0	C13	
0	IO_L63N_SCP6_0	A13	
0	IO_L64P_SCP5_0	F10	
0	IO_L64N_SCP4_0	E11	
0	IO_L65P_SCP3_0	B14	
0	IO_L65N_SCP2_0	A14	
0	IO_L66P_SCP1_0	D11	
0	IO_L66N_SCP0_0	D12	
NA	TCK	C14	
NA	TDI	C12	
NA	TMS	A15	
NA	TDO	E14	
1	IO_L1P_A25_1	E13	
1	IO_L1N_A24_VREF_1	E12	
1	IO_L29P_A23_M1A13_1	B15	
1	IO_L29N_A22_M1A14_1	B16	
1	IO_L30P_A21_M1RESET_1	F12	
1	IO_L30N_A20_M1A11_1	G11	
1	IO_L31P_A19_M1CKE_1	D14	
1	IO_L31N_A18_M1A12_1	D16	
1	IO_L32P_A17_M1A8_1	F13	
1	IO_L32N_A16_M1A9_1	F14	
1	IO_L33P_A15_M1A10_1	C15	
1	IO_L33N_A14_M1A4_1	C16	
1	IO_L34P_A13_M1WE_1	E15	
1	IO_L34N_A12_M1BA2_1	E16	
1	IO_L35P_A11_M1A7_1	F15	
1	IO_L35N_A10_M1A2_1	F16	
1	IO_L36P_A9_M1BA0_1	G14	
1	IO_L36N_A8_M1BA1_1	G16	
1	IO_L37P_A7_M1A0_1	H15	
1	IO_L37N_A6_M1A1_1	H16	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L38P_A5_M1CLK_1	G12	
1	IO_L38N_A4_M1CLKN_1	H11	
1	IO_L39P_M1A3_1	H13	
1	IO_L39N_M1ODT_1	H14	
1	IO_L40P_GCLK11_M1A5_1	J11	
1	IO_L40N_GCLK10_M1A6_1	J12	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	J13	
1	IO_L41N_GCLK8_M1CASN_1	K14	
1	IO_L42P_GCLK7_M1UDM_1	K12	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	K11	
1	IO_L43P_GCLK5_M1DQ4_1	J14	
1	IO_L43N_GCLK4_M1DQ5_1	J16	
1	IO_L44P_A3_M1DQ6_1	K15	
1	IO_L44N_A2_M1DQ7_1	K16	
1	IO_L45P_A1_M1LDQS_1	N14	
1	IO_L45N_A0_M1LDQSN_1	N16	
1	IO_L46P_FCS_B_M1DQ2_1	M15	
1	IO_L46N_FOE_B_M1DQ3_1	M16	
1	IO_L47P_FWE_B_M1DQ0_1	L14	
1	IO_L47N_LDC_M1DQ1_1	L16	
1	IO_L48P_HDC_M1DQ8_1	P15	
1	IO_L48N_M1DQ9_1	P16	
1	IO_L49P_M1DQ10_1	R15	
1	IO_L49N_M1DQ11_1	R16	
1	IO_L50P_M1UDQS_1	R14	
1	IO_L50N_M1UDQSN_1	T15	
1	IO_L51P_M1DQ12_1	T14	
1	IO_L51N_M1DQ13_1	T13	
1	IO_L52P_M1DQ14_1	R12	
1	IO_L52N_M1DQ15_1	T12	
1	IO_L53P_1	L12	
1	IO_L53N_VREF_1	L13	
1	IO_L74P_AWAKE_1	M13	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L74N_DOUT_BUSY_1	M14	
NA	SUSPEND	P14	
2	CMPCS_B_2	L11	
2	DONE_2	P13	
2	IO_L1P_CCLK_2	R11	
2	IO_L1N_M0_CMPMISO_2	T11	
2	IO_L2P_CMPCLK_2	M12	
2	IO_L2N_CMPMOSI_2	M11	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P10	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T10	
2	IO_L12P_D1_MISO2_2	N12	
2	IO_L12N_D2_MISO3_2	P12	
2	IO_L13P_M1_2	N11	
2	IO_L13N_D10_2	P11	
2	IO_L14P_D11_2	N9	
2	IO_L14N_D12_2	P9	
2	IO_L16P_2	L10	
2	IO_L16N_VREF_2	M10	
2	IO_L23P_2	R9	
2	IO_L23N_2	T9	
2	IO_L29P_GCLK3_2	M9	
2	IO_L29N_GCLK2_2	N8	
2	IO_L30P_GCLK1_D13_2	P8	
2	IO_L30N_GCLK0_USERCCLK_2	T8	
2	IO_L31P_GCLK31_D14_2	P7	
2	IO_L31N_GCLK30_D15_2	M7	
2	IO_L32P_GCLK29_2	R7	
2	IO_L32N_GCLK28_2	T7	
2	IO_L47P_2	P6	
2	IO_L47N_2	T6	
2	IO_L48P_D7_2	R5	
2	IO_L48N_RDWR_B_VREF_2	T5	
2	IO_L49P_D3_2	N5	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L49N_D4_2	P5	
2	IO_L62P_D5_2	L8	
2	IO_L62N_D6_2	L7	
2	IO_L63P_2	P4	
2	IO_L63N_2	T4	
2	IO_L64P_D8_2	M6	
2	IO_L64N_D9_2	N6	
2	IO_L65P_INIT_B_2	R3	
2	IO_L65N_CSO_B_2	T3	
2	PROGRAM_B_2	T2	
3	IO_L1P_3	M4	
3	IO_L1N_VREF_3	M3	
3	IO_L2P_3	M5	
3	IO_L2N_3	N4	
3	IO_L32P_M3DQ14_3	R2	
3	IO_L32N_M3DQ15_3	R1	
3	IO_L33P_M3DQ12_3	P2	
3	IO_L33N_M3DQ13_3	P1	
3	IO_L34P_M3UDQS_3	N3	
3	IO_L34N_M3UDQSN_3	N1	
3	IO_L35P_M3DQ10_3	M2	
3	IO_L35N_M3DQ11_3	M1	
3	IO_L36P_M3DQ8_3	L3	
3	IO_L36N_M3DQ9_3	L1	
3	IO_L37P_M3DQ0_3	K2	
3	IO_L37N_M3DQ1_3	K1	
3	IO_L38P_M3DQ2_3	J3	
3	IO_L38N_M3DQ3_3	J1	
3	IO_L39P_M3LDQS_3	H2	
3	IO_L39N_M3LDQSN_3	H1	
3	IO_L40P_M3DQ6_3	G3	
3	IO_L40N_M3DQ7_3	G1	
3	IO_L41P_GCLK27_M3DQ4_3	F2	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L41N_GCLK26_M3DQ5_3	F1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K3	
3	IO_L42N_GCLK24_M3LDM_3	J4	
3	IO_L43P_GCLK23_M3RASN_3	J6	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	H5	
3	IO_L44P_GCLK21_M3A5_3	H4	
3	IO_L44N_GCLK20_M3A6_3	H3	
3	IO_L45P_M3A3_3	L4	
3	IO_L45N_M3ODT_3	L5	
3	IO_L46P_M3CLK_3	E2	
3	IO_L46N_M3CLKN_3	E1	
3	IO_L47P_M3A0_3	K5	
3	IO_L47N_M3A1_3	K6	
3	IO_L48P_M3BA0_3	C3	
3	IO_L48N_M3BA1_3	C2	
3	IO_L49P_M3A7_3	D3	
3	IO_L49N_M3A2_3	D1	
3	IO_L50P_M3WE_3	C1	
3	IO_L50N_M3BA2_3	B1	
3	IO_L51P_M3A10_3	G6	
3	IO_L51N_M3A4_3	G5	
3	IO_L52P_M3A8_3	B2	
3	IO_L52N_M3A9_3	A2	
3	IO_L53P_M3CKE_3	F4	
3	IO_L53N_M3A12_3	F3	
3	IO_L54P_M3RESET_3	E4	
3	IO_L54N_M3A11_3	E3	
3	IO_L55P_M3A13_3	F6	
3	IO_L55N_M3A14_3	F5	
3	IO_L83P_3	B3	
3	IO_L83N_VREF_3	A3	
NA	GND	A1	
NA	GND	A16	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B11	
NA	GND	B7	
NA	GND	D13	
NA	GND	D4	
NA	GND	E9	
NA	GND	G15	
NA	GND	G2	
NA	GND	G8	
NA	GND	H12	
NA	GND	H7	
NA	GND	H9	
NA	GND	J5	
NA	GND	J8	
NA	GND	K7	
NA	GND	K9	
NA	GND	L15	
NA	GND	L2	
NA	GND	M8	
NA	GND	N13	
NA	GND	P3	
NA	GND	R10	
NA	GND	R6	
NA	GND	T1	
NA	GND	T16	
NA	VCCAUX	E5	
NA	VCCAUX	F11	
NA	VCCAUX	F8	
NA	VCCAUX	G10	
NA	VCCAUX	H6	
NA	VCCAUX	J10	
NA	VCCAUX	L6	
NA	VCCAUX	L9	
NA	VCCINT	G7	

Table 2-4: **FT(G)256 Package—LX9, LX16, and LX25 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	G9	
NA	VCCINT	H10	
NA	VCCINT	H8	
NA	VCCINT	J7	
NA	VCCINT	J9	
NA	VCCINT	K10	
NA	VCCINT	K8	
0	VCCO_0	B13	
0	VCCO_0	B4	
0	VCCO_0	B9	
0	VCCO_0	D10	
0	VCCO_0	D7	
1	VCCO_1	D15	
1	VCCO_1	G13	
1	VCCO_1	J15	
1	VCCO_1	K13	
1	VCCO_1	N15	
1	VCCO_1	R13	
2	VCCO_2	N10	
2	VCCO_2	N7	
2	VCCO_2	R4	
2	VCCO_2	R8	
3	VCCO_3	D2	
3	VCCO_3	G4	
3	VCCO_3	J2	
3	VCCO_3	K4	
3	VCCO_3	N2	

CSG324 Package—LX9, LX16, LX25, and LX45

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	D4	
0	IO_L1N_VREF_0	C4	
0	IO_L2P_0	B2	
0	IO_L2N_0	A2	
0	IO_L3P_0	D6	
0	IO_L3N_0	C6	
0	IO_L4P_0	B3	
0	IO_L4N_0	A3	
0	IO_L5P_0	B4	
0	IO_L5N_0	A4	
0	IO_L6P_0	C5	
0	IO_L6N_0	A5	
0	IO_L7P_0	F7	LX9, LX25, LX45
0	IO_L7N_0	E6	LX9, LX25, LX45
0	IO_L8P_0	B6	
0	IO_L8N_VREF_0	A6	
0	IO_L9P_0	E7	LX9, LX25, LX45
0	IO_L9N_0	E8	LX9, LX25, LX45
0	IO_L10P_0	C7	
0	IO_L10N_0	A7	
0	IO_L11P_0	D8	
0	IO_L11N_0	C8	
0	IO_L32P_0	G8	LX9, LX25, LX45
0	IO_L32N_0	F8	LX9, LX25, LX45
0	IO_L33P_0	B8	
0	IO_L33N_0	A8	
0	IO_L34P_GCLK19_0	D9	
0	IO_L34N_GCLK18_0	C9	
0	IO_L35P_GCLK17_0	B9	
0	IO_L35N_GCLK16_0	A9	
0	IO_L36P_GCLK15_0	D11	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L36N_GCLK14_0	C11	
0	IO_L37P_GCLK13_0	C10	
0	IO_L37N_GCLK12_0	A10	
0	IO_L38P_0	G9	
0	IO_L38N_VREF_0	F9	
0	IO_L39P_0	B11	
0	IO_L39N_0	A11	
0	IO_L40P_0	G11	LX9, LX45
0	IO_L40N_0	F10	LX9, LX45
0	IO_L41P_0	B12	
0	IO_L41N_0	A12	
0	IO_L42P_0	F11	LX9, LX45
0	IO_L42N_0	E11	LX9, LX45
0	IO_L47P_0	D12	LX9, LX45
0	IO_L47N_0	C12	LX9, LX45
0	IO_L50P_0	C13	LX9
0	IO_L50N_0	A13	LX9
0	IO_L51P_0	F12	LX9, LX45
0	IO_L51N_0	E12	LX9, LX45
0	IO_L62P_0	B14	
0	IO_L62N_VREF_0	A14	
0	IO_L63P_SCP7_0	F13	
0	IO_L63N_SCP6_0	E13	
0	IO_L64P_SCP5_0	C15	
0	IO_L64N_SCP4_0	A15	
0	IO_L65P_SCP3_0	D14	
0	IO_L65N_SCP2_0	C14	
0	IO_L66P_SCP1_0	B16	
0	IO_L66N_SCP0_0	A16	
NA	TCK	A17	
NA	TDI	D15	
NA	TMS	B18	
NA	TDO	D16	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L1P_A25_1	F15	
1	IO_L1N_A24_VREF_1	F16	
1	IO_L29P_A23_M1A13_1	C17	
1	IO_L29N_A22_M1A14_1	C18	
1	IO_L30P_A21_M1RESET_1	F14	
1	IO_L30N_A20_M1A11_1	G14	
1	IO_L31P_A19_M1CKE_1	D17	
1	IO_L31N_A18_M1A12_1	D18	
1	IO_L32P_A17_M1A8_1	H12	
1	IO_L32N_A16_M1A9_1	G13	
1	IO_L33P_A15_M1A10_1	E16	
1	IO_L33N_A14_M1A4_1	E18	
1	IO_L34P_A13_M1WE_1	K12	
1	IO_L34N_A12_M1BA2_1	K13	
1	IO_L35P_A11_M1A7_1	F17	
1	IO_L35N_A10_M1A2_1	F18	
1	IO_L36P_A9_M1BA0_1	H13	
1	IO_L36N_A8_M1BA1_1	H14	
1	IO_L37P_A7_M1A0_1	H15	
1	IO_L37N_A6_M1A1_1	H16	
1	IO_L38P_A5_M1CLK_1	G16	
1	IO_L38N_A4_M1CLKN_1	G18	
1	IO_L39P_M1A3_1	J13	
1	IO_L39N_M1ODT_1	K14	
1	IO_L40P_GCLK11_M1A5_1	L12	
1	IO_L40N_GCLK10_M1A6_1	L13	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K15	
1	IO_L41N_GCLK8_M1CASN_1	K16	
1	IO_L42P_GCLK7_M1UDM_1	L15	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L16	
1	IO_L43P_GCLK5_M1DQ4_1	H17	
1	IO_L43N_GCLK4_M1DQ5_1	H18	
1	IO_L44P_A3_M1DQ6_1	J16	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L44N_A2_M1DQ7_1	J18	
1	IO_L45P_A1_M1LDQS_1	K17	
1	IO_L45N_A0_M1LDQSN_1	K18	
1	IO_L46P_FCS_B_M1DQ2_1	L17	
1	IO_L46N_FOE_B_M1DQ3_1	L18	
1	IO_L47P_FWE_B_M1DQ0_1	M16	
1	IO_L47N_LDC_M1DQ1_1	M18	
1	IO_L48P_HDC_M1DQ8_1	N17	
1	IO_L48N_M1DQ9_1	N18	
1	IO_L49P_M1DQ10_1	P17	
1	IO_L49N_M1DQ11_1	P18	
1	IO_L50P_M1UDQS_1	N15	
1	IO_L50N_M1UDQSN_1	N16	
1	IO_L51P_M1DQ12_1	T17	
1	IO_L51N_M1DQ13_1	T18	
1	IO_L52P_M1DQ14_1	U17	
1	IO_L52N_M1DQ15_1	U18	
1	IO_L53P_1	M14	
1	IO_L53N_VREF_1	N14	
1	IO_L61P_1	L14	
1	IO_L61N_1	M13	
1	IO_L74P_AWAKE_1	P15	
1	IO_L74N_DOUT_BUSY_1	P16	
NA	SUSPEND	R16	
2	CMPCS_B_2	P13	
2	DONE_2	V17	
2	IO_L1P_CCLK_2	R15	
2	IO_L1N_M0_CMPMISO_2	T15	
2	IO_L2P_CMPCLK_2	U16	
2	IO_L2N_CMPMOSI_2	V16	
2	IO_L3P_D0_DIN_MISO_MISO1_2	R13	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T13	
2	IO_L5P_2	U15	LX9

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L5N_2	V15	LX9
2	IO_L12P_D1_MISO2_2	T14	
2	IO_L12N_D2_MISO3_2	V14	
2	IO_L13P_M1_2	N12	
2	IO_L13N_D10_2	P12	
2	IO_L14P_D11_2	U13	
2	IO_L14N_D12_2	V13	
2	IO_L15P_2	M11	LX9
2	IO_L15N_2	N11	LX9
2	IO_L16P_2	R11	
2	IO_L16N_VREF_2	T11	
2	IO_L19P_2	T12	LX9
2	IO_L19N_2	V12	LX9
2	IO_L20P_2	N10	LX9
2	IO_L20N_2	P11	LX9
2	IO_L22P_2	M10	LX9
2	IO_L22N_2	N9	LX9
2	IO_L23P_2	U11	
2	IO_L23N_2	V11	
2	IO_L29P_GCLK3_2	R10	
2	IO_L29N_GCLK2_2	T10	
2	IO_L30P_GCLK1_D13_2	U10	
2	IO_L30N_GCLK0_USERCCLK_2	V10	
2	IO_L31P_GCLK31_D14_2	R8	
2	IO_L31N_GCLK30_D15_2	T8	
2	IO_L32P_GCLK29_2	T9	
2	IO_L32N_GCLK28_2	V9	
2	IO_L40P_2	M8	LX9
2	IO_L40N_2	N8	LX9
2	IO_L41P_2	U8	
2	IO_L41N_VREF_2	V8	
2	IO_L43P_2	U7	
2	IO_L43N_2	V7	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L44P_2	N7	LX9
2	IO_L44N_2	P8	LX9
2	IO_L45P_2	T6	
2	IO_L45N_2	V6	
2	IO_L46P_2	R7	
2	IO_L46N_2	T7	
2	IO_L47P_2	N6	LX9
2	IO_L47N_2	P7	LX9
2	IO_L48P_D7_2	R5	
2	IO_L48N_RDWR_B_VREF_2	T5	
2	IO_L49P_D3_2	U5	
2	IO_L49N_D4_2	V5	
2	IO_L62P_D5_2	R3	
2	IO_L62N_D6_2	T3	
2	IO_L63P_2	T4	
2	IO_L63N_2	V4	
2	IO_L64P_D8_2	N5	
2	IO_L64N_D9_2	P6	
2	IO_L65P_INIT_B_2	U3	
2	IO_L65N_CSO_B_2	V3	
2	PROGRAM_B_2	V2	
3	IO_L1P_3	N4	
3	IO_L1N_VREF_3	N3	
3	IO_L2P_3	P4	
3	IO_L2N_3	P3	
3	IO_L31P_3	L6	
3	IO_L31N_VREF_3	M5	
3	IO_L32P_M3DQ14_3	U2	
3	IO_L32N_M3DQ15_3	U1	
3	IO_L33P_M3DQ12_3	T2	
3	IO_L33N_M3DQ13_3	T1	
3	IO_L34P_M3UDQS_3	P2	
3	IO_L34N_M3UDQSN_3	P1	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L35P_M3DQ10_3	N2	
3	IO_L35N_M3DQ11_3	N1	
3	IO_L36P_M3DQ8_3	M3	
3	IO_L36N_M3DQ9_3	M1	
3	IO_L37P_M3DQ0_3	L2	
3	IO_L37N_M3DQ1_3	L1	
3	IO_L38P_M3DQ2_3	K2	
3	IO_L38N_M3DQ3_3	K1	
3	IO_L39P_M3LDQS_3	L4	
3	IO_L39N_M3LDQSN_3	L3	
3	IO_L40P_M3DQ6_3	J3	
3	IO_L40N_M3DQ7_3	J1	
3	IO_L41P_GCLK27_M3DQ4_3	H2	
3	IO_L41N_GCLK26_M3DQ5_3	H1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	
3	IO_L42N_GCLK24_M3LDM_3	K3	
3	IO_L43P_GCLK23_M3RASN_3	L5	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	
3	IO_L44P_GCLK21_M3A5_3	H4	
3	IO_L44N_GCLK20_M3A6_3	H3	
3	IO_L45P_M3A3_3	L7	
3	IO_L45N_M3ODT_3	K6	
3	IO_L46P_M3CLK_3	G3	
3	IO_L46N_M3CLKN_3	G1	
3	IO_L47P_M3A0_3	J7	
3	IO_L47N_M3A1_3	J6	
3	IO_L48P_M3BA0_3	F2	
3	IO_L48N_M3BA1_3	F1	
3	IO_L49P_M3A7_3	H6	
3	IO_L49N_M3A2_3	H5	
3	IO_L50P_M3WE_3	E3	
3	IO_L50N_M3BA2_3	E1	
3	IO_L51P_M3A10_3	F4	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L51N_M3A4_3	F3	
3	IO_L52P_M3A8_3	D2	
3	IO_L52N_M3A9_3	D1	
3	IO_L53P_M3CKE_3	H7	
3	IO_L53N_M3A12_3	G6	
3	IO_L54P_M3RESET_3	E4	
3	IO_L54N_M3A11_3	D3	
3	IO_L55P_M3A13_3	F6	
3	IO_L55N_M3A14_3	F5	
3	IO_L83P_3	C2	
3	IO_L83N_VREF_3	C1	
NA	GND	A1	
NA	GND	A18	
NA	GND	B13	
NA	GND	B7	
NA	GND	C16	
NA	GND	C3	
NA	GND	D10	
NA	GND	D5	
NA	GND	E15	
NA	GND	G12	
NA	GND	G17	
NA	GND	G2	
NA	GND	G5	
NA	GND	H10	
NA	GND	H8	
NA	GND	J11	
NA	GND	J15	
NA	GND	J4	
NA	GND	J9	
NA	GND	K10	
NA	GND	K8	
NA	GND	L11	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	L9	
NA	GND	M17	
NA	GND	M2	
NA	GND	M6	
NA	GND	N13	
NA	GND	R1	
NA	GND	R14	
NA	GND	R18	
NA	GND	R4	
NA	GND	R9	
NA	GND	T16	
NA	GND	U12	
NA	GND	U6	
NA	GND	V1	
NA	GND	V18	
NA	VCCAUX	B1	
NA	VCCAUX	B17	
NA	VCCAUX	E14	
NA	VCCAUX	E5	
NA	VCCAUX	E9	
NA	VCCAUX	G10	
NA	VCCAUX	J12	
NA	VCCAUX	K7	
NA	VCCAUX	M9	
NA	VCCAUX	P10	
NA	VCCAUX	P14	
NA	VCCAUX	P5	
NA	VCCINT	G7	
NA	VCCINT	H11	
NA	VCCINT	H9	
NA	VCCINT	J10	
NA	VCCINT	J8	
NA	VCCINT	K11	

Table 2-5: **CSG324 Package—LX9, LX16, LX25, and LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	K9	
NA	VCCINT	L10	
NA	VCCINT	L8	
NA	VCCINT	M12	
NA	VCCINT	M7	
0	VCCO_0	B10	
0	VCCO_0	B15	
0	VCCO_0	B5	
0	VCCO_0	D13	
0	VCCO_0	D7	
0	VCCO_0	E10	
1	VCCO_1	E17	
1	VCCO_1	G15	
1	VCCO_1	J14	
1	VCCO_1	J17	
1	VCCO_1	M15	
1	VCCO_1	R17	
2	VCCO_2	P9	
2	VCCO_2	R12	
2	VCCO_2	R6	
2	VCCO_2	U14	
2	VCCO_2	U4	
2	VCCO_2	U9	
3	VCCO_3	E2	
3	VCCO_3	G4	
3	VCCO_3	J2	
3	VCCO_3	J5	
3	VCCO_3	M4	
3	VCCO_3	R2	

CSG324 Package—LX25T and LX45T

Table 2-6: **CSG324 Package—LX25T and LX45T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	
0	IO_L1N_VREF_0	A2	
0	IO_L2P_0	B3	
0	IO_L2N_0	A3	
0	IO_L34P_GCLK19_0	E6	
0	IO_L34N_GCLK18_0	F7	
0	IO_L35P_GCLK17_0	G8	
0	IO_L35N_GCLK16_0	E8	
0	IO_L36P_GCLK15_0	G9	
0	IO_L36N_GCLK14_0	G11	
0	IO_L37P_GCLK13_0	F12	
0	IO_L37N_GCLK12_0	E12	
0	IO_L64P_SCP5_0	C15	
0	IO_L64N_SCP4_0	A15	
0	IO_L65P_SCP3_0	B16	
0	IO_L65N_SCP2_0	A16	
0	IO_L66P_SCP1_0	E14	
0	IO_L66N_SCP0_0	D15	
NA	TCK	A17	
NA	TDI	F13	
NA	TMS	B18	
NA	TDO	D16	
1	IO_L1P_A25_1	F15	
1	IO_L1N_A24_VREF_1	F16	
1	IO_L29P_A23_M1A13_1	C17	
1	IO_L29N_A22_M1A14_1	C18	
1	IO_L30P_A21_M1RESET_1	F14	
1	IO_L30N_A20_M1A11_1	G14	
1	IO_L31P_A19_M1CKE_1	D17	
1	IO_L31N_A18_M1A12_1	D18	
1	IO_L32P_A17_M1A8_1	H12	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L32N_A16_M1A9_1	G13	
1	IO_L33P_A15_M1A10_1	E16	
1	IO_L33N_A14_M1A4_1	E18	
1	IO_L34P_A13_M1WE_1	K12	
1	IO_L34N_A12_M1BA2_1	K13	
1	IO_L35P_A11_M1A7_1	F17	
1	IO_L35N_A10_M1A2_1	F18	
1	IO_L36P_A9_M1BA0_1	H13	
1	IO_L36N_A8_M1BA1_1	H14	
1	IO_L37P_A7_M1A0_1	H15	
1	IO_L37N_A6_M1A1_1	H16	
1	IO_L38P_A5_M1CLK_1	G16	
1	IO_L38N_A4_M1CLKN_1	G18	
1	IO_L39P_M1A3_1	J13	
1	IO_L39N_M1ODT_1	K14	
1	IO_L40P_GCLK11_M1A5_1	L12	
1	IO_L40N_GCLK10_M1A6_1	L13	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K15	
1	IO_L41N_GCLK8_M1CASN_1	K16	
1	IO_L42P_GCLK7_M1UDM_1	L15	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L16	
1	IO_L43P_GCLK5_M1DQ4_1	H17	
1	IO_L43N_GCLK4_M1DQ5_1	H18	
1	IO_L44P_A3_M1DQ6_1	J16	
1	IO_L44N_A2_M1DQ7_1	J18	
1	IO_L45P_A1_M1LDQS_1	K17	
1	IO_L45N_A0_M1LDQSN_1	K18	
1	IO_L46P_FCS_B_M1DQ2_1	L17	
1	IO_L46N_FOE_B_M1DQ3_1	L18	
1	IO_L47P_FWE_B_M1DQ0_1	M16	
1	IO_L47N_LDC_M1DQ1_1	M18	
1	IO_L48P_HDC_M1DQ8_1	N17	
1	IO_L48N_M1DQ9_1	N18	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L49P_M1DQ10_1	P17	
1	IO_L49N_M1DQ11_1	P18	
1	IO_L50P_M1UDQS_1	N15	
1	IO_L50N_M1UDQSN_1	N16	
1	IO_L51P_M1DQ12_1	T17	
1	IO_L51N_M1DQ13_1	T18	
1	IO_L52P_M1DQ14_1	U17	
1	IO_L52N_M1DQ15_1	U18	
1	IO_L53P_1	M14	
1	IO_L53N_VREF_1	N14	
1	IO_L61P_1	L14	
1	IO_L61N_1	M13	
1	IO_L74P_AWAKE_1	P15	
1	IO_L74N_DOUT_BUSY_1	P16	
NA	SUSPEND	R16	
2	CMPCS_B_2	P13	
2	DONE_2	V17	
2	IO_L1P_CCLK_2	R15	
2	IO_L1N_M0_CMPMISO_2	T15	
2	IO_L2P_CMPCLK_2	U16	
2	IO_L2N_CMPMOSI_2	V16	
2	IO_L3P_D0_DIN_MISO_MISO1_2	R13	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T13	
2	IO_L5P_2	U15	
2	IO_L5N_2	V15	
2	IO_L12P_D1_MISO2_2	T14	
2	IO_L12N_D2_MISO3_2	V14	
2	IO_L13P_M1_2	N12	
2	IO_L13N_D10_2	P12	
2	IO_L14P_D11_2	U13	
2	IO_L14N_D12_2	V13	
2	IO_L15P_2	M11	
2	IO_L15N_2	N11	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L16P_2	R11	
2	IO_L16N_VREF_2	T11	
2	IO_L19P_2	T12	
2	IO_L19N_2	V12	
2	IO_L20P_2	N10	
2	IO_L20N_2	P11	
2	IO_L22P_2	M10	
2	IO_L22N_2	N9	
2	IO_L23P_2	U11	
2	IO_L23N_2	V11	
2	IO_L29P_GCLK3_2	R10	
2	IO_L29N_GCLK2_2	T10	
2	IO_L30P_GCLK1_D13_2	U10	
2	IO_L30N_GCLK0_USERCCLK_2	V10	
2	IO_L31P_GCLK31_D14_2	R8	
2	IO_L31N_GCLK30_D15_2	T8	
2	IO_L32P_GCLK29_2	T9	
2	IO_L32N_GCLK28_2	V9	
2	IO_L40P_2	M8	
2	IO_L40N_2	N8	
2	IO_L41P_2	U8	
2	IO_L41N_VREF_2	V8	
2	IO_L43P_2	U7	
2	IO_L43N_2	V7	
2	IO_L44P_2	N7	
2	IO_L44N_2	P8	
2	IO_L45P_2	T6	
2	IO_L45N_2	V6	
2	IO_L46P_2	R7	
2	IO_L46N_2	T7	
2	IO_L47P_2	N6	
2	IO_L47N_2	P7	
2	IO_L48P_D7_2	R5	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L48N_RDWR_B_VREF_2	T5	
2	IO_L49P_D3_2	U5	
2	IO_L49N_D4_2	V5	
2	IO_L62P_D5_2	R3	
2	IO_L62N_D6_2	T3	
2	IO_L63P_2	T4	
2	IO_L63N_2	V4	
2	IO_L64P_D8_2	N5	
2	IO_L64N_D9_2	P6	
2	IO_L65P_INIT_B_2	U3	
2	IO_L65N_CSO_B_2	V3	
2	PROGRAM_B_2	V2	
3	IO_L1P_3	N4	
3	IO_L1N_VREF_3	N3	
3	IO_L2P_3	P4	
3	IO_L2N_3	P3	
3	IO_L31P_3	L6	
3	IO_L31N_VREF_3	M5	
3	IO_L32P_M3DQ14_3	U2	
3	IO_L32N_M3DQ15_3	U1	
3	IO_L33P_M3DQ12_3	T2	
3	IO_L33N_M3DQ13_3	T1	
3	IO_L34P_M3UDQS_3	P2	
3	IO_L34N_M3UDQSN_3	P1	
3	IO_L35P_M3DQ10_3	N2	
3	IO_L35N_M3DQ11_3	N1	
3	IO_L36P_M3DQ8_3	M3	
3	IO_L36N_M3DQ9_3	M1	
3	IO_L37P_M3DQ0_3	L2	
3	IO_L37N_M3DQ1_3	L1	
3	IO_L38P_M3DQ2_3	K2	
3	IO_L38N_M3DQ3_3	K1	
3	IO_L39P_M3LDQS_3	L4	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L39N_M3LDQSN_3	L3	
3	IO_L40P_M3DQ6_3	J3	
3	IO_L40N_M3DQ7_3	J1	
3	IO_L41P_GCLK27_M3DQ4_3	H2	
3	IO_L41N_GCLK26_M3DQ5_3	H1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	
3	IO_L42N_GCLK24_M3LDM_3	K3	
3	IO_L43P_GCLK23_M3RASN_3	L5	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	
3	IO_L44P_GCLK21_M3A5_3	H4	
3	IO_L44N_GCLK20_M3A6_3	H3	
3	IO_L45P_M3A3_3	L7	
3	IO_L45N_M3ODT_3	K6	
3	IO_L46P_M3CLK_3	G3	
3	IO_L46N_M3CLKN_3	G1	
3	IO_L47P_M3A0_3	J7	
3	IO_L47N_M3A1_3	J6	
3	IO_L48P_M3BA0_3	F2	
3	IO_L48N_M3BA1_3	F1	
3	IO_L49P_M3A7_3	H6	
3	IO_L49N_M3A2_3	H5	
3	IO_L50P_M3WE_3	E3	
3	IO_L50N_M3BA2_3	E1	
3	IO_L51P_M3A10_3	F4	
3	IO_L51N_M3A4_3	F3	
3	IO_L52P_M3A8_3	D2	
3	IO_L52N_M3A9_3	D1	
3	IO_L53P_M3CKE_3	H7	
3	IO_L53N_M3A12_3	G6	
3	IO_L54P_M3RESET_3	E4	
3	IO_L54N_M3A11_3	D3	
3	IO_L55P_M3A13_3	F6	
3	IO_L55N_M3A14_3	F5	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L83P_3	C2	
3	IO_L83N_VREF_3	C1	
NA	MGTTXN0_101	A4	
NA	MGTTXP0_101	B4	
NA	MGTAVCCPLL0_101	B7	
NA	MGTREFCLK0N_101	A8	
NA	MGTREFCLK0P_101	B8	
NA	MGTRXN0_101	C5	
NA	MGTRXP0_101	D5	
NA	MGTRREF_101	E7	
NA	MGTRXN1_101	C7	
NA	MGTAVTTRCAL_101	E5	
NA	MGTRXP1_101	D7	
NA	MGTAVCCPLL1_101	D10	
NA	MGTREFCLK1N_101	C9	
NA	MGTREFCLK1P_101	D9	
NA	MGTTXN1_101	A6	
NA	MGTTXP1_101	B6	
NA	MGTTXN0_123	A12	LX25T
NA	MGTTXP0_123	B12	LX25T
NA	MGTAVCCPLL0_123	B11	LX25T
NA	MGTREFCLK0N_123	A10	LX25T
NA	MGTREFCLK0P_123	B10	LX25T
NA	MGTRXN0_123	C11	LX25T
NA	MGTRXP0_123	D11	LX25T
NA	MGTRXN1_123	C13	LX25T
NA	MGTRXP1_123	D13	LX25T
NA	MGTAVCCPLL1_123	E11	LX25T
NA	MGTREFCLK1N_123	E10	LX25T
NA	MGTREFCLK1P_123	F10	LX25T
NA	MGTTXN1_123	A14	LX25T
NA	MGTTXP1_123	B14	LX25T
NA	GND	A1	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A11	
NA	GND	A18	
NA	GND	A7	
NA	GND	A9	
NA	GND	B13	
NA	GND	B5	
NA	GND	B9	
NA	GND	C10	
NA	GND	C12	
NA	GND	C14	
NA	GND	C16	
NA	GND	C4	
NA	GND	C6	
NA	GND	D8	
NA	GND	E13	
NA	GND	E15	
NA	GND	F11	
NA	GND	F9	
NA	GND	G17	
NA	GND	G2	
NA	GND	G5	
NA	GND	H10	
NA	GND	H8	
NA	GND	J11	
NA	GND	J15	
NA	GND	J4	
NA	GND	J9	
NA	GND	K10	
NA	GND	K8	
NA	GND	L11	
NA	GND	L9	
NA	GND	M17	
NA	GND	M2	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M6	
NA	GND	N13	
NA	GND	R1	
NA	GND	R14	
NA	GND	R18	
NA	GND	R4	
NA	GND	R9	
NA	GND	T16	
NA	GND	U12	
NA	GND	U6	
NA	GND	V1	
NA	GND	V18	
NA	VCCAUX	B1	
NA	VCCAUX	B17	
NA	VCCAUX	D14	
NA	VCCAUX	D4	
NA	VCCAUX	G10	
NA	VCCAUX	J12	
NA	VCCAUX	K7	
NA	VCCAUX	M9	
NA	VCCAUX	P10	
NA	VCCAUX	P14	
NA	VCCAUX	P5	
NA	VCCINT	G7	
NA	VCCINT	H11	
NA	VCCINT	H9	
NA	VCCINT	J10	
NA	VCCINT	J8	
NA	VCCINT	K11	
NA	VCCINT	K9	
NA	VCCINT	L10	
NA	VCCINT	L8	
NA	VCCINT	M12	

Table 2-6: **CSG324 Package—LX25T and LX45T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	M7	
0	VCCO_0	B15	
0	VCCO_0	C3	
0	VCCO_0	F8	
0	VCCO_0	G12	
1	VCCO_1	E17	
1	VCCO_1	G15	
1	VCCO_1	J14	
1	VCCO_1	J17	
1	VCCO_1	M15	
1	VCCO_1	R17	
2	VCCO_2	P9	
2	VCCO_2	R12	
2	VCCO_2	R6	
2	VCCO_2	U14	
2	VCCO_2	U4	
2	VCCO_2	U9	
3	VCCO_3	E2	
3	VCCO_3	G4	
3	VCCO_3	J2	
3	VCCO_3	J5	
3	VCCO_3	M4	
3	VCCO_3	R2	
NA	MGTAVTTTX_101	A5	
NA	MGTAVTTTX_123	A13	LX25T
NA	MGTAVTTRX_101	D6	
NA	MGTAVTTRX_123	D12	LX25T
NA	MGTAVCC_101	C8	
NA	MGTAVCC_123	E9	LX25T

FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150

Data on the LX75 is not currently available.

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	
0	IO_L1N_VREF_0	A4	
0	IO_L2P_0	C5	
0	IO_L2N_0	A5	
0	IO_L3P_0	D6	
0	IO_L3N_0	C6	
0	IO_L4P_0	B6	
0	IO_L4N_0	A6	
0	IO_L5P_0	C7	
0	IO_L5N_0	A7	
0	IO_L6P_0	B8	
0	IO_L6N_0	A8	
0	IO_L7P_0	D9	
0	IO_L7N_0	C8	
0	IO_L8P_0	C9	
0	IO_L8N_VREF_0	A9	
0	IO_L14P_0	E8	LX25, LX45
0	IO_L14N_0	F8	LX25, LX45
0	IO_L15P_0	G8	LX25, LX45
0	IO_L15N_0	F9	LX25, LX45
0	IO_L16P_0	G9	LX25, LX45
0	IO_L16N_0	H10	LX25, LX45
0	IO_L17P_0	E10	LX25, LX45
0	IO_L17N_0	F10	LX25, LX45
0	IO_L18P_0	G11	LX25, LX45
0	IO_L18N_0	H11	LX25, LX45
0	IO_L32P_0	D7	
0	IO_L32N_0	D8	
0	IO_L33P_0	D10	
0	IO_L33N_0	C10	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L34P_GCLK19_0	B10	
0	IO_L34N_GCLK18_0	A10	
0	IO_L35P_GCLK17_0	C11	
0	IO_L35N_GCLK16_0	A11	
0	IO_L36P_GCLK15_0	D11	
0	IO_L36N_GCLK14_0	C12	
0	IO_L37P_GCLK13_0	B12	
0	IO_L37N_GCLK12_0	A12	
0	IO_L38P_0	C13	
0	IO_L38N_VREF_0	A13	
0	IO_L43P_0	E12	LX45
0	IO_L43N_0	D12	LX45
0	IO_L44P_0	H12	LX45
0	IO_L44N_0	F12	LX45
0	IO_L45P_0	F13	LX45
0	IO_L45N_0	D13	LX45
0	IO_L46P_0	H13	LX45
0	IO_L46N_0	G13	LX45
0	IO_L47P_0	E14	LX45
0	IO_L47N_0	F15	LX45
0	IO_L48P_0	F14	LX45
0	IO_L48N_0	H14	LX45
0	IO_L49P_0	D14	
0	IO_L49N_0	C14	
0	IO_L50P_0	B14	
0	IO_L50N_0	A14	
0	IO_L51P_0	C15	
0	IO_L51N_0	A15	
0	IO_L62P_0	D15	
0	IO_L62N_VREF_0	C16	
0	IO_L63P_SCP7_0	B16	
0	IO_L63N_SCP6_0	A16	
0	IO_L64P_SCP5_0	C17	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L64N_SCP4_0	A17	
0	IO_L65P_SCP3_0	B18	
0	IO_L65N_SCP2_0	A18	
0	IO_L66P_SCP1_0	E16	
0	IO_L66N_SCP0_0	D17	
NA	TCK	G15	
NA	TDI	E18	
NA	TMS	C18	
NA	TDO	A19	
1	IO_L1P_A25_1	C19	
1	IO_L1N_A24_VREF_1	B20	
1	IO_L9P_1	G16	LX25
1	IO_L9N_1	G17	LX25
1	IO_L10P_1	F16	LX25
1	IO_L10N_1	F17	LX25
1	IO_L19P_1	B21	
1	IO_L19N_1	B22	
1	IO_L20P_1	A20	
1	IO_L20N_1	A21	
1	IO_L21P_1	K16	LX25
1	IO_L21N_1	J16	LX25
1	IO_L28P_1	H16	LX25
1	IO_L28N_VREF_1	H17	LX25
1	IO_L29P_A23_M1A13_1	D19	
1	IO_L29N_A22_M1A14_1	D20	
1	IO_L30P_A21_M1RESET_1	F18	
1	IO_L30N_A20_M1A11_1	F19	
1	IO_L31P_A19_M1CKE_1	D21	
1	IO_L31N_A18_M1A12_1	D22	
1	IO_L32P_A17_M1A8_1	C20	
1	IO_L32N_A16_M1A9_1	C22	
1	IO_L33P_A15_M1A10_1	G19	
1	IO_L33N_A14_M1A4_1	F20	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L34P_A13_M1WE_1	H19	
1	IO_L34N_A12_M1BA2_1	H18	
1	IO_L35P_A11_M1A7_1	E20	
1	IO_L35N_A10_M1A2_1	E22	
1	IO_L36P_A9_M1BA0_1	J17	
1	IO_L36N_A8_M1BA1_1	K17	
1	IO_L37P_A7_M1A0_1	F21	
1	IO_L37N_A6_M1A1_1	F22	
1	IO_L38P_A5_M1CLK_1	H20	
1	IO_L38N_A4_M1CLKN_1	J19	
1	IO_L39P_M1A3_1	G20	
1	IO_L39N_M1ODT_1	G22	
1	IO_L40P_GCLK11_M1A5_1	K20	
1	IO_L40N_GCLK10_M1A6_1	K19	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	H21	
1	IO_L41N_GCLK8_M1CASN_1	H22	
1	IO_L42P_GCLK7_M1UDM_1	M20	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L19	
1	IO_L43P_GCLK5_M1DQ4_1	J20	
1	IO_L43N_GCLK4_M1DQ5_1	J22	
1	IO_L44P_A3_M1DQ6_1	K21	
1	IO_L44N_A2_M1DQ7_1	K22	
1	IO_L45P_A1_M1LDQS_1	L20	
1	IO_L45N_A0_M1LDQSN_1	L22	
1	IO_L46P_FCS_B_M1DQ2_1	M21	
1	IO_L46N_FOE_B_M1DQ3_1	M22	
1	IO_L47P_FWE_B_M1DQ0_1	N20	
1	IO_L47N_LDC_M1DQ1_1	N22	
1	IO_L48P_HDC_M1DQ8_1	P21	
1	IO_L48N_M1DQ9_1	P22	
1	IO_L49P_M1DQ10_1	R20	
1	IO_L49N_M1DQ11_1	R22	
1	IO_L50P_M1UDQS_1	T21	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L50N_M1UDQSN_1	T22	
1	IO_L51P_M1DQ12_1	U20	
1	IO_L51N_M1DQ13_1	U22	
1	IO_L52P_M1DQ14_1	V21	
1	IO_L52N_M1DQ15_1	V22	
1	IO_L53P_1	M19	
1	IO_L53N_VREF_1	N19	
1	IO_L58P_1	M16	LX25
1	IO_L58N_1	L15	LX25
1	IO_L59P_1	P19	
1	IO_L59N_1	P20	
1	IO_L60P_1	W20	
1	IO_L60N_1	W22	
1	IO_L61P_1	L17	
1	IO_L61N_1	K18	
1	IO_L70P_1	U19	LX25
1	IO_L70N_1	V20	LX25
1	IO_L71P_1	M17	LX25
1	IO_L71N_1	M18	LX25
1	IO_L72P_1	P17	LX25
1	IO_L72N_1	N16	LX25
1	IO_L73P_1	P18	LX25
1	IO_L73N_1	R19	LX25
1	IO_L74P_AWAKE_1	T19	
1	IO_L74N_DOUT_BUSY_1	T20	
NA	VFS	P16	LX25, LX45
NA	RFUSE	P15	LX25, LX45
NA	VBATT	R17	LX25, LX45
NA	SUSPEND	N15	
2	CMPCS_B_2	Y20	
2	DONE_2	Y22	
2	IO_L1P_CCLK_2	Y21	
2	IO_L1N_M0_CMPMISO_2	AA22	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L2P_CMPCLK_2	AA21	
2	IO_L2N_CMPMOSI_2	AB21	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AA20	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB20	
2	IO_L4P_2	T18	LX25
2	IO_L4N_VREF_2	T17	LX25
2	IO_L5P_2	Y19	
2	IO_L5N_2	AB19	
2	IO_L6P_2	W18	
2	IO_L6N_2	Y18	
2	IO_L7P_2	T16	LX25
2	IO_L7N_2	T15	LX25
2	IO_L8P_2	U17	LX25
2	IO_L8N_2	U16	LX25
2	IO_L9P_2	V19	LX25
2	IO_L9N_2	V18	LX25
2	IO_L10P_2	R16	LX25
2	IO_L10N_2	R15	LX25
2	IO_L11P_2	V17	LX25
2	IO_L11N_2	W17	LX25
2	IO_L12P_D1_MISO2_2	U14	
2	IO_L12N_D2_MISO3_2	U13	
2	IO_L13P_M1_2	U15	
2	IO_L13N_D10_2	V15	
2	IO_L14P_D11_2	AA18	
2	IO_L14N_D12_2	AB18	
2	IO_L15P_2	Y17	
2	IO_L15N_2	AB17	
2	IO_L16P_2	AA14	
2	IO_L16N_VREF_2	AB14	
2	IO_L17P_2	Y16	LX100
2	IO_L17N_2	W15	LX100
2	IO_L18P_2	V13	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L18N_2	W13	
2	IO_L19P_2	AA16	
2	IO_L19N_2	AB16	
2	IO_L20P_2	W14	
2	IO_L20N_2	Y14	
2	IO_L21P_2	Y15	
2	IO_L21N_2	AB15	
2	IO_L22P_2	T12	LX25, LX100
2	IO_L22N_2	U12	LX25, LX100
2	IO_L23P_2	T14	LX25
2	IO_L23N_2	R13	LX25
2	IO_L29P_GCLK3_2	W12	
2	IO_L29N_GCLK2_2	Y12	
2	IO_L30P_GCLK1_D13_2	Y13	
2	IO_L30N_GCLK0_USERCCLK_2	AB13	
2	IO_L31P_GCLK31_D14_2	AA12	
2	IO_L31N_GCLK30_D15_2	AB12	
2	IO_L32P_GCLK29_2	Y11	
2	IO_L32N_GCLK28_2	AB11	
2	IO_L40P_2	R11	
2	IO_L40N_2	T11	
2	IO_L41P_2	AA10	
2	IO_L41N_VREF_2	AB10	
2	IO_L42P_2	V11	
2	IO_L42N_2	W11	
2	IO_L43P_2	Y9	
2	IO_L43N_2	AB9	
2	IO_L44P_2	W10	
2	IO_L44N_2	Y10	
2	IO_L45P_2	AA8	
2	IO_L45N_2	AB8	
2	IO_L46P_2	W8	
2	IO_L46N_2	V7	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L47P_2	W9	
2	IO_L47N_2	Y8	
2	IO_L48P_D7_2	Y7	
2	IO_L48N_RDWR_B_VREF_2	AB7	
2	IO_L49P_D3_2	AA6	
2	IO_L49N_D4_2	AB6	
2	IO_L50P_2	U9	
2	IO_L50N_2	V9	
2	IO_L51P_2	T8	LX25, LX100
2	IO_L51N_2	U8	LX25, LX100
2	IO_L52P_2	T10	LX25, LX100
2	IO_L52N_2	U10	LX25, LX100
2	IO_L53P_2	W6	LX100
2	IO_L53N_2	Y6	LX100
2	IO_L54P_2	Y5	LX100
2	IO_L54N_2	AB5	LX100
2	IO_L57P_2	AA4	
2	IO_L57N_2	AB4	
2	IO_L58P_2	Y3	
2	IO_L58N_2	AB3	
2	IO_L59P_2	R9	
2	IO_L59N_2	R8	
2	IO_L60P_2	T7	
2	IO_L60N_2	R7	
2	IO_L62P_D5_2	W4	
2	IO_L62N_D6_2	Y4	
2	IO_L63P_2	U6	
2	IO_L63N_2	V5	
2	IO_L64P_D8_2	AA2	
2	IO_L64N_D9_2	AB2	
2	IO_L65P_INIT_B_2	T6	
2	IO_L65N_CSO_B_2	T5	
2	PROGRAM_B_2	AA1	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L1P_3	Y2	
3	IO_L1N_VREF_3	Y1	
3	IO_L2P_3	W3	
3	IO_L2N_3	W1	
3	IO_L7P_3	P8	LX25
3	IO_L7N_3	P7	LX25
3	IO_L8P_3	P6	LX25
3	IO_L8N_3	P5	LX25
3	IO_L9P_3	T4	
3	IO_L9N_3	T3	
3	IO_L10P_3	U4	
3	IO_L10N_3	V3	
3	IO_L11P_3	N6	LX25
3	IO_L11N_3	N7	LX25
3	IO_L23P_3	M7	LX25
3	IO_L23N_3	M8	LX25
3	IO_L24P_3	R4	LX25
3	IO_L24N_3	P4	LX25
3	IO_L25P_3	M6	LX25
3	IO_L25N_3	L6	LX25
3	IO_L26P_3	P3	LX25
3	IO_L26N_3	N4	LX25
3	IO_L31P_3	M5	
3	IO_L31N_VREF_3	M4	
3	IO_L32P_M3DQ14_3	V2	
3	IO_L32N_M3DQ15_3	V1	
3	IO_L33P_M3DQ12_3	U3	
3	IO_L33N_M3DQ13_3	U1	
3	IO_L34P_M3UDQS_3	T2	
3	IO_L34N_M3UDQSN_3	T1	
3	IO_L35P_M3DQ10_3	R3	
3	IO_L35N_M3DQ11_3	R1	
3	IO_L36P_M3DQ8_3	P2	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L36N_M3DQ9_3	P1	
3	IO_L37P_M3DQ0_3	N3	
3	IO_L37N_M3DQ1_3	N1	
3	IO_L38P_M3DQ2_3	M2	
3	IO_L38N_M3DQ3_3	M1	
3	IO_L39P_M3LDQS_3	L3	
3	IO_L39N_M3LDQSN_3	L1	
3	IO_L40P_M3DQ6_3	K2	
3	IO_L40N_M3DQ7_3	K1	
3	IO_L41P_GCLK27_M3DQ4_3	J3	
3	IO_L41N_GCLK26_M3DQ5_3	J1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	M3	
3	IO_L42N_GCLK24_M3LDM_3	L4	
3	IO_L43P_GCLK23_M3RASN_3	K5	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K4	
3	IO_L44P_GCLK21_M3A5_3	K3	
3	IO_L44N_GCLK20_M3A6_3	J4	
3	IO_L45P_M3A3_3	K6	
3	IO_L45N_M3ODT_3	J6	
3	IO_L46P_M3CLK_3	H4	
3	IO_L46N_M3CLKN_3	H3	
3	IO_L47P_M3A0_3	H2	
3	IO_L47N_M3A1_3	H1	
3	IO_L48P_M3BA0_3	G3	
3	IO_L48N_M3BA1_3	G1	
3	IO_L49P_M3A7_3	H6	
3	IO_L49N_M3A2_3	H5	
3	IO_L50P_M3WE_3	F2	
3	IO_L50N_M3BA2_3	F1	
3	IO_L51P_M3A10_3	G4	
3	IO_L51N_M3A4_3	F3	
3	IO_L52P_M3A8_3	E3	
3	IO_L52N_M3A9_3	E1	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L53P_M3CKE_3	D2	
3	IO_L53N_M3A12_3	D1	
3	IO_L54P_M3RESET_3	C3	
3	IO_L54N_M3A11_3	C1	
3	IO_L55P_M3A13_3	G6	
3	IO_L55N_M3A14_3	F5	
3	IO_L57P_3	K7	LX25
3	IO_L57N_VREF_3	K8	LX25
3	IO_L58P_3	D5	LX25
3	IO_L58N_3	E4	LX25
3	IO_L59P_3	J7	
3	IO_L59N_3	H8	
3	IO_L60P_3	B2	
3	IO_L60N_3	B1	
3	IO_L80P_3	G7	LX25
3	IO_L80N_3	F7	LX25
3	IO_L81P_3	D3	LX25
3	IO_L81N_3	C4	LX25
3	IO_L82P_3	E5	LX25
3	IO_L82N_3	E6	LX25
3	IO_L83P_3	A2	
3	IO_L83N_VREF_3	B3	
NA	GND	A1	
NA	GND	A22	
NA	GND	AA13	
NA	GND	AA17	
NA	GND	AA5	
NA	GND	AA9	
NA	GND	AB1	
NA	GND	AB22	
NA	GND	B13	
NA	GND	B17	
NA	GND	B5	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B9	
NA	GND	D18	
NA	GND	D4	
NA	GND	E11	
NA	GND	E15	
NA	GND	E2	
NA	GND	E21	
NA	GND	E7	
NA	GND	G18	
NA	GND	G5	
NA	GND	H7	
NA	GND	J11	
NA	GND	J13	
NA	GND	J15	
NA	GND	J2	
NA	GND	J21	
NA	GND	J9	
NA	GND	K10	
NA	GND	K12	
NA	GND	K14	
NA	GND	L11	
NA	GND	L13	
NA	GND	L18	
NA	GND	L5	
NA	GND	L9	
NA	GND	M10	
NA	GND	M12	
NA	GND	M14	
NA	GND	N11	
NA	GND	N13	
NA	GND	N17	
NA	GND	N2	
NA	GND	N21	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N9	
NA	GND	P10	
NA	GND	P12	
NA	GND	P14	
NA	GND	R18	
NA	GND	R5	
NA	GND	U2	
NA	GND	U21	
NA	GND	U7	
NA	GND	V10	
NA	GND	V14	
NA	GND	V4	
NA	GND	W16	
NA	GND	W19	
NA	GND	W7	
NA	VCCAUX	D16	
NA	VCCAUX	F11	
NA	VCCAUX	G12	
NA	VCCAUX	H15	
NA	VCCAUX	H9	
NA	VCCAUX	K15	
NA	VCCAUX	L8	
NA	VCCAUX	M15	
NA	VCCAUX	N8	
NA	VCCAUX	R10	
NA	VCCAUX	R12	
NA	VCCAUX	R6	
NA	VCCAUX	U11	
NA	VCCAUX	V6	
NA	VCCINT	J10	
NA	VCCINT	J12	
NA	VCCINT	J14	
NA	VCCINT	J8	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	K11	
NA	VCCINT	K13	
NA	VCCINT	K9	
NA	VCCINT	L10	
NA	VCCINT	L12	
NA	VCCINT	L14	
NA	VCCINT	M11	
NA	VCCINT	M13	
NA	VCCINT	M9	
NA	VCCINT	N10	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	P9	
NA	VCCINT	R14	
0	VCCO_0	B11	
0	VCCO_0	B15	
0	VCCO_0	B19	
0	VCCO_0	B4	
0	VCCO_0	B7	
0	VCCO_0	E13	
0	VCCO_0	E17	
0	VCCO_0	E9	
0	VCCO_0	G10	
0	VCCO_0	G14	
1	VCCO_1	C21	
1	VCCO_1	E19	
1	VCCO_1	G21	
1	VCCO_1	J18	
1	VCCO_1	L16	
1	VCCO_1	L21	
1	VCCO_1	N18	

Table 2-7: **FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	VCCO_1	R21	
1	VCCO_1	U18	
1	VCCO_1	W21	
2	VCCO_2	AA11	
2	VCCO_2	AA15	
2	VCCO_2	AA19	
2	VCCO_2	AA3	
2	VCCO_2	AA7	
2	VCCO_2	T13	
2	VCCO_2	T9	
2	VCCO_2	V12	
2	VCCO_2	V16	
2	VCCO_2	V8	
2	VCCO_2	W5	
3	VCCO_3	C2	
3	VCCO_3	F4	
3	VCCO_3	F6	
3	VCCO_3	G2	
3	VCCO_3	J5	
3	VCCO_3	L2	
3	VCCO_3	L7	
3	VCCO_3	N5	
3	VCCO_3	R2	
3	VCCO_3	U5	
3	VCCO_3	W2	

FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T

Data on the LX75T is not currently available.

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	C3	
0	IO_L1N_VREF_0	D3	
0	IO_L2P_0	D4	
0	IO_L2N_0	D5	
0	IO_L3P_0	B2	
0	IO_L3N_0	A2	
0	IO_L4P_0	E5	
0	IO_L4N_0	E6	
0	IO_L5P_0	B3	
0	IO_L5N_0	A3	
0	IO_L6P_0	C4	
0	IO_L6N_0	A4	
0	IO_L7P_0	F7	
0	IO_L7N_0	F8	
0	IO_L8P_0	C5	
0	IO_L8N_VREF_0	A5	
NA	MGTTXN0_101	A6	
NA	MGTTXP0_101	B6	
NA	MGTAVCCPLL0_101	B9	
NA	MGTREFCLK0N_101	B10	
NA	MGTREFCLK0P_101	A10	
NA	MGTRXN0_101	C7	
NA	MGTRXP0_101	D7	
NA	MGTRREF_101	E9	
NA	MGTRXN1_101	C9	
NA	MGTAVTTRCAL_101	E8	
NA	MGTRXP1_101	D9	
NA	MGTAVCCPLL1_101	D12	
NA	MGTREFCLK1N_101	D11	
NA	MGTREFCLK1P_101	C11	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXN1_101	A8	
NA	MGTTXP1_101	B8	
0	IO_L32P_0	G8	
0	IO_L32N_0	F9	
0	IO_L33P_0	H10	
0	IO_L33N_0	H11	
0	IO_L34P_GCLK19_0	G9	
0	IO_L34N_GCLK18_0	F10	
0	IO_L35P_GCLK17_0	H12	
0	IO_L35N_GCLK16_0	G11	
0	IO_L36P_GCLK15_0	F14	
0	IO_L36N_GCLK14_0	F15	
0	IO_L37P_GCLK13_0	E16	
0	IO_L37N_GCLK12_0	F16	
0	IO_L38P_0	H13	
0	IO_L38N_VREF_0	G13	
NA	MGTTXN0_123	A14	LX25T
NA	MGTTXP0_123	B14	LX25T
NA	MGTAVCCPLL0_123	B13	LX25T
NA	MGTREFCLK0N_123	B12	LX25T
NA	MGTREFCLK0P_123	A12	LX25T
NA	MGTRXN0_123	C13	LX25T
NA	MGTRXP0_123	D13	LX25T
NA	MGTRXN1_123	C15	LX25T
NA	MGTRXP1_123	D15	LX25T
NA	MGTAVCCPLL1_123	E13	LX25T
NA	MGTREFCLK1N_123	F12	LX25T
NA	MGTREFCLK1P_123	E12	LX25T
NA	MGTTXN1_123	A16	LX25T
NA	MGTTXP1_123	B16	LX25T
0	IO_L49P_0	H14	
0	IO_L49N_0	G15	
0	IO_L50P_0	C17	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L50N_0	A17	
0	IO_L51P_0	G16	
0	IO_L51N_0	F17	
0	IO_L62P_0	D18	
0	IO_L62N_VREF_0	D19	
0	IO_L63P_SCP7_0	B18	
0	IO_L63N_SCP6_0	A18	
0	IO_L64P_SCP5_0	C19	
0	IO_L64N_SCP4_0	A19	
0	IO_L65P_SCP3_0	B20	
0	IO_L65N_SCP2_0	A20	
0	IO_L66P_SCP1_0	D17	
0	IO_L66N_SCP0_0	C18	
NA	TCK	A21	
NA	TDI	E18	
NA	TMS	D20	
NA	TDO	G17	
1	IO_L1P_A25_1	F18	
1	IO_L1N_A24_VREF_1	F19	
1	IO_L9P_1	H16	LX25T
1	IO_L9N_1	H17	LX25T
1	IO_L10P_1	B21	LX25T
1	IO_L10N_1	B22	LX25T
1	IO_L19P_1	J16	
1	IO_L19N_1	J17	
1	IO_L20P_1	C20	
1	IO_L20N_1	C22	
1	IO_L21P_1	L15	LX25T
1	IO_L21N_1	K16	LX25T
1	IO_L28P_1	D21	LX25T
1	IO_L28N_VREF_1	D22	LX25T
1	IO_L29P_A23_M1A13_1	G19	
1	IO_L29N_A22_M1A14_1	F20	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L30P_A21_M1RESET_1	H18	
1	IO_L30N_A20_M1A11_1	H19	
1	IO_L31P_A19_M1CKE_1	F21	
1	IO_L31N_A18_M1A12_1	F22	
1	IO_L32P_A17_M1A8_1	E20	
1	IO_L32N_A16_M1A9_1	E22	
1	IO_L33P_A15_M1A10_1	J19	
1	IO_L33N_A14_M1A4_1	H20	
1	IO_L34P_A13_M1WE_1	K19	
1	IO_L34N_A12_M1BA2_1	K18	
1	IO_L35P_A11_M1A7_1	G20	
1	IO_L35N_A10_M1A2_1	G22	
1	IO_L36P_A9_M1BA0_1	K17	
1	IO_L36N_A8_M1BA1_1	L17	
1	IO_L37P_A7_M1A0_1	H21	
1	IO_L37N_A6_M1A1_1	H22	
1	IO_L38P_A5_M1CLK_1	K20	
1	IO_L38N_A4_M1CLKN_1	L19	
1	IO_L39P_M1A3_1	J20	
1	IO_L39N_M1ODT_1	J22	
1	IO_L40P_GCLK11_M1A5_1	M20	
1	IO_L40N_GCLK10_M1A6_1	M19	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K21	
1	IO_L41N_GCLK8_M1CASN_1	K22	
1	IO_L42P_GCLK7_M1UDM_1	P20	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	N19	
1	IO_L43P_GCLK5_M1DQ4_1	L20	
1	IO_L43N_GCLK4_M1DQ5_1	L22	
1	IO_L44P_A3_M1DQ6_1	M21	
1	IO_L44N_A2_M1DQ7_1	M22	
1	IO_L45P_A1_M1LDQS_1	N20	
1	IO_L45N_A0_M1LDQSN_1	N22	
1	IO_L46P_FCS_B_M1DQ2_1	P21	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L46N_FOE_B_M1DQ3_1	P22	
1	IO_L47P_FWE_B_M1DQ0_1	R20	
1	IO_L47N_LDC_M1DQ1_1	R22	
1	IO_L48P_HDC_M1DQ8_1	T21	
1	IO_L48N_M1DQ9_1	T22	
1	IO_L49P_M1DQ10_1	U20	
1	IO_L49N_M1DQ11_1	U22	
1	IO_L50P_M1UDQS_1	V21	
1	IO_L50N_M1UDQSN_1	V22	
1	IO_L51P_M1DQ12_1	W20	
1	IO_L51N_M1DQ13_1	W22	
1	IO_L52P_M1DQ14_1	Y21	
1	IO_L52N_M1DQ15_1	Y22	
1	IO_L53P_1	P19	
1	IO_L53N_VREF_1	R19	
1	IO_L58P_1	M16	LX25T
1	IO_L58N_1	N15	LX25T
1	IO_L59P_1	U19	
1	IO_L59N_1	T20	
1	IO_L60P_1	N16	
1	IO_L60N_1	P16	
1	IO_L61P_1	M17	
1	IO_L61N_1	M18	
1	IO_L70P_1	R15	LX25T
1	IO_L70N_1	R16	LX25T
1	IO_L71P_1	P17	LX25T
1	IO_L71N_1	P18	LX25T
1	IO_L72P_1	R17	LX25T
1	IO_L72N_1	T17	LX25T
1	IO_L73P_1	T19	LX25T
1	IO_L73N_1	T18	LX25T
1	IO_L74P_AWAKE_1	V19	
1	IO_L74N_DOUT_BUSY_1	V20	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VFS	U17	LX25T, LX45T
NA	RFUSE	P15	LX25T, LX45T
NA	VBATT	T16	LX25T, LX45T
NA	SUSPEND	AA22	
2	CMPCS_B_2	V18	
2	DONE_2	AB21	
2	IO_L1P_CCLK_2	Y20	
2	IO_L1N_M0_CMPMISO_2	AA21	
2	IO_L2P_CMPCLK_2	V17	
2	IO_L2N_CMPMOSI_2	W18	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AA20	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB20	
2	IO_L4P_2	U16	LX25T
2	IO_L4N_VREF_2	V15	LX25T
2	IO_L5P_2	W17	
2	IO_L5N_2	Y18	
2	IO_L6P_2	AA14	
2	IO_L6N_2	AB14	
2	IO_L12P_D1_MISO2_2	R13	
2	IO_L12N_D2_MISO3_2	T14	
2	IO_L13P_M1_2	Y19	
2	IO_L13N_D10_2	AB19	
2	IO_L14P_D11_2	AA18	
2	IO_L14N_D12_2	AB18	
2	IO_L15P_2	Y17	
2	IO_L15N_2	AB17	
2	IO_L16P_2	U14	
2	IO_L16N_VREF_2	U13	
2	IO_L17P_2	Y16	
2	IO_L17N_2	W15	
2	IO_L18P_2	V13	
2	IO_L18N_2	W13	
2	IO_L19P_2	AA16	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L19N_2	AB16	
2	IO_L20P_2	W14	
2	IO_L20N_2	Y14	
2	IO_L21P_2	Y15	
2	IO_L21N_2	AB15	
2	IO_L22P_2	R11	LX25T
2	IO_L22N_2	T11	LX25T
2	IO_L23P_2	T15	LX25T
2	IO_L23N_2	U15	LX25T
2	IO_L29P_GCLK3_2	T12	
2	IO_L29N_GCLK2_2	U12	
2	IO_L30P_GCLK1_D13_2	Y13	
2	IO_L30N_GCLK0_USERCCLK_2	AB13	
2	IO_L31P_GCLK31_D14_2	AA12	
2	IO_L31N_GCLK30_D15_2	AB12	
2	IO_L32P_GCLK29_2	Y11	
2	IO_L32N_GCLK28_2	AB11	
2	IO_L40P_2	W12	
2	IO_L40N_2	Y12	
2	IO_L41P_2	AA10	
2	IO_L41N_VREF_2	AB10	
2	IO_L42P_2	V11	
2	IO_L42N_2	W11	
2	IO_L43P_2	Y9	
2	IO_L43N_2	AB9	
2	IO_L44P_2	W10	
2	IO_L44N_2	Y10	
2	IO_L45P_2	AA8	
2	IO_L45N_2	AB8	
2	IO_L46P_2	T10	
2	IO_L46N_2	U10	
2	IO_L47P_2	Y7	
2	IO_L47N_2	AB7	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L48P_D7_2	W9	
2	IO_L48N_RDWR_B_VREF_2	Y8	
2	IO_L49P_D3_2	AA6	
2	IO_L49N_D4_2	AB6	
2	IO_L50P_2	U9	
2	IO_L50N_2	V9	
2	IO_L57P_2	T8	
2	IO_L57N_2	U8	
2	IO_L58P_2	V7	
2	IO_L58N_2	W8	
2	IO_L59P_2	R9	
2	IO_L59N_2	R8	
2	IO_L60P_2	W6	
2	IO_L60N_2	Y6	
2	IO_L62P_D5_2	Y5	
2	IO_L62N_D6_2	AB5	
2	IO_L63P_2	AA4	
2	IO_L63N_2	AB4	
2	IO_L64P_D8_2	T7	
2	IO_L64N_D9_2	U6	
2	IO_L65P_INIT_B_2	Y4	
2	IO_L65N_CSO_B_2	AA3	
2	PROGRAM_B_2	AB2	
3	IO_L1P_3	R7	
3	IO_L1N_VREF_3	P8	
3	IO_L2P_3	W4	
3	IO_L2N_3	Y3	
3	IO_L7P_3	T6	LX25T
3	IO_L7N_3	T5	LX25T
3	IO_L8P_3	V5	LX25T
3	IO_L8N_3	V3	LX25T
3	IO_L9P_3	P5	
3	IO_L9N_3	P4	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L10P_3	AA2	
3	IO_L10N_3	AA1	
3	IO_L23P_3	N6	LX25T
3	IO_L23N_3	N7	LX25T
3	IO_L24P_3	U4	LX25T
3	IO_L24N_3	T4	LX25T
3	IO_L25P_3	P6	LX25T
3	IO_L25N_3	P7	LX25T
3	IO_L26P_3	T3	LX25T
3	IO_L26N_3	R4	LX25T
3	IO_L31P_3	M7	
3	IO_L31N_VREF_3	M8	
3	IO_L32P_M3DQ14_3	Y2	
3	IO_L32N_M3DQ15_3	Y1	
3	IO_L33P_M3DQ12_3	W3	
3	IO_L33N_M3DQ13_3	W1	
3	IO_L34P_M3UDQS_3	V2	
3	IO_L34N_M3UDQSN_3	V1	
3	IO_L35P_M3DQ10_3	U3	
3	IO_L35N_M3DQ11_3	U1	
3	IO_L36P_M3DQ8_3	T2	
3	IO_L36N_M3DQ9_3	T1	
3	IO_L37P_M3DQ0_3	R3	
3	IO_L37N_M3DQ1_3	R1	
3	IO_L38P_M3DQ2_3	P2	
3	IO_L38N_M3DQ3_3	P1	
3	IO_L39P_M3LDQS_3	N3	
3	IO_L39N_M3LDQSN_3	N1	
3	IO_L40P_M3DQ6_3	M2	
3	IO_L40N_M3DQ7_3	M1	
3	IO_L41P_GCLK27_M3DQ4_3	L3	
3	IO_L41N_GCLK26_M3DQ5_3	L1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	P3	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L42N_GCLK24_M3LDM_3	N4	
3	IO_L43P_GCLK23_M3RASN_3	M5	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	M4	
3	IO_L44P_GCLK21_M3A5_3	M3	
3	IO_L44N_GCLK20_M3A6_3	L4	
3	IO_L45P_M3A3_3	M6	
3	IO_L45N_M3ODT_3	L6	
3	IO_L46P_M3CLK_3	K4	
3	IO_L46N_M3CLKN_3	K3	
3	IO_L47P_M3A0_3	K2	
3	IO_L47N_M3A1_3	K1	
3	IO_L48P_M3BA0_3	J3	
3	IO_L48N_M3BA1_3	J1	
3	IO_L49P_M3A7_3	K6	
3	IO_L49N_M3A2_3	K5	
3	IO_L50P_M3WE_3	H2	
3	IO_L50N_M3BA2_3	H1	
3	IO_L51P_M3A10_3	J4	
3	IO_L51N_M3A4_3	H3	
3	IO_L52P_M3A8_3	G3	
3	IO_L52N_M3A9_3	G1	
3	IO_L53P_M3CKE_3	F2	
3	IO_L53N_M3A12_3	F1	
3	IO_L54P_M3RESET_3	E3	
3	IO_L54N_M3A11_3	E1	
3	IO_L55P_M3A13_3	J6	
3	IO_L55N_M3A14_3	H5	
3	IO_L57P_3	K7	LX25T
3	IO_L57N_VREF_3	K8	LX25T
3	IO_L58P_3	H4	LX25T
3	IO_L58N_3	G4	LX25T
3	IO_L59P_3	D2	
3	IO_L59N_3	D1	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L60P_3	F3	
3	IO_L60N_3	E4	
3	IO_L80P_3	H6	LX25T
3	IO_L80N_3	G7	LX25T
3	IO_L81P_3	J7	LX25T
3	IO_L81N_3	H8	LX25T
3	IO_L82P_3	F5	LX25T
3	IO_L82N_3	G6	LX25T
3	IO_L83P_3	C1	
3	IO_L83N_VREF_3	B1	
NA	GND	A1	
NA	GND	A11	
NA	GND	A13	
NA	GND	A22	
NA	GND	A9	
NA	GND	AA13	
NA	GND	AA17	
NA	GND	AA5	
NA	GND	AA9	
NA	GND	AB1	
NA	GND	AB22	
NA	GND	B11	
NA	GND	B15	
NA	GND	B17	
NA	GND	B5	
NA	GND	B7	
NA	GND	C12	
NA	GND	C14	
NA	GND	C16	
NA	GND	C6	
NA	GND	C8	
NA	GND	D10	
NA	GND	D16	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	D6	
NA	GND	E11	
NA	GND	E14	
NA	GND	E15	
NA	GND	E2	
NA	GND	E21	
NA	GND	E7	
NA	GND	F13	
NA	GND	G18	
NA	GND	G5	
NA	GND	H7	
NA	GND	J11	
NA	GND	J13	
NA	GND	J15	
NA	GND	J2	
NA	GND	J21	
NA	GND	J9	
NA	GND	K10	
NA	GND	K12	
NA	GND	K14	
NA	GND	L11	
NA	GND	L13	
NA	GND	L18	
NA	GND	L5	
NA	GND	L9	
NA	GND	M10	
NA	GND	M12	
NA	GND	M14	
NA	GND	N11	
NA	GND	N13	
NA	GND	N17	
NA	GND	N2	
NA	GND	N21	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N9	
NA	GND	P10	
NA	GND	P12	
NA	GND	P14	
NA	GND	R18	
NA	GND	R5	
NA	GND	U2	
NA	GND	U21	
NA	GND	U7	
NA	GND	V10	
NA	GND	V14	
NA	GND	V4	
NA	GND	W16	
NA	GND	W19	
NA	GND	W7	
NA	MGTAVCC_101	C10	
NA	MGTAVCC_123	E10	LX25T
NA	MGTAVTTRX_101	D8	
NA	MGTAVTTRX_123	D14	LX25T
NA	MGTAVTTTX_101	A7	
NA	MGTAVTTTX_123	A15	LX25T
NA	VCCAUX	F11	
NA	VCCAUX	G12	
NA	VCCAUX	H15	
NA	VCCAUX	H9	
NA	VCCAUX	K15	
NA	VCCAUX	L8	
NA	VCCAUX	M15	
NA	VCCAUX	N8	
NA	VCCAUX	R10	
NA	VCCAUX	R12	
NA	VCCAUX	R6	
NA	VCCAUX	U11	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	V6	
NA	VCCINT	J10	
NA	VCCINT	J12	
NA	VCCINT	J14	
NA	VCCINT	J8	
NA	VCCINT	K11	
NA	VCCINT	K13	
NA	VCCINT	K9	
NA	VCCINT	L10	
NA	VCCINT	L12	
NA	VCCINT	L14	
NA	VCCINT	M11	
NA	VCCINT	M13	
NA	VCCINT	M9	
NA	VCCINT	N10	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	P9	
NA	VCCINT	R14	
0	VCCO_0	B19	
0	VCCO_0	B4	
0	VCCO_0	E17	
0	VCCO_0	F6	
0	VCCO_0	G10	
0	VCCO_0	G14	
1	VCCO_1	C21	
1	VCCO_1	E19	
1	VCCO_1	G21	
1	VCCO_1	J18	
1	VCCO_1	L16	
1	VCCO_1	L21	

Table 2-8: **FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	VCCO_1	N18	
1	VCCO_1	R21	
1	VCCO_1	U18	
1	VCCO_1	W21	
2	VCCO_2	AA11	
2	VCCO_2	AA15	
2	VCCO_2	AA19	
2	VCCO_2	AA7	
2	VCCO_2	AB3	
2	VCCO_2	T13	
2	VCCO_2	T9	
2	VCCO_2	V12	
2	VCCO_2	V16	
2	VCCO_2	V8	
2	VCCO_2	W5	
3	VCCO_3	C2	
3	VCCO_3	F4	
3	VCCO_3	G2	
3	VCCO_3	J5	
3	VCCO_3	L2	
3	VCCO_3	L7	
3	VCCO_3	N5	
3	VCCO_3	R2	
3	VCCO_3	U5	
3	VCCO_3	W2	

CSG484 Package—LX45, LX75, LX100, and LX150

Table 2-9: **CSG484 Package—LX45, LX75, LX100, and LX150**

Bank	Pin Description	Pin Number	No Connect (NC)
Data is not currently available on devices in this package.			

CSG484 Package—LX45T, LX75T, LX100T, and LX150T

Table 2-10: **CSG484 Package—LX45T, LX75T, LX100T, and LX150T**

Bank	Pin Description	Pin Number	No Connect (NC)
Data is not currently available on devices in this package.			

FG(G)676 Package—LX45

Table 2-11: **FG(G)676 Package—LX45**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	
0	IO_L1N_VREF_0	A2	
0	IO_L2P_0	B4	
0	IO_L2N_0	A4	
0	IO_L4P_0	C5	
0	IO_L4N_0	A5	
0	IO_L6P_0	B6	
0	IO_L6N_0	A6	
0	IO_L12P_0	C7	
0	IO_L12N_0	A7	
0	IO_L16P_0	B8	
0	IO_L16N_0	A8	
0	IO_L17P_0	C9	
0	IO_L17N_0	A9	
0	IO_L8P_0	D6	
0	IO_L8N_VREF_0	C6	
0	IO_L24P_0	C11	
0	IO_L24N_0	A11	
0	IO_L26P_0	B12	
0	IO_L26N_0	A12	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L34P_GCLK19_0	C13	
0	IO_L34N_GCLK18_0	A13	
0	IO_L35P_GCLK17_0	B14	
0	IO_L35N_GCLK16_0	A14	
0	IO_L36P_GCLK15_0	D14	
0	IO_L36N_GCLK14_0	C14	
0	IO_L37P_GCLK13_0	C15	
0	IO_L37N_GCLK12_0	A15	
0	IO_L38P_0	B16	
0	IO_L38N_VREF_0	A16	
0	IO_L50P_0	C17	
0	IO_L50N_0	A17	
0	IO_L52P_0	D18	
0	IO_L52N_0	C18	
0	IO_L56P_0	D21	
0	IO_L56N_0	C20	
0	IO_L62P_0	B18	
0	IO_L62N_VREF_0	A18	
0	IO_L63P_SCP7_0	C19	
0	IO_L63N_SCP6_0	A19	
0	IO_L64P_SCP5_0	B20	
0	IO_L64N_SCP4_0	A20	
0	IO_L65P_SCP3_0	C21	
0	IO_L65N_SCP2_0	A21	
0	IO_L66P_SCP1_0	B22	
0	IO_L66N_SCP0_0	A22	
NA	TCK	E21	
NA	TDI	F20	
NA	TMS	C23	
NA	TDO	A24	
1	IO_L1P_A25_1	B23	
1	IO_L1N_A24_VREF_1	A23	
1	IO_L10P_1	B24	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L10N_1	A25	
1	IO_L11P_1	C25	
1	IO_L11N_1	C26	
1	IO_L12P_1	B25	
1	IO_L12N_1	B26	
1	IO_L16P_1	E25	
1	IO_L16N_1	E26	
1	IO_L17P_1	D24	
1	IO_L17N_1	D26	
1	IO_L18P_1	F24	
1	IO_L18N_1	F26	
1	IO_L19P_1	H24	
1	IO_L19N_1	H26	
1	IO_L20P_1	G25	
1	IO_L20N_1	G26	
1	IO_L21P_1	K24	
1	IO_L21N_1	K26	
1	IO_L22P_1	J25	
1	IO_L22N_1	J26	
1	IO_L23P_1	M24	
1	IO_L23N_1	M26	
1	IO_L24P_1	L25	
1	IO_L24N_1	L26	
1	IO_L25P_1	N25	
1	IO_L25N_1	N26	
1	IO_L28P_1	L19	
1	IO_L28N_VREF_1	K19	
1	IO_L29P_A23_M1A13_1	L23	
1	IO_L29N_A22_M1A14_1	L24	
1	IO_L30P_A21_M1RESET_1	P20	
1	IO_L30N_A20_M1A11_1	N21	
1	IO_L31P_A19_M1CKE_1	M23	
1	IO_L31N_A18_M1A12_1	N24	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L32P_A17_M1A8_1	L17	
1	IO_L32N_A16_M1A9_1	K18	
1	IO_L33P_A15_M1A10_1	P24	
1	IO_L33N_A14_M1A4_1	P26	
1	IO_L34P_A13_M1WE_1	M19	
1	IO_L34N_A12_M1BA2_1	L18	
1	IO_L35P_A11_M1A7_1	R25	
1	IO_L35N_A10_M1A2_1	R26	
1	IO_L36P_A9_M1BA0_1	M18	
1	IO_L36N_A8_M1BA1_1	N19	
1	IO_L37P_A7_M1A0_1	N22	
1	IO_L37N_A6_M1A1_1	N23	
1	IO_L38P_A5_M1CLK_1	N17	
1	IO_L38N_A4_M1CLKN_1	N18	
1	IO_L39P_M1A3_1	R23	
1	IO_L39N_M1ODT_1	R24	
1	IO_L40P_GCLK11_M1A5_1	N20	
1	IO_L40N_GCLK10_M1A6_1	M21	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	P21	
1	IO_L41N_GCLK8_M1CASN_1	P22	
1	IO_L42P_GCLK7_M1UDM_1	V23	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	
1	IO_L43P_GCLK5_M1DQ4_1	U25	
1	IO_L43N_GCLK4_M1DQ5_1	U26	
1	IO_L44P_A3_M1DQ6_1	W25	
1	IO_L44N_A2_M1DQ7_1	W26	
1	IO_L45P_A1_M1LDQS_1	V24	
1	IO_L45N_A0_M1LDQSN_1	V26	
1	IO_L46P_FCS_B_M1DQ2_1	T24	
1	IO_L46N_FOE_B_M1DQ3_1	T26	
1	IO_L47P_FWE_B_M1DQ0_1	Y24	
1	IO_L47N_LDC_M1DQ1_1	Y26	
1	IO_L48P_HDC_M1DQ8_1	AD24	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L48N_M1DQ9_1	AD26	
1	IO_L49P_M1DQ10_1	AB24	
1	IO_L49N_M1DQ11_1	AB26	
1	IO_L50P_M1UDQS_1	AC25	
1	IO_L50N_M1UDQSN_1	AC26	
1	IO_L51P_M1DQ12_1	AA25	
1	IO_L51N_M1DQ13_1	AA26	
1	IO_L52P_M1DQ14_1	AE25	
1	IO_L52N_M1DQ15_1	AE26	
1	IO_L53P_1	T23	
1	IO_L53N_VREF_1	U24	
1	IO_L57P_1	R20	
1	IO_L57N_1	R19	
1	IO_L59P_1	T22	
1	IO_L59N_1	U23	
1	IO_L60P_1	T18	
1	IO_L60N_1	T19	
1	IO_L61P_1	U21	
1	IO_L61N_1	U22	
1	IO_L63P_1	AA23	
1	IO_L63N_1	AA24	
1	IO_L64P_1	T20	
1	IO_L64N_1	U20	
1	IO_L65P_1	AC23	
1	IO_L65N_1	AC24	
1	IO_L66P_1	V18	
1	IO_L66N_1	V19	
1	IO_L67P_1	AE24	
1	IO_L67N_1	AF25	
1	IO_L68P_1	W18	
1	IO_L68N_1	W19	
1	IO_L62P_1	U17	
1	IO_L62N_1	V17	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L70P_1	U19	
1	IO_L70N_1	V20	
1	IO_L71P_1	V22	
1	IO_L71N_1	W22	
1	IO_L72P_1	Y20	
1	IO_L72N_1	Y21	
1	IO_L73P_1	Y22	
1	IO_L73N_1	AA22	
1	IO_L74P_AWAKE_1	AE23	
1	IO_L74N_DOUT_BUSY_1	AF24	
NA	SUSPEND	AD23	
2	CMPCS_B_2	AC22	
2	DONE_2	AF23	
2	IO_L1P_CCLK_2	AD22	
2	IO_L1N_M0_CMPMISO_2	AF22	
2	IO_L2P_CMPCLK_2	AE21	
2	IO_L2N_CMPMOSI_2	AF21	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD20	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF20	
2	IO_L4P_2	AE19	
2	IO_L4N_VREF_2	AF19	
2	IO_L5P_2	AC20	
2	IO_L5N_2	AD21	
2	IO_L6P_2	Y18	
2	IO_L6N_2	AA19	
2	IO_L7P_2	AC19	
2	IO_L7N_2	AD19	
2	IO_L8P_2	V16	
2	IO_L8N_2	W17	
2	IO_L9P_2	AD18	
2	IO_L9N_2	AF18	
2	IO_L10P_2	Y16	
2	IO_L10N_2	AA17	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L11P_2	AA18	
2	IO_L11N_2	AB18	
2	IO_L12P_D1_MISO2_2	AE17	
2	IO_L12N_D2_MISO3_2	AF17	
2	IO_L13P_M1_2	AD16	
2	IO_L13N_D10_2	AF16	
2	IO_L14P_D11_2	AE15	
2	IO_L14N_D12_2	AF15	
2	IO_L15P_2	AB17	
2	IO_L15N_2	AC17	
2	IO_L16P_2	AC15	
2	IO_L16N_VREF_2	AD15	
2	IO_L17P_2	AC16	
2	IO_L17N_2	AD17	
2	IO_L18P_2	V15	
2	IO_L18N_2	W16	
2	IO_L19P_2	AB15	
2	IO_L19N_2	AC14	
2	IO_L20P_2	Y15	
2	IO_L20N_2	AA15	
2	IO_L28P_2	Y14	
2	IO_L28N_2	AA14	
2	IO_L29P_GCLK3_2	AD14	
2	IO_L29N_GCLK2_2	AF14	
2	IO_L30P_GCLK1_D13_2	AE13	
2	IO_L30N_GCLK0_USERCCLK_2	AF13	
2	IO_L31P_GCLK31_D14_2	AC13	
2	IO_L31N_GCLK30_D15_2	AD13	
2	IO_L32P_GCLK29_2	AD12	
2	IO_L32N_GCLK28_2	AF12	
2	IO_L34P_2	AA13	
2	IO_L34N_2	AB13	
2	IO_L41P_2	AA12	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L41N_VREF_2	AC12	
2	IO_L42P_2	U15	
2	IO_L42N_2	V14	
2	IO_L43P_2	AA11	
2	IO_L43N_2	AB11	
2	IO_L44P_2	V13	
2	IO_L44N_2	W14	
2	IO_L45P_2	AC11	
2	IO_L45N_2	AD11	
2	IO_L46P_2	V12	
2	IO_L46N_2	W12	
2	IO_L47P_2	AE11	
2	IO_L47N_2	AF11	
2	IO_L48P_D7_2	AE9	
2	IO_L48N_RDWR_B_VREF_2	AF9	
2	IO_L49P_D3_2	AD10	
2	IO_L49N_D4_2	AF10	
2	IO_L50P_2	U13	
2	IO_L50N_2	U12	
2	IO_L51P_2	Y10	
2	IO_L51N_2	AB10	
2	IO_L52P_2	V11	
2	IO_L52N_2	W11	
2	IO_L58P_2	AC9	
2	IO_L58N_2	AD9	
2	IO_L53P_2	AD8	
2	IO_L53N_2	AF8	
2	IO_L62P_D5_2	AE7	
2	IO_L62N_D6_2	AF7	
2	IO_L63P_2	AD6	
2	IO_L63N_2	AF6	
2	IO_L64P_D8_2	AE5	
2	IO_L64N_D9_2	AF5	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L65P_INIT_B_2	AE4	
2	IO_L65N_CSO_B_2	AF4	
2	PROGRAM_B_2	AF3	
3	IO_L1P_3	AC7	
3	IO_L1N_VREF_3	AD7	
3	IO_L2P_3	AE3	
3	IO_L2N_3	AF2	
3	IO_L3P_3	AC4	
3	IO_L3N_3	AD4	
3	IO_L7P_3	AA7	
3	IO_L7N_3	Y6	
3	IO_L8P_3	AB7	
3	IO_L8N_3	AB6	
3	IO_L10P_3	AC5	
3	IO_L10N_3	AD5	
3	IO_L16P_3	AA5	
3	IO_L16N_3	AB5	
3	IO_L15P_3	W8	
3	IO_L15N_3	W7	
3	IO_L18P_3	AB4	
3	IO_L18N_3	AC3	
3	IO_L20P_3	AA4	
3	IO_L20N_3	AA3	
3	IO_L22P_3	W5	
3	IO_L22N_3	Y5	
3	IO_L23P_3	U8	
3	IO_L23N_3	U7	
3	IO_L24P_3	U5	
3	IO_L24N_3	V5	
3	IO_L28P_3	U4	
3	IO_L28N_3	U3	
3	IO_L29P_3	T8	
3	IO_L29N_3	T6	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L30P_3	R5	
3	IO_L30N_3	T4	
3	IO_L31P_3	R7	
3	IO_L31N_VREF_3	R6	
3	IO_L32P_M3DQ14_3	AB3	
3	IO_L32N_M3DQ15_3	AB1	
3	IO_L33P_M3DQ12_3	AD3	
3	IO_L33N_M3DQ13_3	AD1	
3	IO_L34P_M3UDQS_3	AC2	
3	IO_L34N_M3UDQSN_3	AC1	
3	IO_L35P_M3DQ10_3	AE2	
3	IO_L35N_M3DQ11_3	AE1	
3	IO_L36P_M3DQ8_3	AA2	
3	IO_L36N_M3DQ9_3	AA1	
3	IO_L37P_M3DQ0_3	Y3	
3	IO_L37N_M3DQ1_3	Y1	
3	IO_L38P_M3DQ2_3	W2	
3	IO_L38N_M3DQ3_3	W1	
3	IO_L39P_M3LDQS_3	V3	
3	IO_L39N_M3LDQSN_3	V1	
3	IO_L40P_M3DQ6_3	U2	
3	IO_L40N_M3DQ7_3	U1	
3	IO_L41P_GCLK27_M3DQ4_3	T3	
3	IO_L41N_GCLK26_M3DQ5_3	T1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	
3	IO_L42N_GCLK24_M3LDM_3	W3	
3	IO_L43P_GCLK23_M3RASN_3	N8	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P8	
3	IO_L44P_GCLK21_M3A5_3	R2	
3	IO_L44N_GCLK20_M3A6_3	R1	
3	IO_L45P_M3A3_3	P7	
3	IO_L45N_M3ODT_3	P6	
3	IO_L46P_M3CLK_3	R4	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L46N_M3CLKN_3	R3	
3	IO_L47P_M3A0_3	N7	
3	IO_L47N_M3A1_3	N6	
3	IO_L48P_M3BA0_3	P3	
3	IO_L48N_M3BA1_3	P1	
3	IO_L49P_M3A7_3	P10	
3	IO_L49N_M3A2_3	R9	
3	IO_L50P_M3WE_3	P5	
3	IO_L50N_M3BA2_3	N5	
3	IO_L51P_M3A10_3	M10	
3	IO_L51N_M3A4_3	N9	
3	IO_L52P_M3A8_3	N4	
3	IO_L52N_M3A9_3	N3	
3	IO_L53P_M3CKE_3	M9	
3	IO_L53N_M3A12_3	M8	
3	IO_L54P_M3RESET_3	L4	
3	IO_L54N_M3A11_3	L3	
3	IO_L55P_M3A13_3	M6	
3	IO_L55N_M3A14_3	M4	
3	IO_L57P_3	L7	
3	IO_L57N_VREF_3	L6	
3	IO_L59P_3	N2	
3	IO_L59N_3	N1	
3	IO_L60P_3	M3	
3	IO_L60N_3	M1	
3	IO_L61P_3	L2	
3	IO_L61N_3	L1	
3	IO_L62P_3	K3	
3	IO_L62N_3	K1	
3	IO_L63P_3	J2	
3	IO_L63N_3	J1	
3	IO_L64P_3	H3	
3	IO_L64N_3	H1	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L65P_3	G2	
3	IO_L65N_3	G1	
3	IO_L66P_3	F3	
3	IO_L66N_3	F1	
3	IO_L67P_3	E2	
3	IO_L67N_3	E1	
3	IO_L68P_3	D3	
3	IO_L68N_3	D1	
3	IO_L77P_3	E4	
3	IO_L77N_3	E3	
3	IO_L79P_3	C2	
3	IO_L79N_3	C1	
3	IO_L81P_3	B2	
3	IO_L81N_3	B1	
3	IO_L83P_3	C4	
3	IO_L83N_VREF_3	C3	
NA	GND	A1	
NA	GND	A26	
NA	GND	AB12	
NA	GND	AB16	
NA	GND	AB2	
NA	GND	AB20	
NA	GND	AB25	
NA	GND	AC8	
NA	GND	AE10	
NA	GND	AE14	
NA	GND	AE18	
NA	GND	AE22	
NA	GND	AE6	
NA	GND	AF1	
NA	GND	AF26	
NA	GND	B13	
NA	GND	B17	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B21	
NA	GND	B5	
NA	GND	B9	
NA	GND	D4	
NA	GND	E11	
NA	GND	E15	
NA	GND	E22	
NA	GND	E7	
NA	GND	F19	
NA	GND	F2	
NA	GND	F25	
NA	GND	H11	
NA	GND	H23	
NA	GND	H4	
NA	GND	J19	
NA	GND	J8	
NA	GND	K16	
NA	GND	K2	
NA	GND	K25	
NA	GND	L11	
NA	GND	L13	
NA	GND	L15	
NA	GND	M12	
NA	GND	M14	
NA	GND	M16	
NA	GND	M22	
NA	GND	M5	
NA	GND	N11	
NA	GND	N13	
NA	GND	N15	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	P19	
NA	GND	P2	
NA	GND	P25	
NA	GND	R11	
NA	GND	R13	
NA	GND	R15	
NA	GND	R8	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T21	
NA	GND	T5	
NA	GND	U11	
NA	GND	V2	
NA	GND	V25	
NA	GND	W15	
NA	GND	W20	
NA	GND	Y11	
NA	GND	Y23	
NA	GND	Y4	
NA	GND	Y7	
NA	VCCAUX	AA10	
NA	VCCAUX	AA16	
NA	VCCAUX	AA21	
NA	VCCAUX	AA6	
NA	VCCAUX	F21	
NA	VCCAUX	F6	
NA	VCCAUX	G12	
NA	VCCAUX	G15	
NA	VCCAUX	J18	
NA	VCCAUX	J9	
NA	VCCAUX	K13	
NA	VCCAUX	L22	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	L5	
NA	VCCAUX	M17	
NA	VCCAUX	N10	
NA	VCCAUX	U14	
NA	VCCAUX	U6	
NA	VCCAUX	V9	
NA	VCCAUX	Y19	
NA	VCCINT	K11	
NA	VCCINT	K17	
NA	VCCINT	L10	
NA	VCCINT	L12	
NA	VCCINT	L14	
NA	VCCINT	L16	
NA	VCCINT	M11	
NA	VCCINT	M13	
NA	VCCINT	M15	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	N16	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	T11	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T17	
NA	VCCINT	U10	
NA	VCCINT	U16	
0	VCCO_0	B11	
0	VCCO_0	B15	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	VCCO_0	B19	
0	VCCO_0	B3	
0	VCCO_0	B7	
0	VCCO_0	C22	
0	VCCO_0	D17	
0	VCCO_0	D9	
0	VCCO_0	E13	
0	VCCO_0	G10	
0	VCCO_0	G18	
0	VCCO_0	H14	
1	VCCO_1	AB23	
1	VCCO_1	AD25	
1	VCCO_1	M20	
1	VCCO_1	P23	
1	VCCO_1	T25	
1	VCCO_1	U18	
1	VCCO_1	V21	
1	VCCO_1	W23	
1	VCCO_1	Y25	
2	VCCO_2	AB14	
2	VCCO_2	AC10	
2	VCCO_2	AC18	
2	VCCO_2	AC21	
2	VCCO_2	AE12	
2	VCCO_2	AE16	
2	VCCO_2	AE20	
2	VCCO_2	AE8	
2	VCCO_2	Y12	
2	VCCO_2	Y17	
3	VCCO_3	AC6	
3	VCCO_3	AD2	
3	VCCO_3	M7	
3	VCCO_3	P4	

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	VCCO_3	P9	
3	VCCO_3	T2	
3	VCCO_3	T7	
3	VCCO_3	W4	
3	VCCO_3	W6	
3	VCCO_3	Y2	
3	VCCO_3	D2	
3	VCCO_3	F4	
3	VCCO_3	H2	
3	VCCO_3	J6	
3	VCCO_3	K4	
3	VCCO_3	M2	
1	VCCO_1	D25	
1	VCCO_1	F23	
1	VCCO_1	H25	
1	VCCO_1	J21	
1	VCCO_1	K23	
1	VCCO_1	M25	
NC	No Connect	A10	LX45
NC	No Connect	AA20	LX45
NC	No Connect	AA8	LX45
NC	No Connect	AB19	LX45
NC	No Connect	AB8	LX45
NC	No Connect	C10	LX45
NC	No Connect	C12	LX45
NC	No Connect	C16	LX45
NC	No Connect	C24	LX45
NC	No Connect	C8	LX45
NC	No Connect	B10	LX45
NC	No Connect	D10	LX45
NC	No Connect	D11	LX45
NC	No Connect	D12	LX45
NC	No Connect	D13	LX45

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NC	No Connect	D15	LX45
NC	No Connect	D16	LX45
NC	No Connect	D19	LX45
NC	No Connect	D20	LX45
NC	No Connect	D22	LX45
NC	No Connect	D23	LX45
NC	No Connect	D5	LX45
NC	No Connect	D7	LX45
NC	No Connect	D8	LX45
NC	No Connect	E10	LX45
NC	No Connect	E12	LX45
NC	No Connect	E14	LX45
NC	No Connect	E16	LX45
NC	No Connect	E17	LX45
NC	No Connect	E18	LX45
NC	No Connect	E19	LX45
NC	No Connect	E20	LX45
NC	No Connect	E23	LX45
NC	No Connect	E24	LX45
NC	No Connect	E5	LX45
NC	No Connect	E6	LX45
NC	No Connect	E8	LX45
NC	No Connect	E9	LX45
NC	No Connect	F10	LX45
NC	No Connect	F11	LX45
NC	No Connect	F12	LX45
NC	No Connect	F13	LX45
NC	No Connect	F14	LX45
NC	No Connect	F15	LX45
NC	No Connect	F16	LX45
NC	No Connect	F17	LX45
NC	No Connect	F18	LX45
NC	No Connect	F22	LX45

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NC	No Connect	F5	LX45
NC	No Connect	F7	LX45
NC	No Connect	F8	LX45
NC	No Connect	F9	LX45
NC	No Connect	G11	LX45
NC	No Connect	G13	LX45
NC	No Connect	G14	LX45
NC	No Connect	G16	LX45
NC	No Connect	G17	LX45
NC	No Connect	G19	LX45
NC	No Connect	G20	LX45
NC	No Connect	G21	LX45
NC	No Connect	G22	LX45
NC	No Connect	G23	LX45
NC	No Connect	G24	LX45
NC	No Connect	G3	LX45
NC	No Connect	G4	LX45
NC	No Connect	G5	LX45
NC	No Connect	G6	LX45
NC	No Connect	G7	LX45
NC	No Connect	G8	LX45
NC	No Connect	G9	LX45
NC	No Connect	H10	LX45
NC	No Connect	H12	LX45
NC	No Connect	H13	LX45
NC	No Connect	H15	LX45
NC	No Connect	H16	LX45
NC	No Connect	H17	LX45
NC	No Connect	H18	LX45
NC	No Connect	H19	LX45
NC	No Connect	H20	LX45
NC	No Connect	H21	LX45
NC	No Connect	H22	LX45

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NC	No Connect	H5	LX45
NC	No Connect	H6	LX45
NC	No Connect	H7	LX45
NC	No Connect	H8	LX45
NC	No Connect	H9	LX45
NC	No Connect	J10	LX45
NC	No Connect	J11	LX45
NC	No Connect	J12	LX45
NC	No Connect	J13	LX45
NC	No Connect	J14	LX45
NC	No Connect	J15	LX45
NC	No Connect	J16	LX45
NC	No Connect	J17	LX45
NC	No Connect	J20	LX45
NC	No Connect	J22	LX45
NC	No Connect	J23	LX45
NC	No Connect	J24	LX45
NC	No Connect	J5	LX45
NC	No Connect	J7	LX45
NC	No Connect	K10	LX45
NC	No Connect	K12	LX45
NC	No Connect	K14	LX45
NC	No Connect	K15	LX45
NC	No Connect	K20	LX45
NC	No Connect	K21	LX45
NC	No Connect	K22	LX45
NC	No Connect	K5	LX45
NC	No Connect	K6	LX45
NC	No Connect	K7	LX45
NC	No Connect	K8	LX45
NC	No Connect	K9	LX45
NC	No Connect	L20	LX45
NC	No Connect	L21	LX45

Table 2-11: **FG(G)676 Package—LX45 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NC	No Connect	J3	LX45
NC	No Connect	J4	LX45
NC	No Connect	L8	LX45
NC	No Connect	L9	LX45
NC	No Connect	P17	LX45
NC	No Connect	P18	LX45
NC	No Connect	R10	LX45
NC	No Connect	R17	LX45
NC	No Connect	R18	LX45
NC	No Connect	R21	LX45
NC	No Connect	R22	LX45
NC	No Connect	T10	LX45
NC	No Connect	T9	LX45
NC	No Connect	AA9	LX45
NC	No Connect	AB9	LX45
NC	No Connect	U9	LX45
NC	No Connect	V10	LX45
NC	No Connect	W10	LX45
NC	No Connect	W13	LX45
NC	No Connect	W21	LX45
NC	No Connect	W9	LX45
NC	No Connect	Y13	LX45
NC	No Connect	Y8	LX45
NC	No Connect	Y9	LX45
NC	No Connect	V6	LX45
NC	No Connect	V7	LX45
NC	No Connect	V8	LX45
NC	No Connect	AB21	LX45
NC	No Connect	AB22	LX45

FG(G)676 Package—LX75, LX100, and LX150

Data on the LX75 is not currently available.

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	
0	IO_L1N_VREF_0	A2	
0	IO_L2P_0	B4	
0	IO_L2N_0	A4	
0	IO_L3P_0	E6	
0	IO_L3N_0	D5	
0	IO_L4P_0	C5	
0	IO_L4N_0	A5	
0	IO_L5P_0	G8	
0	IO_L5N_0	F7	
0	IO_L6P_0	B6	
0	IO_L6N_0	A6	
0	IO_L7P_0	G9	LX100
0	IO_L7N_0	F8	LX100
0	IO_L8P_0	D6	
0	IO_L8N_VREF_0	C6	
0	IO_L9P_0	K12	LX100
0	IO_L9N_0	J11	LX100
0	IO_L11P_0	H10	LX100
0	IO_L11N_0	H9	LX100
0	IO_L12P_0	C7	
0	IO_L12N_0	A7	
0	IO_L13P_0	E8	
0	IO_L13N_0	D7	
0	IO_L14P_0	D8	
0	IO_L14N_0	C8	
0	IO_L15P_0	F9	
0	IO_L15N_0	E9	
0	IO_L16P_0	B8	
0	IO_L16N_0	A8	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L17P_0	C9	
0	IO_L17N_0	A9	
0	IO_L18P_0	E10	
0	IO_L18N_0	F10	
0	IO_L19P_0	D10	
0	IO_L19N_0	C10	
0	IO_L21P_0	J12	LX100
0	IO_L21N_0	H13	LX100
0	IO_L22P_0	B10	
0	IO_L22N_0	A10	
0	IO_L23P_0	D11	
0	IO_L23N_0	F11	
0	IO_L24P_0	C11	
0	IO_L24N_0	A11	
0	IO_L25P_0	H12	LX100
0	IO_L25N_0	G11	LX100
0	IO_L26P_0	B12	
0	IO_L26N_0	A12	
0	IO_L30P_0	F12	LX100
0	IO_L30N_0	E12	LX100
0	IO_L31P_0	D12	
0	IO_L31N_0	C12	
0	IO_L32P_0	G13	LX100
0	IO_L32N_0	F14	LX100
0	IO_L33P_0	F13	
0	IO_L33N_0	D13	
0	IO_L34P_GCLK19_0	C13	
0	IO_L34N_GCLK18_0	A13	
0	IO_L35P_GCLK17_0	B14	
0	IO_L35N_GCLK16_0	A14	
0	IO_L36P_GCLK15_0	D14	
0	IO_L36N_GCLK14_0	C14	
0	IO_L37P_GCLK13_0	C15	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L37N_GCLK12_0	A15	
0	IO_L38P_0	B16	
0	IO_L38N_VREF_0	A16	
0	IO_L43P_0	J14	
0	IO_L43N_0	G14	
0	IO_L44P_0	E14	
0	IO_L44N_0	D15	
0	IO_L45P_0	J13	LX100
0	IO_L45N_0	K14	LX100
0	IO_L46P_0	D16	
0	IO_L46N_0	C16	
0	IO_L47P_0	G16	
0	IO_L47N_0	F15	
0	IO_L48P_0	F17	
0	IO_L48N_0	E17	
0	IO_L49P_0	F16	
0	IO_L49N_0	E16	
0	IO_L50P_0	C17	
0	IO_L50N_0	A17	
0	IO_L51P_0	J15	
0	IO_L51N_0	H15	
0	IO_L52P_0	D18	
0	IO_L52N_0	C18	
0	IO_L53P_0	K15	LX100
0	IO_L53N_0	J16	LX100
0	IO_L54P_0	E19	
0	IO_L54N_0	D19	
0	IO_L55P_0	H16	
0	IO_L55N_0	G17	
0	IO_L56P_0	D21	
0	IO_L56N_0	C20	
0	IO_L57P_0	F18	
0	IO_L57N_0	E18	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L58P_0	E20	
0	IO_L58N_0	D20	
0	IO_L59P_0	J17	
0	IO_L59N_0	H17	
0	IO_L62P_0	B18	
0	IO_L62N_VREF_0	A18	
0	IO_L63P_SCP7_0	C19	
0	IO_L63N_SCP6_0	A19	
0	IO_L64P_SCP5_0	B20	
0	IO_L64N_SCP4_0	A20	
0	IO_L65P_SCP3_0	C21	
0	IO_L65N_SCP2_0	A21	
0	IO_L66P_SCP1_0	B22	
0	IO_L66N_SCP0_0	A22	
NA	TCK	E21	
NA	TDI	F20	
NA	TMS	C23	
NA	TDO	A24	
5	IO_L1P_A25_5	B23	
5	IO_L1N_A24_VREF_5	A23	
5	IO_L2P_M5A13_5	G20	
5	IO_L2N_M5A14_5	G21	
5	IO_L3P_M5RESET_5	D23	
5	IO_L3N_M5A11_5	C24	
5	IO_L4P_M5CKE_5	F22	
5	IO_L4N_M5A12_5	D22	
5	IO_L5P_M5A8_5	H20	
5	IO_L5N_M5A9_5	H21	
5	IO_L6P_M5A10_5	H22	
5	IO_L6N_M5A4_5	G22	
5	IO_L7P_M5WE_5	E23	
5	IO_L7N_M5BA2_5	E24	
5	IO_L8P_M5A7_5	G23	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L8N_M5A2_5	G24	
5	IO_L9P_M5BA0_5	H18	
5	IO_L9N_M5BA1_5	G19	
5	IO_L10P_M5A0_5	B24	
5	IO_L10N_M5A1_5	A25	
5	IO_L11P_M5CLK_5	C25	
5	IO_L11N_M5CLKN_5	C26	
5	IO_L12P_M5A3_5	B25	
5	IO_L12N_M5ODT_5	B26	
5	IO_L13P_M5A5_5	K20	
5	IO_L13N_M5A6_5	K21	
5	IO_L14P_M5RASN_5	K22	
5	IO_L14N_M5CASN_5	J22	
5	IO_L15P_M5UDM_5	J23	
5	IO_L15N_M5LDM_5	J24	
5	IO_L16P_M5DQ4_5	E25	
5	IO_L16N_M5DQ5_5	E26	
5	IO_L17P_M5DQ6_5	D24	
5	IO_L17N_M5DQ7_5	D26	
5	IO_L18P_M5LDQS_5	F24	
5	IO_L18N_M5LDQSN_5	F26	
5	IO_L19P_M5DQ2_5	H24	
5	IO_L19N_M5DQ3_5	H26	
5	IO_L20P_M5DQ0_5	G25	
5	IO_L20N_M5DQ1_5	G26	
5	IO_L21P_M5DQ8_5	K24	
5	IO_L21N_M5DQ9_5	K26	
5	IO_L22P_M5DQ10_5	J25	
5	IO_L22N_M5DQ11_5	J26	
5	IO_L23P_M5UDQS_5	M24	
5	IO_L23N_M5UDQSN_5	M26	
5	IO_L24P_M5DQ12_5	L25	
5	IO_L24N_M5DQ13_5	L26	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L25P_M5DQ14_5	N25	
5	IO_L25N_M5DQ15_5	N26	
5	IO_L26P_5	L20	
5	IO_L26N_VREF_5	L21	
5	IO_L27P_5	H19	
5	IO_L27N_5	J20	
1	IO_L28P_1	L19	
1	IO_L28N_VREF_1	K19	
1	IO_L29P_A23_M1A13_1	L23	
1	IO_L29N_A22_M1A14_1	L24	
1	IO_L30P_A21_M1RESET_1	P20	
1	IO_L30N_A20_M1A11_1	N21	
1	IO_L31P_A19_M1CKE_1	M23	
1	IO_L31N_A18_M1A12_1	N24	
1	IO_L32P_A17_M1A8_1	L17	
1	IO_L32N_A16_M1A9_1	K18	
1	IO_L33P_A15_M1A10_1	P24	
1	IO_L33N_A14_M1A4_1	P26	
1	IO_L34P_A13_M1WE_1	M19	
1	IO_L34N_A12_M1BA2_1	L18	
1	IO_L35P_A11_M1A7_1	R25	
1	IO_L35N_A10_M1A2_1	R26	
1	IO_L36P_A9_M1BA0_1	M18	
1	IO_L36N_A8_M1BA1_1	N19	
1	IO_L37P_A7_M1A0_1	N22	
1	IO_L37N_A6_M1A1_1	N23	
1	IO_L38P_A5_M1CLK_1	N17	
1	IO_L38N_A4_M1CLKN_1	N18	
1	IO_L39P_M1A3_1	R23	
1	IO_L39N_M1ODT_1	R24	
1	IO_L40P_GCLK11_M1A5_1	N20	
1	IO_L40N_GCLK10_M1A6_1	M21	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	P21	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L41N_GCLK8_M1CASN_1	P22	
1	IO_L42P_GCLK7_M1UDM_1	V23	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	
1	IO_L43P_GCLK5_M1DQ4_1	U25	
1	IO_L43N_GCLK4_M1DQ5_1	U26	
1	IO_L44P_A3_M1DQ6_1	W25	
1	IO_L44N_A2_M1DQ7_1	W26	
1	IO_L45P_A1_M1LDQS_1	V24	
1	IO_L45N_A0_M1LDQSN_1	V26	
1	IO_L46P_FCS_B_M1DQ2_1	T24	
1	IO_L46N_FOE_B_M1DQ3_1	T26	
1	IO_L47P_FWE_B_M1DQ0_1	Y24	
1	IO_L47N_LDC_M1DQ1_1	Y26	
1	IO_L48P_HDC_M1DQ8_1	AD24	
1	IO_L48N_M1DQ9_1	AD26	
1	IO_L49P_M1DQ10_1	AB24	
1	IO_L49N_M1DQ11_1	AB26	
1	IO_L50P_M1UDQS_1	AC25	
1	IO_L50N_M1UDQSN_1	AC26	
1	IO_L51P_M1DQ12_1	AA25	
1	IO_L51N_M1DQ13_1	AA26	
1	IO_L52P_M1DQ14_1	AE25	
1	IO_L52N_M1DQ15_1	AE26	
1	IO_L53P_1	T23	
1	IO_L53N_VREF_1	U24	
1	IO_L55P_1	R22	
1	IO_L55N_1	R21	
1	IO_L56P_1	P17	
1	IO_L56N_1	P18	
1	IO_L57P_1	R20	
1	IO_L57N_1	R19	
1	IO_L58P_1	R17	
1	IO_L58N_1	R18	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L59P_1	T22	
1	IO_L59N_1	U23	
1	IO_L60P_1	T18	
1	IO_L60N_1	T19	
1	IO_L61P_1	U21	
1	IO_L61N_1	U22	
1	IO_L62P_1	U17	
1	IO_L62N_1	V17	
1	IO_L63P_1	AA23	
1	IO_L63N_1	AA24	
1	IO_L64P_1	T20	
1	IO_L64N_1	U20	
1	IO_L65P_1	AC23	
1	IO_L65N_1	AC24	
1	IO_L66P_1	V18	
1	IO_L66N_1	V19	
1	IO_L67P_1	AE24	
1	IO_L67N_1	AF25	
1	IO_L68P_1	W18	
1	IO_L68N_1	W19	
1	IO_L69P_1	AB21	
1	IO_L69N_VREF_1	AB22	
1	IO_L70P_1	U19	
1	IO_L70N_1	V20	
1	IO_L71P_1	V22	
1	IO_L71N_1	W22	
1	IO_L72P_1	Y20	
1	IO_L72N_1	Y21	
1	IO_L73P_1	Y22	
1	IO_L73N_1	AA22	
1	IO_L74P_AWAKE_1	AE23	
1	IO_L74N_DOUT_BUSY_1	AF24	
NA	VFS	AB19	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	RFUSE	AA20	
NA	VBATT	W21	
NA	SUSPEND	AD23	
2	CMPCS_B_2	AC22	
2	DONE_2	AF23	
2	IO_L1P_CCLK_2	AD22	
2	IO_L1N_M0_CMPMISO_2	AF22	
2	IO_L2P_CMPCLK_2	AE21	
2	IO_L2N_CMPMOSI_2	AF21	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD20	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF20	
2	IO_L4P_2	AE19	
2	IO_L4N_VREF_2	AF19	
2	IO_L5P_2	AC20	
2	IO_L5N_2	AD21	
2	IO_L6P_2	Y18	
2	IO_L6N_2	AA19	
2	IO_L7P_2	AC19	
2	IO_L7N_2	AD19	
2	IO_L8P_2	V16	
2	IO_L8N_2	W17	
2	IO_L9P_2	AD18	
2	IO_L9N_2	AF18	
2	IO_L10P_2	Y16	
2	IO_L10N_2	AA17	
2	IO_L11P_2	AA18	
2	IO_L11N_2	AB18	
2	IO_L12P_D1_MISO2_2	AE17	
2	IO_L12N_D2_MISO3_2	AF17	
2	IO_L13P_M1_2	AD16	
2	IO_L13N_D10_2	AF16	
2	IO_L14P_D11_2	AE15	
2	IO_L14N_D12_2	AF15	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L15P_2	AB17	
2	IO_L15N_2	AC17	
2	IO_L16P_2	AC15	
2	IO_L16N_VREF_2	AD15	
2	IO_L17P_2	AC16	
2	IO_L17N_2	AD17	
2	IO_L18P_2	V15	
2	IO_L18N_2	W16	
2	IO_L19P_2	AB15	
2	IO_L19N_2	AC14	
2	IO_L20P_2	Y15	
2	IO_L20N_2	AA15	
2	IO_L28P_2	Y14	
2	IO_L28N_2	AA14	
2	IO_L29P_GCLK3_2	AD14	
2	IO_L29N_GCLK2_2	AF14	
2	IO_L30P_GCLK1_D13_2	AE13	
2	IO_L30N_GCLK0_USERCCLK_2	AF13	
2	IO_L31P_GCLK31_D14_2	AC13	
2	IO_L31N_GCLK30_D15_2	AD13	
2	IO_L32P_GCLK29_2	AD12	
2	IO_L32N_GCLK28_2	AF12	
2	IO_L33P_2	W13	
2	IO_L33N_2	Y13	
2	IO_L34P_2	AA13	
2	IO_L34N_2	AB13	
2	IO_L41P_2	AA12	
2	IO_L41N_VREF_2	AC12	
2	IO_L42P_2	U15	
2	IO_L42N_2	V14	
2	IO_L43P_2	AA11	
2	IO_L43N_2	AB11	
2	IO_L44P_2	V13	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L44N_2	W14	
2	IO_L45P_2	AC11	
2	IO_L45N_2	AD11	
2	IO_L46P_2	V12	
2	IO_L46N_2	W12	
2	IO_L47P_2	AE11	
2	IO_L47N_2	AF11	
2	IO_L48P_D7_2	AE9	
2	IO_L48N_RDWR_B_VREF_2	AF9	
2	IO_L49P_D3_2	AD10	
2	IO_L49N_D4_2	AF10	
2	IO_L50P_2	U13	
2	IO_L50N_2	U12	
2	IO_L51P_2	Y10	
2	IO_L51N_2	AB10	
2	IO_L52P_2	V11	
2	IO_L52N_2	W11	
2	IO_L53P_2	AD8	
2	IO_L53N_2	AF8	
2	IO_L58P_2	AC9	
2	IO_L58N_2	AD9	
2	IO_L61P_2	AA9	
2	IO_L61N_VREF_2	AB9	
2	IO_L62P_D5_2	AE7	
2	IO_L62N_D6_2	AF7	
2	IO_L63P_2	AD6	
2	IO_L63N_2	AF6	
2	IO_L64P_D8_2	AE5	
2	IO_L64N_D9_2	AF5	
2	IO_L65P_INIT_B_2	AE4	
2	IO_L65N_CSO_B_2	AF4	
2	PROGRAM_B_2	AF3	
3	IO_L1P_3	AC7	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L1N_VREF_3	AD7	
3	IO_L2P_3	AE3	
3	IO_L2N_3	AF2	
3	IO_L3P_3	AC4	
3	IO_L3N_3	AD4	
3	IO_L4P_3	AA8	
3	IO_L4N_3	AB8	
3	IO_L7P_3	AA7	
3	IO_L7N_3	Y6	
3	IO_L8P_3	AB7	
3	IO_L8N_3	AB6	
3	IO_L9P_3	Y9	
3	IO_L9N_3	Y8	
3	IO_L10P_3	AC5	
3	IO_L10N_3	AD5	
3	IO_L15P_3	W8	
3	IO_L15N_3	W7	
3	IO_L16P_3	AA5	
3	IO_L16N_3	AB5	
3	IO_L17P_3	V7	
3	IO_L17N_VREF_3	V6	
3	IO_L18P_3	AB4	
3	IO_L18N_3	AC3	
3	IO_L19P_3	W9	
3	IO_L19N_3	V8	
3	IO_L20P_3	AA4	
3	IO_L20N_3	AA3	
3	IO_L21P_3	W10	
3	IO_L21N_3	V10	
3	IO_L22P_3	W5	
3	IO_L22N_3	Y5	
3	IO_L23P_3	U8	
3	IO_L23N_3	U7	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L24P_3	U5	
3	IO_L24N_3	V5	
3	IO_L25P_3	T10	
3	IO_L25N_3	U9	
3	IO_L27P_3	R10	
3	IO_L27N_3	T9	
3	IO_L28P_3	U4	
3	IO_L28N_3	U3	
3	IO_L29P_3	T8	
3	IO_L29N_3	T6	
3	IO_L30P_3	R5	
3	IO_L30N_3	T4	
3	IO_L31P_3	R7	
3	IO_L31N_VREF_3	R6	
3	IO_L32P_M3DQ14_3	AB3	
3	IO_L32N_M3DQ15_3	AB1	
3	IO_L33P_M3DQ12_3	AD3	
3	IO_L33N_M3DQ13_3	AD1	
3	IO_L34P_M3UDQS_3	AC2	
3	IO_L34N_M3UDQSN_3	AC1	
3	IO_L35P_M3DQ10_3	AE2	
3	IO_L35N_M3DQ11_3	AE1	
3	IO_L36P_M3DQ8_3	AA2	
3	IO_L36N_M3DQ9_3	AA1	
3	IO_L37P_M3DQ0_3	Y3	
3	IO_L37N_M3DQ1_3	Y1	
3	IO_L38P_M3DQ2_3	W2	
3	IO_L38N_M3DQ3_3	W1	
3	IO_L39P_M3LDQS_3	V3	
3	IO_L39N_M3LDQSN_3	V1	
3	IO_L40P_M3DQ6_3	U2	
3	IO_L40N_M3DQ7_3	U1	
3	IO_L41P_GCLK27_M3DQ4_3	T3	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L41N_GCLK26_M3DQ5_3	T1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	
3	IO_L42N_GCLK24_M3LDM_3	W3	
3	IO_L43P_GCLK23_M3RASN_3	N8	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P8	
3	IO_L44P_GCLK21_M3A5_3	R2	
3	IO_L44N_GCLK20_M3A6_3	R1	
3	IO_L45P_M3A3_3	P7	
3	IO_L45N_M3ODT_3	P6	
3	IO_L46P_M3CLK_3	R4	
3	IO_L46N_M3CLKN_3	R3	
3	IO_L47P_M3A0_3	N7	
3	IO_L47N_M3A1_3	N6	
3	IO_L48P_M3BA0_3	P3	
3	IO_L48N_M3BA1_3	P1	
3	IO_L49P_M3A7_3	P10	
3	IO_L49N_M3A2_3	R9	
3	IO_L50P_M3WE_3	P5	
3	IO_L50N_M3BA2_3	N5	
3	IO_L51P_M3A10_3	M10	
3	IO_L51N_M3A4_3	N9	
3	IO_L52P_M3A8_3	N4	
3	IO_L52N_M3A9_3	N3	
3	IO_L53P_M3CKE_3	M9	
3	IO_L53N_M3A12_3	M8	
3	IO_L54P_M3RESET_3	L4	
3	IO_L54N_M3A11_3	L3	
3	IO_L55P_M3A13_3	M6	
3	IO_L55N_M3A14_3	M4	
3	IO_L57P_3	L7	
3	IO_L57N_VREF_3	L6	
4	IO_L58P_4	K8	
4	IO_L58N_VREF_4	L8	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L59P_M4DQ14_4	N2	
4	IO_L59N_M4DQ15_4	N1	
4	IO_L60P_M4DQ12_4	M3	
4	IO_L60N_M4DQ13_4	M1	
4	IO_L61P_M4UDQS_4	L2	
4	IO_L61N_M4UDQSN_4	L1	
4	IO_L62P_M4DQ10_4	K3	
4	IO_L62N_M4DQ11_4	K1	
4	IO_L63P_M4DQ8_4	J2	
4	IO_L63N_M4DQ9_4	J1	
4	IO_L64P_M4DQ0_4	H3	
4	IO_L64N_M4DQ1_4	H1	
4	IO_L65P_M4DQ2_4	G2	
4	IO_L65N_M4DQ3_4	G1	
4	IO_L66P_M4LDQS_4	F3	
4	IO_L66N_M4LDQSN_4	F1	
4	IO_L67P_M4DQ6_4	E2	
4	IO_L67N_M4DQ7_4	E1	
4	IO_L68P_M4DQ4_4	D3	
4	IO_L68N_M4DQ5_4	D1	
4	IO_L69P_M4UDM_4	J4	
4	IO_L69N_M4LDM_4	J3	
4	IO_L70P_M4RASN_4	K7	
4	IO_L70N_M4CASN_4	K6	
4	IO_L71P_M4A5_4	K5	
4	IO_L71N_M4A6_4	J5	
4	IO_L72P_M4A3_4	J7	
4	IO_L72N_M4ODT_4	H7	
4	IO_L73P_M4CLK_4	G4	
4	IO_L73N_M4CLKN_4	G3	
4	IO_L74P_M4A0_4	K10	
4	IO_L74N_M4A1_4	L9	
4	IO_L75P_M4BA0_4	H6	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L75N_M4BA1_4	H5	
4	IO_L76P_M4A7_4	J10	
4	IO_L76N_M4A2_4	K9	
4	IO_L77P_M4WE_4	E4	
4	IO_L77N_M4BA2_4	E3	
4	IO_L78P_M4A10_4	G6	
4	IO_L78N_M4A4_4	G5	
4	IO_L79P_M4A8_4	C2	
4	IO_L79N_M4A9_4	C1	
4	IO_L80P_M4CKE_4	F5	
4	IO_L80N_M4A12_4	E5	
4	IO_L81P_M4RESET_4	B2	
4	IO_L81N_M4A11_4	B1	
4	IO_L82P_M4A13_4	H8	
4	IO_L82N_M4A14_4	G7	
4	IO_L83P_4	C4	
4	IO_L83N_VREF_4	C3	
NA	GND	A1	
NA	GND	A26	
NA	GND	AB12	
NA	GND	AB16	
NA	GND	AB2	
NA	GND	AB20	
NA	GND	AB25	
NA	GND	AC8	
NA	GND	AE10	
NA	GND	AE14	
NA	GND	AE18	
NA	GND	AE22	
NA	GND	AE6	
NA	GND	AF1	
NA	GND	AF26	
NA	GND	B13	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B17	
NA	GND	B21	
NA	GND	B5	
NA	GND	B9	
NA	GND	D4	
NA	GND	E11	
NA	GND	E15	
NA	GND	E22	
NA	GND	E7	
NA	GND	F19	
NA	GND	F2	
NA	GND	F25	
NA	GND	H11	
NA	GND	H23	
NA	GND	H4	
NA	GND	J19	
NA	GND	J8	
NA	GND	K16	
NA	GND	K2	
NA	GND	K25	
NA	GND	L11	
NA	GND	L13	
NA	GND	L15	
NA	GND	M12	
NA	GND	M14	
NA	GND	M16	
NA	GND	M22	
NA	GND	M5	
NA	GND	N11	
NA	GND	N13	
NA	GND	N15	
NA	GND	P12	
NA	GND	P14	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	P16	
NA	GND	P19	
NA	GND	P2	
NA	GND	P25	
NA	GND	R11	
NA	GND	R13	
NA	GND	R15	
NA	GND	R8	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T21	
NA	GND	T5	
NA	GND	U11	
NA	GND	V2	
NA	GND	V25	
NA	GND	W15	
NA	GND	W20	
NA	GND	Y11	
NA	GND	Y23	
NA	GND	Y4	
NA	GND	Y7	
NA	VCCAUX	AA10	
NA	VCCAUX	AA16	
NA	VCCAUX	AA21	
NA	VCCAUX	AA6	
NA	VCCAUX	F21	
NA	VCCAUX	F6	
NA	VCCAUX	G12	
NA	VCCAUX	G15	
NA	VCCAUX	J18	
NA	VCCAUX	J9	
NA	VCCAUX	K13	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	L22	
NA	VCCAUX	L5	
NA	VCCAUX	M17	
NA	VCCAUX	N10	
NA	VCCAUX	U14	
NA	VCCAUX	U6	
NA	VCCAUX	V9	
NA	VCCAUX	Y19	
NA	VCCINT	K11	
NA	VCCINT	K17	
NA	VCCINT	L10	
NA	VCCINT	L12	
NA	VCCINT	L14	
NA	VCCINT	L16	
NA	VCCINT	M11	
NA	VCCINT	M13	
NA	VCCINT	M15	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	N16	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	T11	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T17	
NA	VCCINT	U10	
NA	VCCINT	U16	
0	VCCO_0	B11	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	VCCO_0	B15	
0	VCCO_0	B19	
0	VCCO_0	B3	
0	VCCO_0	B7	
0	VCCO_0	C22	
0	VCCO_0	D17	
0	VCCO_0	D9	
0	VCCO_0	E13	
0	VCCO_0	G10	
0	VCCO_0	G18	
0	VCCO_0	H14	
1	VCCO_1	AB23	
1	VCCO_1	AD25	
1	VCCO_1	M20	
1	VCCO_1	P23	
1	VCCO_1	T25	
1	VCCO_1	U18	
1	VCCO_1	V21	
1	VCCO_1	W23	
1	VCCO_1	Y25	
2	VCCO_2	AB14	
2	VCCO_2	AC10	
2	VCCO_2	AC18	
2	VCCO_2	AC21	
2	VCCO_2	AE12	
2	VCCO_2	AE16	
2	VCCO_2	AE20	
2	VCCO_2	AE8	
2	VCCO_2	Y12	
2	VCCO_2	Y17	
3	VCCO_3	AC6	
3	VCCO_3	AD2	
3	VCCO_3	M7	

Table 2-12: **FG(G)676 Package—LX75, LX100, and LX150 *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	VCCO_3	P4	
3	VCCO_3	P9	
3	VCCO_3	T2	
3	VCCO_3	T7	
3	VCCO_3	W4	
3	VCCO_3	W6	
3	VCCO_3	Y2	
4	VCCO_4	D2	
4	VCCO_4	F4	
4	VCCO_4	H2	
4	VCCO_4	J6	
4	VCCO_4	K4	
4	VCCO_4	M2	
5	VCCO_5	D25	
5	VCCO_5	F23	
5	VCCO_5	H25	
5	VCCO_5	J21	
5	VCCO_5	K23	
5	VCCO_5	M25	

FG(G)676 Package—LX75T, LX100T, and LX150T

Data on the LX75T is not currently available.

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L1P_HSWAPEN_0	H7	
0	IO_L1N_VREF_0	G7	
0	IO_L2P_0	H8	
0	IO_L2N_0	G8	
0	IO_L3P_0	F7	
0	IO_L3N_0	F6	
0	IO_L4P_0	C3	
0	IO_L4N_0	B3	
0	IO_L5P_0	G6	
0	IO_L5N_0	F5	
0	IO_L8P_0	E6	
0	IO_L8N_VREF_0	E5	
0	IO_L13P_0	H9	
0	IO_L13N_0	G9	
0	IO_L14P_0	A3	
0	IO_L14N_0	A2	
0	IO_L15P_0	F9	
0	IO_L15N_0	E8	
0	IO_L16P_0	D5	
0	IO_L16N_0	C5	
0	IO_L21P_0	H10	
0	IO_L21N_0	G10	
0	IO_L22P_0	B4	
0	IO_L22N_0	A4	
0	IO_L23P_0	F10	
0	IO_L23N_0	E10	
0	IO_L24P_0	B5	
0	IO_L24N_0	A5	
NA	MGTTXN0_101	A6	
NA	MGTTXP0_101	B6	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCCPLL0_101	B11	
NA	MGTREFCLK0N_101	A10	
NA	MGTREFCLK0P_101	B10	
NA	MGTRXN0_101	C7	
NA	MGTRXP0_101	D7	
NA	MGTRREF_101	E9	
NA	MGTRXN1_101	C9	
NA	MGTAVTTRCAL_101	E11	
NA	MGTRXP1_101	D9	
NA	MGTAVCCPLL1_101	C12	
NA	MGTREFCLK1N_101	C11	
NA	MGTREFCLK1P_101	D11	
NA	MGTTXN1_101	A8	
NA	MGTTXP1_101	B8	
0	IO_L30P_0	G12	LX100T
0	IO_L30N_0	F11	LX100T
0	IO_L31P_0	F12	LX100T
0	IO_L31N_0	E12	LX100T
0	IO_L32P_0	J11	
0	IO_L32N_0	G11	
0	IO_L33P_0	H12	
0	IO_L33N_0	G13	
0	IO_L34P_GCLK19_0	E13	
0	IO_L34N_GCLK18_0	D13	
0	IO_L35P_GCLK17_0	C13	
0	IO_L35N_GCLK16_0	A13	
0	IO_L36P_GCLK15_0	B12	
0	IO_L36N_GCLK14_0	A12	
0	IO_L37P_GCLK13_0	B14	
0	IO_L37N_GCLK12_0	A14	
0	IO_L38P_0	K12	
0	IO_L38N_VREF_0	J12	
0	IO_L39P_0	J13	LX100T

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L39N_0	H13	LX100T
0	IO_L40P_0	F14	LX100T
0	IO_L40N_0	E14	LX100T
0	IO_L41P_0	K14	LX100T
0	IO_L41N_0	H14	LX100T
NA	MGTTXN0_123	A18	
NA	MGTTXP0_123	B18	
NA	MGTAVCCPLL0_123	C14	
NA	MGTREFCLK0N_123	C15	
NA	MGTREFCLK0P_123	D15	
NA	MGTRXN0_123	C17	
NA	MGTRXP0_123	D17	
NA	MGTRXN1_123	C19	
NA	MGTRXP1_123	D19	
NA	MGTAVCCPLL1_123	B15	
NA	MGTREFCLK1N_123	A16	
NA	MGTREFCLK1P_123	B16	
NA	MGTTXN1_123	A20	
NA	MGTTXP1_123	B20	
0	IO_L43P_0	J15	
0	IO_L43N_0	H15	
0	IO_L48P_0	J16	
0	IO_L48N_0	J17	
0	IO_L49P_0	F16	
0	IO_L49N_0	E16	
0	IO_L50P_0	G15	
0	IO_L50N_0	F15	
0	IO_L51P_0	F18	
0	IO_L51N_0	E18	
0	IO_L56P_0	G16	
0	IO_L56N_0	F17	
0	IO_L57P_0	F20	
0	IO_L57N_0	E20	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	IO_L58P_0	H17	
0	IO_L58N_0	G17	
0	IO_L59P_0	C21	
0	IO_L59N_0	B21	
0	IO_L62P_0	H18	
0	IO_L62N_VREF_0	H19	
0	IO_L63P_SCP7_0	B22	
0	IO_L63N_SCP6_0	A22	
0	IO_L64P_SCP5_0	G19	
0	IO_L64N_SCP4_0	F19	
0	IO_L65P_SCP3_0	B23	
0	IO_L65N_SCP2_0	A23	
0	IO_L66P_SCP1_0	D21	
0	IO_L66N_SCP0_0	D22	
NA	TCK	A24	
NA	TDI	C23	
NA	TMS	F21	
NA	TDO	G21	
5	IO_L1P_A25_5	H20	
5	IO_L1N_A24_VREF_5	G20	
5	IO_L2P_M5A13_5	B24	
5	IO_L2N_M5A14_5	A25	
5	IO_L3P_M5RESET_5	K18	
5	IO_L3N_M5A11_5	K19	
5	IO_L4P_M5CKE_5	D23	
5	IO_L4N_M5A12_5	C24	
5	IO_L5P_M5A8_5	H21	
5	IO_L5N_M5A9_5	H22	
5	IO_L6P_M5A10_5	F22	
5	IO_L6N_M5A4_5	G23	
5	IO_L7P_M5WE_5	J20	
5	IO_L7N_M5BA2_5	J22	
5	IO_L8P_M5A7_5	E23	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L8N_M5A2_5	E24	
5	IO_L9P_M5BA0_5	L19	
5	IO_L9N_M5BA1_5	K20	
5	IO_L10P_M5A0_5	C25	
5	IO_L10N_M5A1_5	C26	
5	IO_L11P_M5CLK_5	B25	
5	IO_L11N_M5CLKN_5	B26	
5	IO_L12P_M5A3_5	K21	
5	IO_L12N_M5ODT_5	K22	
5	IO_L13P_M5A5_5	M18	
5	IO_L13N_M5A6_5	M19	
5	IO_L14P_M5RASN_5	F23	
5	IO_L14N_M5CASN_5	G24	
5	IO_L15P_M5UDM_5	J23	
5	IO_L15N_M5LDM_5	J24	
5	IO_L16P_M5DQ4_5	E25	
5	IO_L16N_M5DQ5_5	E26	
5	IO_L17P_M5DQ6_5	D24	
5	IO_L17N_M5DQ7_5	D26	
5	IO_L18P_M5LDQS_5	F24	
5	IO_L18N_M5LDQSN_5	F26	
5	IO_L19P_M5DQ2_5	H24	
5	IO_L19N_M5DQ3_5	H26	
5	IO_L20P_M5DQ0_5	G25	
5	IO_L20N_M5DQ1_5	G26	
5	IO_L21P_M5DQ8_5	K24	
5	IO_L21N_M5DQ9_5	K26	
5	IO_L22P_M5DQ10_5	J25	
5	IO_L22N_M5DQ11_5	J26	
5	IO_L23P_M5UDQS_5	M24	
5	IO_L23N_M5UDQSN_5	M26	
5	IO_L24P_M5DQ12_5	L25	
5	IO_L24N_M5DQ13_5	L26	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L25P_M5DQ14_5	N25	
5	IO_L25N_M5DQ15_5	N26	
5	IO_L26P_5	M21	
5	IO_L26N_VREF_5	M23	
5	IO_L27P_5	L20	
5	IO_L27N_5	L21	
1	IO_L28P_1	N17	
1	IO_L28N_VREF_1	N18	
1	IO_L29P_A23_M1A13_1	L23	
1	IO_L29N_A22_M1A14_1	L24	
1	IO_L30P_A21_M1RESET_1	N19	
1	IO_L30N_A20_M1A11_1	N20	
1	IO_L31P_A19_M1CKE_1	N21	
1	IO_L31N_A18_M1A12_1	N22	
1	IO_L32P_A17_M1A8_1	P17	
1	IO_L32N_A16_M1A9_1	P19	
1	IO_L33P_A15_M1A10_1	N23	
1	IO_L33N_A14_M1A4_1	N24	
1	IO_L34P_A13_M1WE_1	R18	
1	IO_L34N_A12_M1BA2_1	R19	
1	IO_L35P_A11_M1A7_1	P21	
1	IO_L35N_A10_M1A2_1	P22	
1	IO_L36P_A9_M1BA0_1	R20	
1	IO_L36N_A8_M1BA1_1	R21	
1	IO_L37P_A7_M1A0_1	P24	
1	IO_L37N_A6_M1A1_1	P26	
1	IO_L38P_A5_M1CLK_1	R23	
1	IO_L38N_A4_M1CLKN_1	R24	
1	IO_L39P_M1A3_1	T22	
1	IO_L39N_M1ODT_1	T23	
1	IO_L40P_GCLK11_M1A5_1	U23	
1	IO_L40N_GCLK10_M1A6_1	U24	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	R25	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L41N_GCLK8_M1CASN_1	R26	
1	IO_L42P_GCLK7_M1UDM_1	V23	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	
1	IO_L43P_GCLK5_M1DQ4_1	U25	
1	IO_L43N_GCLK4_M1DQ5_1	U26	
1	IO_L44P_A3_M1DQ6_1	T24	
1	IO_L44N_A2_M1DQ7_1	T26	
1	IO_L45P_A1_M1LDQS_1	V24	
1	IO_L45N_A0_M1LDQSN_1	V26	
1	IO_L46P_FCS_B_M1DQ2_1	W25	
1	IO_L46N_FOE_B_M1DQ3_1	W26	
1	IO_L47P_FWE_B_M1DQ0_1	AA25	
1	IO_L47N_LDC_M1DQ1_1	AA26	
1	IO_L48P_HDC_M1DQ8_1	AD24	
1	IO_L48N_M1DQ9_1	AD26	
1	IO_L49P_M1DQ10_1	AB24	
1	IO_L49N_M1DQ11_1	AB26	
1	IO_L50P_M1UDQS_1	AC25	
1	IO_L50N_M1UDQSN_1	AC26	
1	IO_L51P_M1DQ12_1	Y24	
1	IO_L51N_M1DQ13_1	Y26	
1	IO_L52P_M1DQ14_1	AE25	
1	IO_L52N_M1DQ15_1	AE26	
1	IO_L53P_1	U21	
1	IO_L53N_VREF_1	U22	
1	IO_L66P_1	T19	
1	IO_L66N_1	T20	
1	IO_L67P_1	AA23	
1	IO_L67N_1	AA24	
1	IO_L68P_1	U19	
1	IO_L68N_1	U20	
1	IO_L69P_1	V20	
1	IO_L69N_VREF_1	V21	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L74P_AWAKE_1	AC23	
1	IO_L74N_DOUT_BUSY_1	AC24	
NA	VFS	W22	
NA	RFUSE	V19	
NA	VBATT	V22	
NA	SUSPEND	Y22	
2	CMPCS_B_2	Y19	
2	DONE_2	AF25	
2	IO_L1P_CCLK_2	AE24	
2	IO_L1N_M0_CMPMISO_2	AF24	
2	IO_L2P_CMPCLK_2	Y21	
2	IO_L2N_CMPMOSI_2	AA22	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD23	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF23	
2	IO_L4P_2	W20	
2	IO_L4N_VREF_2	Y20	
2	IO_L5P_2	AB22	
2	IO_L5N_2	AC22	
2	IO_L12P_D1_MISO2_2	V18	
2	IO_L12N_D2_MISO3_2	W19	
2	IO_L13P_M1_2	AD22	
2	IO_L13N_D10_2	AF22	
2	IO_L14P_D11_2	W17	
2	IO_L14N_D12_2	W18	
2	IO_L15P_2	AA21	
2	IO_L15N_2	AB21	
2	IO_L16P_2	Y17	
2	IO_L16N_VREF_2	AA17	
2	IO_L17P_2	U15	
2	IO_L17N_2	V16	
2	IO_L18P_2	AA19	
2	IO_L18N_2	AB19	
2	IO_L19P_2	W16	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L19N_2	Y16	
2	IO_L20P_2	AA18	
2	IO_L20N_2	AB17	
NA	MGTTXP1_267	AE21	
NA	MGTTXN1_267	AF21	
NA	MGTAVCCPLL1_267	AE16	
NA	MGTREFCLK1P_267	AE17	
NA	MGTREFCLK1N_267	AF17	
NA	MGTRXP1_267	AC20	
NA	MGTRXN1_267	AD20	
NA	MGTRXP0_267	AC18	
NA	MGTRXN0_267	AD18	
NA	MGTAVCCPLL0_267	AD15	
NA	MGTREFCLK0P_267	AC16	
NA	MGTREFCLK0N_267	AD16	
NA	MGTTXP0_267	AE19	
NA	MGTTXN0_267	AF19	
2	IO_L24P_2	Y15	LX100T
2	IO_L24N_VREF_2	AA16	LX100T
2	IO_L26P_2	V14	LX100T
2	IO_L26N_2	V15	LX100T
2	IO_L27P_2	U13	LX100T
2	IO_L27N_2	V13	LX100T
2	IO_L28P_2	AA15	
2	IO_L28N_2	AB15	
2	IO_L29P_GCLK3_2	AE15	
2	IO_L29N_GCLK2_2	AF15	
2	IO_L30P_GCLK1_D13_2	AB14	
2	IO_L30N_GCLK0_USERCCLK_2	AC14	
2	IO_L31P_GCLK31_D14_2	AE13	
2	IO_L31N_GCLK30_D15_2	AF13	
2	IO_L32P_GCLK29_2	AD14	
2	IO_L32N_GCLK28_2	AF14	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L33P_2	Y12	
2	IO_L33N_2	AA12	
2	IO_L34P_2	W14	
2	IO_L34N_2	Y13	
2	IO_L35P_2	V12	LX100T
2	IO_L35N_2	W12	LX100T
2	IO_L36P_2	AB13	LX100T
2	IO_L36N_2	AA13	LX100T
NA	MGTTXP1_245	AE9	
NA	MGTTXN1_245	AF9	
NA	MGTAVCCPLL1_245	AD13	
NA	MGTREFCLK1P_245	AC12	
NA	MGTREFCLK1N_245	AD12	
NA	MGTRXP1_245	AC10	
NA	MGTAVTTRCAL_245	AB12	
NA	MGTRXN1_245	AD10	
NA	MGTRREF_245	AB10	
NA	MGTRXP0_245	AC8	
NA	MGTRXN0_245	AD8	
NA	MGTAVCCPLL0_245	AE12	
NA	MGTREFCLK0P_245	AE11	
NA	MGTREFCLK0N_245	AF11	
NA	MGTTXP0_245	AE7	
NA	MGTTXN0_245	AF7	
2	IO_L41P_2	Y11	
2	IO_L41N_VREF_2	AA11	
2	IO_L46P_2	V11	
2	IO_L46N_2	V10	
2	IO_L47P_2	AA9	
2	IO_L47N_2	AB9	
2	IO_L48P_D7_2	AA10	
2	IO_L48N_RDWR_B_VREF_2	AB11	
2	IO_L49P_D3_2	AD6	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L49N_D4_2	AF6	
2	IO_L50P_2	W10	
2	IO_L50N_2	W9	
2	IO_L51P_2	AE5	
2	IO_L51N_2	AF5	
2	IO_L52P_2	Y9	
2	IO_L52N_2	AA8	
2	IO_L53P_2	AB7	
2	IO_L53N_2	AC6	
2	IO_L61P_2	AC5	
2	IO_L61N_VREF_2	AD5	
2	IO_L62P_D5_2	W8	
2	IO_L62N_D6_2	W7	
2	IO_L63P_2	AD4	
2	IO_L63N_2	AF4	
2	IO_L64P_D8_2	AA7	
2	IO_L64N_D9_2	AA6	
2	IO_L65P_INIT_B_2	AE3	
2	IO_L65N_CSO_B_2	AF3	
2	PROGRAM_B_2	AF2	
3	IO_L1P_3	AB5	
3	IO_L1N_VREF_3	AC4	
3	IO_L2P_3	AA4	
3	IO_L2N_3	AA3	
3	IO_L7P_3	Y6	
3	IO_L7N_3	Y5	
3	IO_L8P_3	AB4	
3	IO_L8N_3	AC3	
3	IO_L9P_3	V7	
3	IO_L9N_3	V6	
3	IO_L10P_3	U4	
3	IO_L10N_3	U3	
3	IO_L17P_3	V5	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L17N_VREF_3	W5	
3	IO_L18P_3	U9	
3	IO_L18N_3	U8	
3	IO_L31P_3	U7	
3	IO_L31N_VREF_3	T6	
3	IO_L32P_M3DQ14_3	AB3	
3	IO_L32N_M3DQ15_3	AB1	
3	IO_L33P_M3DQ12_3	AD3	
3	IO_L33N_M3DQ13_3	AD1	
3	IO_L34P_M3UDQS_3	AC2	
3	IO_L34N_M3UDQSN_3	AC1	
3	IO_L35P_M3DQ10_3	AE2	
3	IO_L35N_M3DQ11_3	AE1	
3	IO_L36P_M3DQ8_3	AA2	
3	IO_L36N_M3DQ9_3	AA1	
3	IO_L37P_M3DQ0_3	Y3	
3	IO_L37N_M3DQ1_3	Y1	
3	IO_L38P_M3DQ2_3	W2	
3	IO_L38N_M3DQ3_3	W1	
3	IO_L39P_M3LDQS_3	V3	
3	IO_L39N_M3LDQSN_3	V1	
3	IO_L40P_M3DQ6_3	U2	
3	IO_L40N_M3DQ7_3	U1	
3	IO_L41P_GCLK27_M3DQ4_3	T3	
3	IO_L41N_GCLK26_M3DQ5_3	T1	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	
3	IO_L42N_GCLK24_M3LDM_3	W3	
3	IO_L43P_GCLK23_M3RASN_3	R7	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	R6	
3	IO_L44P_GCLK21_M3A5_3	R2	
3	IO_L44N_GCLK20_M3A6_3	R1	
3	IO_L45P_M3A3_3	R8	
3	IO_L45N_M3ODT_3	T8	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L46P_M3CLK_3	U5	
3	IO_L46N_M3CLKN_3	T4	
3	IO_L47P_M3A0_3	R10	
3	IO_L47N_M3A1_3	T9	
3	IO_L48P_M3BA0_3	P3	
3	IO_L48N_M3BA1_3	P1	
3	IO_L49P_M3A7_3	N6	
3	IO_L49N_M3A2_3	P6	
3	IO_L50P_M3WE_3	P5	
3	IO_L50N_M3BA2_3	R5	
3	IO_L51P_M3A10_3	N8	
3	IO_L51N_M3A4_3	N7	
3	IO_L52P_M3A8_3	R4	
3	IO_L52N_M3A9_3	R3	
3	IO_L53P_M3CKE_3	R9	
3	IO_L53N_M3A12_3	P8	
3	IO_L54P_M3RESET_3	N5	
3	IO_L54N_M3A11_3	N4	
3	IO_L55P_M3A13_3	P10	
3	IO_L55N_M3A14_3	N9	
3	IO_L57P_3	M10	
3	IO_L57N_VREF_3	M9	
4	IO_L58P_4	M4	
4	IO_L58N_VREF_4	N3	
4	IO_L59P_M4DQ14_4	N2	
4	IO_L59N_M4DQ15_4	N1	
4	IO_L60P_M4DQ12_4	M3	
4	IO_L60N_M4DQ13_4	M1	
4	IO_L61P_M4UDQS_4	L2	
4	IO_L61N_M4UDQSN_4	L1	
4	IO_L62P_M4DQ10_4	K3	
4	IO_L62N_M4DQ11_4	K1	
4	IO_L63P_M4DQ8_4	J2	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L63N_M4DQ9_4	J1	
4	IO_L64P_M4DQ0_4	H3	
4	IO_L64N_M4DQ1_4	H1	
4	IO_L65P_M4DQ2_4	G2	
4	IO_L65N_M4DQ3_4	G1	
4	IO_L66P_M4LDQS_4	F3	
4	IO_L66N_M4LDQSN_4	F1	
4	IO_L67P_M4DQ6_4	E2	
4	IO_L67N_M4DQ7_4	E1	
4	IO_L68P_M4DQ4_4	D3	
4	IO_L68N_M4DQ5_4	D1	
4	IO_L69P_M4UDM_4	J4	
4	IO_L69N_M4LDM_4	J3	
4	IO_L70P_M4RASN_4	L9	
4	IO_L70N_M4CASN_4	L8	
4	IO_L71P_M4A5_4	L4	
4	IO_L71N_M4A6_4	L3	
4	IO_L72P_M4A3_4	M8	
4	IO_L72N_M4ODT_4	M6	
4	IO_L73P_M4CLK_4	K5	
4	IO_L73N_M4CLKN_4	J5	
4	IO_L74P_M4A0_4	L7	
4	IO_L74N_M4A1_4	L6	
4	IO_L75P_M4BA0_4	B2	
4	IO_L75N_M4BA1_4	B1	
4	IO_L76P_M4A7_4	L10	
4	IO_L76N_M4A2_4	K10	
4	IO_L77P_M4WE_4	G4	
4	IO_L77N_M4BA2_4	G3	
4	IO_L78P_M4A10_4	J9	
4	IO_L78N_M4A4_4	J7	
4	IO_L79P_M4A8_4	C2	
4	IO_L79N_M4A9_4	C1	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L80P_M4CKE_4	K9	
4	IO_L80N_M4A12_4	K8	
4	IO_L81P_M4RESET_4	E4	
4	IO_L81N_M4A11_4	E3	
4	IO_L82P_M4A13_4	K7	
4	IO_L82N_M4A14_4	K6	
4	IO_L83P_4	H6	
4	IO_L83N_VREF_4	H5	
NA	GND	A1	
NA	GND	A11	
NA	GND	A15	
NA	GND	A17	
NA	GND	A21	
NA	GND	A26	
NA	GND	A9	
NA	GND	AB16	
NA	GND	AB2	
NA	GND	AB20	
NA	GND	AB25	
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AD19	
NA	GND	AD21	
NA	GND	AD7	
NA	GND	AD9	
NA	GND	AE10	
NA	GND	AE18	
NA	GND	AE20	
NA	GND	AE22	
NA	GND	AE6	
NA	GND	AE8	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AF1	
NA	GND	AF10	
NA	GND	AF12	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF26	
NA	GND	B17	
NA	GND	B19	
NA	GND	B7	
NA	GND	B9	
NA	GND	C18	
NA	GND	C20	
NA	GND	C6	
NA	GND	C8	
NA	GND	D10	
NA	GND	D12	
NA	GND	D14	
NA	GND	D16	
NA	GND	D4	
NA	GND	E15	
NA	GND	E19	
NA	GND	E22	
NA	GND	E7	
NA	GND	F2	
NA	GND	F25	
NA	GND	G14	
NA	GND	H23	
NA	GND	H4	
NA	GND	J19	
NA	GND	J8	
NA	GND	K16	
NA	GND	K2	
NA	GND	K25	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	L11	
NA	GND	L13	
NA	GND	L15	
NA	GND	L17	
NA	GND	M22	
NA	GND	M5	
NA	GND	N11	
NA	GND	N14	
NA	GND	P13	
NA	GND	P16	
NA	GND	P2	
NA	GND	P20	
NA	GND	P25	
NA	GND	P7	
NA	GND	T10	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T18	
NA	GND	T21	
NA	GND	T5	
NA	GND	U11	
NA	GND	U17	
NA	GND	V2	
NA	GND	V25	
NA	GND	V8	
NA	GND	Y10	
NA	GND	Y14	
NA	GND	Y23	
NA	GND	Y4	
NA	GND	Y7	
NA	MGTAVCC_101	C10	
NA	MGTAVCC_123	C16	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_245	AD11	
NA	MGTAVCC_267	AD17	
NA	MGTAVTTRX_101	D8	
NA	MGTAVTTRX_123	D18	
NA	MGTAVTTRX_245	AC9	
NA	MGTAVTTRX_267	AC19	
NA	MGTAVTTTX_101	A7	
NA	MGTAVTTTX_123	A19	
NA	MGTAVTTTX_245	AF8	
NA	MGTAVTTTX_267	AF20	
NA	VCCAUX	AA5	
NA	VCCAUX	AB18	
NA	VCCAUX	AB8	
NA	VCCAUX	AC21	
NA	VCCAUX	AC7	
NA	VCCAUX	D20	
NA	VCCAUX	D6	
NA	VCCAUX	E17	
NA	VCCAUX	G5	
NA	VCCAUX	J10	
NA	VCCAUX	J18	
NA	VCCAUX	K13	
NA	VCCAUX	K15	
NA	VCCAUX	L18	
NA	VCCAUX	L22	
NA	VCCAUX	L5	
NA	VCCAUX	M17	
NA	VCCAUX	N10	
NA	VCCAUX	R22	
NA	VCCAUX	U12	
NA	VCCAUX	U14	
NA	VCCAUX	U18	
NA	VCCAUX	U6	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	V17	
NA	VCCAUX	V9	
NA	VCCAUX	W13	
NA	VCCINT	K11	
NA	VCCINT	K17	
NA	VCCINT	L12	
NA	VCCINT	L14	
NA	VCCINT	L16	
NA	VCCINT	M11	
NA	VCCINT	M12	
NA	VCCINT	M13	
NA	VCCINT	M14	
NA	VCCINT	M15	
NA	VCCINT	M16	
NA	VCCINT	N12	
NA	VCCINT	N13	
NA	VCCINT	N15	
NA	VCCINT	N16	
NA	VCCINT	P11	
NA	VCCINT	P12	
NA	VCCINT	P14	
NA	VCCINT	P15	
NA	VCCINT	R11	
NA	VCCINT	R12	
NA	VCCINT	R13	
NA	VCCINT	R14	
NA	VCCINT	R15	
NA	VCCINT	R16	
NA	VCCINT	R17	
NA	VCCINT	T11	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T17	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	U10	
NA	VCCINT	U16	
0	VCCO_0	B13	
0	VCCO_0	C22	
0	VCCO_0	C4	
0	VCCO_0	E21	
0	VCCO_0	F13	
0	VCCO_0	F8	
0	VCCO_0	G18	
0	VCCO_0	H11	
0	VCCO_0	H16	
0	VCCO_0	J14	
1	VCCO_1	AB23	
1	VCCO_1	AD25	
1	VCCO_1	P18	
1	VCCO_1	P23	
1	VCCO_1	T25	
1	VCCO_1	W21	
1	VCCO_1	W23	
1	VCCO_1	Y25	
2	VCCO_2	AA14	
2	VCCO_2	AA20	
2	VCCO_2	AB6	
2	VCCO_2	AE14	
2	VCCO_2	AE23	
2	VCCO_2	AE4	
2	VCCO_2	W11	
2	VCCO_2	W15	
2	VCCO_2	Y18	
2	VCCO_2	Y8	
3	VCCO_3	AD2	
3	VCCO_3	P4	
3	VCCO_3	P9	

Table 2-13: **FG(G)676 Package—LX75T, LX100T, and LX150T *(Cont'd)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	VCCO_3	T2	
3	VCCO_3	T7	
3	VCCO_3	W4	
3	VCCO_3	W6	
3	VCCO_3	Y2	
4	VCCO_4	D2	
4	VCCO_4	F4	
4	VCCO_4	H2	
4	VCCO_4	J6	
4	VCCO_4	K4	
4	VCCO_4	M2	
4	VCCO_4	M7	
5	VCCO_5	D25	
5	VCCO_5	G22	
5	VCCO_5	H25	
5	VCCO_5	J21	
5	VCCO_5	K23	
5	VCCO_5	M20	
5	VCCO_5	M25	

FG(G)900 Package—LX150

Table 2-14: **FG(G)900 Package—LX150**

Bank	Pin Description	Pin Number	No Connect (NC)
Data is not currently available on devices in this package.			

FG(G)900 Package—LX100T and LX150T

Table 2-15: **FG(G)900 Package—LX100T and LX150T**

Bank	Pin Description	Pin Number	No Connect (NC)
Data is not currently available on devices in this package.			

XILINX®

Chapter 3

Pinout and SelectIO Bank Diagrams

Summary

This chapter provides pinout diagrams for each Spartan-6 FPGA package/device combination.

The multi-function I/O pins in these diagrams are represented by symbols based on functionality, using the following precedence:

- VREF
- GCLK
- D0–D15
- A0–A25

For example, a pin description such as IO_L37N_GCLK12_0 is represented with an N_GCLK symbol, a pin description such as IO_L1N_VREF_0 is represented with a VREF symbol, and a pin description such as IO_L13N_D10_2 is represented with a D0–D15 symbol.

Data on the LX75 is not currently available.

- FG(G)484 Package—LX100, page 171
- FG(G)484 Package—LX150, page 173
- FG(G)484 Package—LX45T, LX75T, LX100T, and LX150T, page 175
  Data on the LX75T is not currently available.
- CSG484 Package—LX45 and LX75, page 176
  Data on devices in this package is not currently available.
- CSG484 Package—LX100, page 176
  Data on devices in this package is not currently available.
- CSG484 Package—LX150, page 176
  Data on devices in this package is not currently available.
- CSG484 Package—LX45T, LX75T, LX100T, and LX150T, page 176
  Data on devices in this package is not currently available.
- FG(G)676 Package—LX45, page 177
- FG(G)676 Package—LX75, page 178
  Data on the LX75 is not currently available.
- FG(G)676 Package—LX75T, page 178
  Data on the LX75T is not currently available.
- FG(G)676 Package—LX100, page 179
- FG(G)676 Package—LX100T, page 181
- FG(G)676 Package—LX150, page 183
- FG(G)676 Package—LX150T, page 185
- FG(G)900 Package—LX100T, page 186
  Data on devices in this package is not currently available.
- FG(G)900 Package—LX150, page 186
  Data on devices in this package is not currently available.
- FG(G)900 Package—LX150T, page 186
  Data on devices in this package is not currently available.

CPG196 Package—LX4, LX9, and LX16

Data on devices listed in this package is not currently available.

Figure 3-1: **CPG196 Package—LX4, LX9, and LX16 Pinout Diagram**

Figure 3-2: **CPG196 Package—LX4, LX9, and LX16 SelectIO Bank Diagram**

TQG144 Package—LX4 and LX9

Data on the LX4 is not currently available.

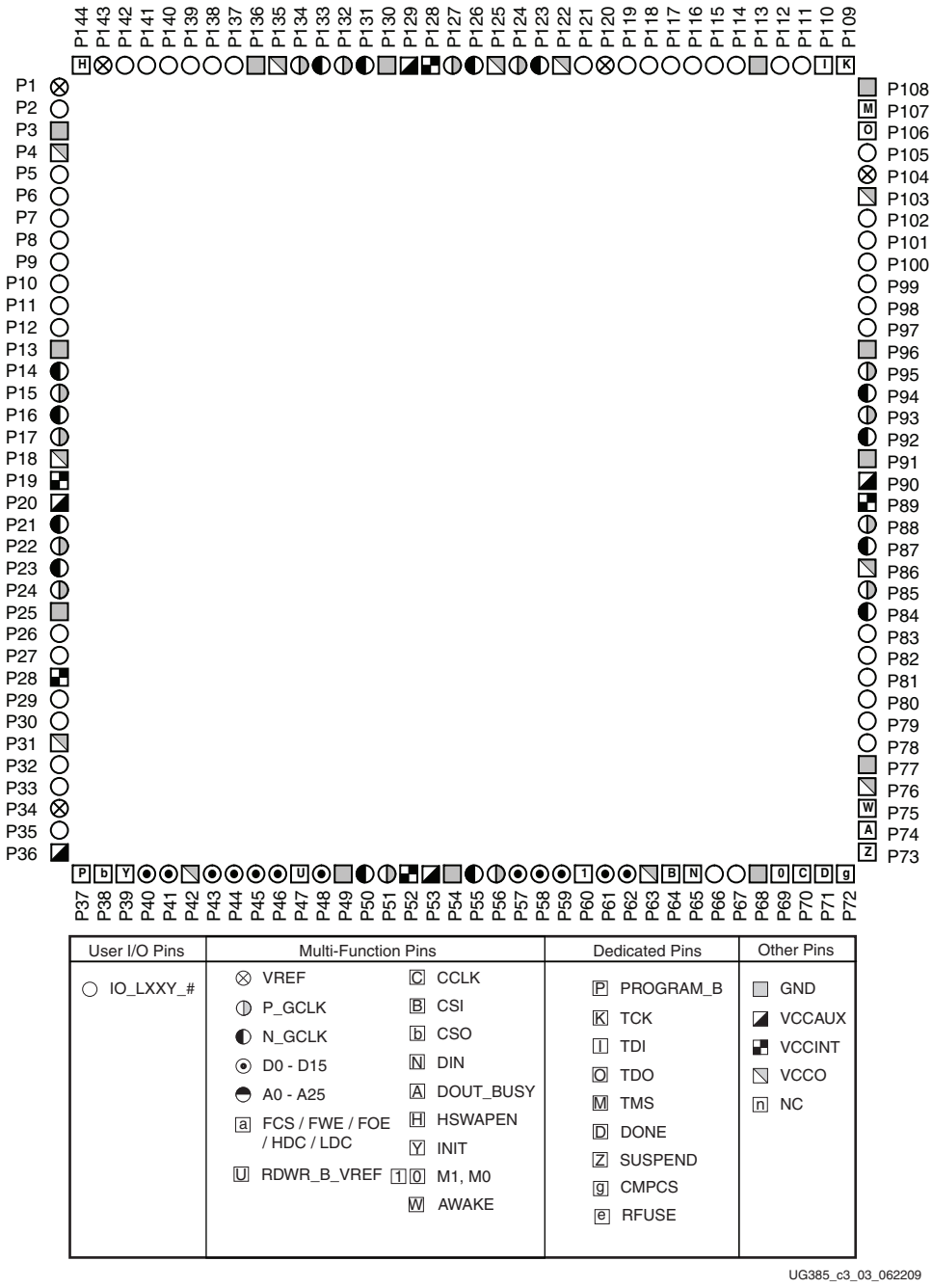


Figure 3-3: **TQG144 Package—LX4 and LX9 Pinout Diagram**

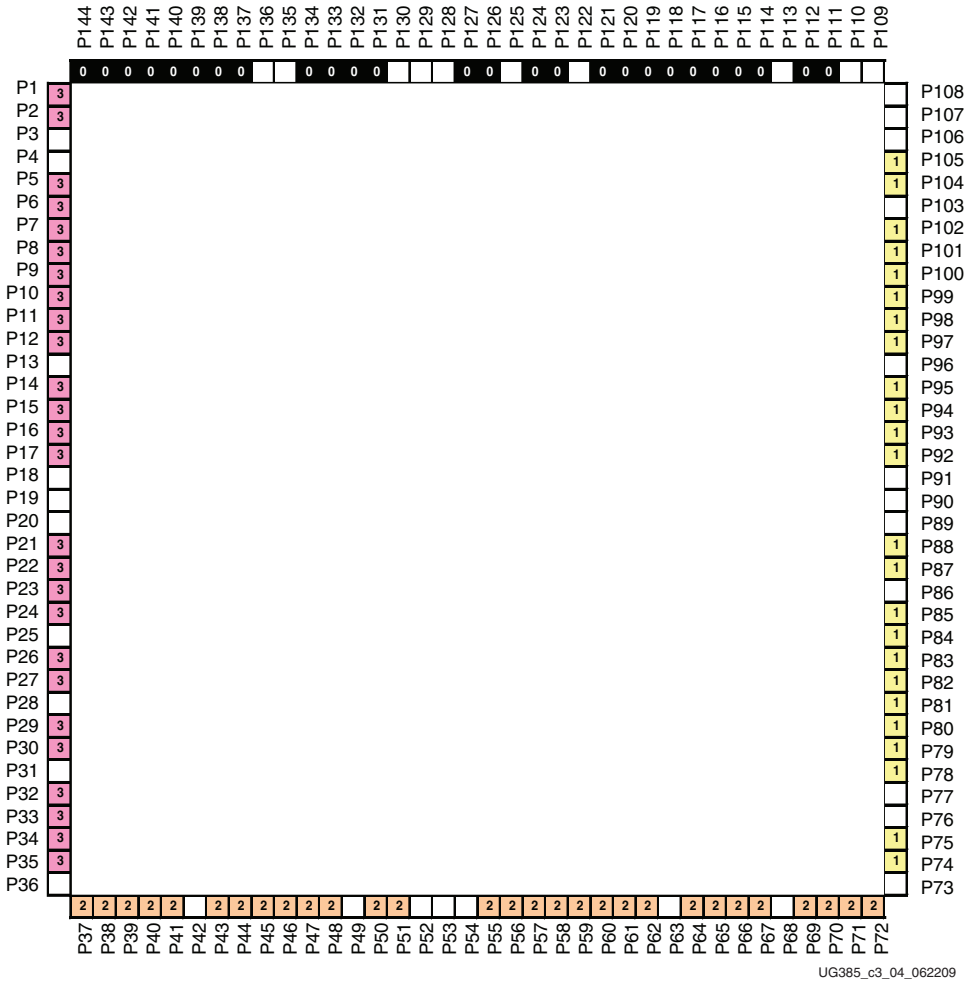


Figure 3-4: **TQG144 Package—LX4 and LX9 SelectIO Bank Diagram**

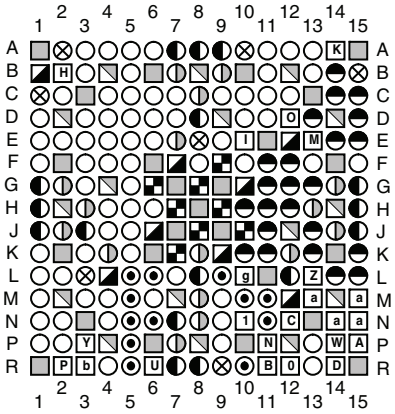
CSG225 Package—LX4

Data on this device in this package is not currently available.

Figure 3-5: **CSG225 Package—LX4 Pinout Diagram**

Figure 3-6: **CSG225 Package—LX4 SelectIO Bank Diagram**

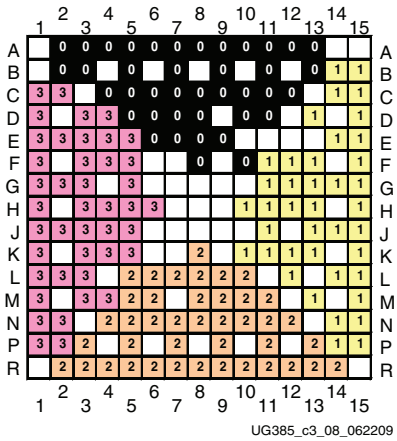
CSG225 Package—LX9 and LX16



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND
	P_GCLK	CSI	TCK	VCCAUX
	N_GCLK	CSO	TDI	VCCINT
	D0 - D15	DIN	TDO	VCCO
	A0 - A25	DOUT_BUSY	TMS	NC
	FCS / FWE / FOE / HDC / LDC	HSWAPEN	DONE	
	RDWR_B_VREF	INIT	SUSPEND	
		M1, M0	CMPCS	
		AWAKE	RFUSE	

UG385_c3_07_062209

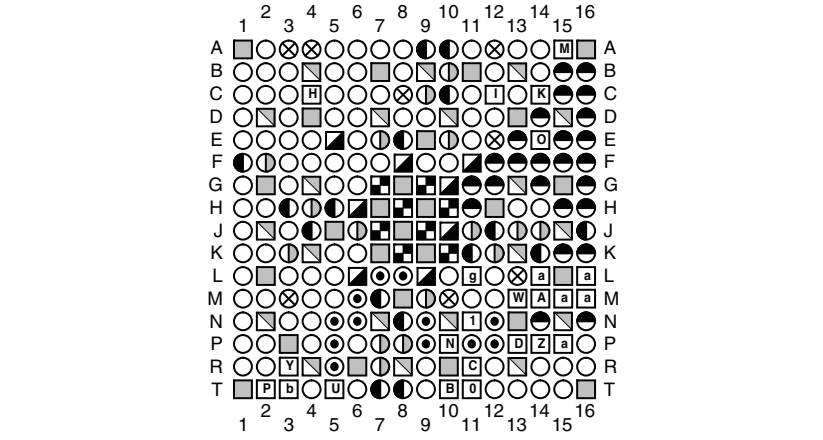
Figure 3-7: **CSG225 Package—LX9 and LX16 Pinout Diagram**



UG385_c3_08_062209

Figure 3-8: **CSG225 Package—LX9 and LX16 SelectIO Bank Diagram**

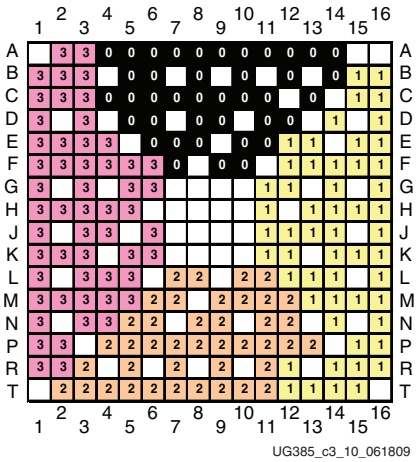
FT(G)256 Package—LX9, LX16, and LX25



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	VCCAUX
	◐ N_GCLK	b CSO	I TDI	VCCINT
	⊙ D0 - D15	N DIN	O TDO	VCCO
	◓ A0 - A25	A DOUT_BUSY	M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	
	U RDWR_B_VREF	Y INIT	Z SUSPEND	
		1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_09_061809

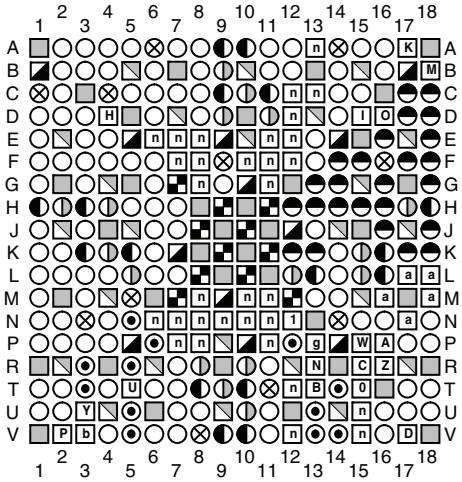
Figure 3-9: **FT(G)256 Package—LX9, LX16, and LX25 Pinout Diagram**



UG385_c3_10_061809

Figure 3-10: **FT(G)256 Package—LX9, LX16, and LX25 SelectIO Bank Diagram**

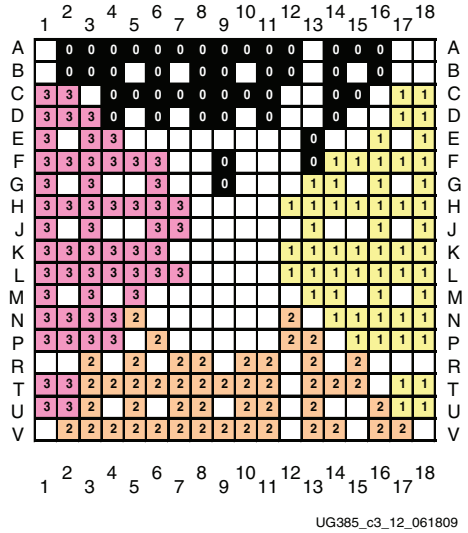
CSG324 Package—LX9



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	◪ VCCAUX
	◐ N_GCLK	b CSO	I TDI	▪ VCCINT
	⊙ D0 - D15	N DIN	O TDO	▧ VCCO
	◓ A0 - A25	A DOUT_BUSY	M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	
		Y INIT	Z SUSPEND	
	U RDWR_B_VREF	1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_11_061809

Figure 3-11: **CSG324 Package—LX9 Pinout Diagram**



UG385_c3_12_061809

Figure 3-12: **CSG324 Package—LX9 SelectIO Bank Diagram**

CSG324 Package—LX16

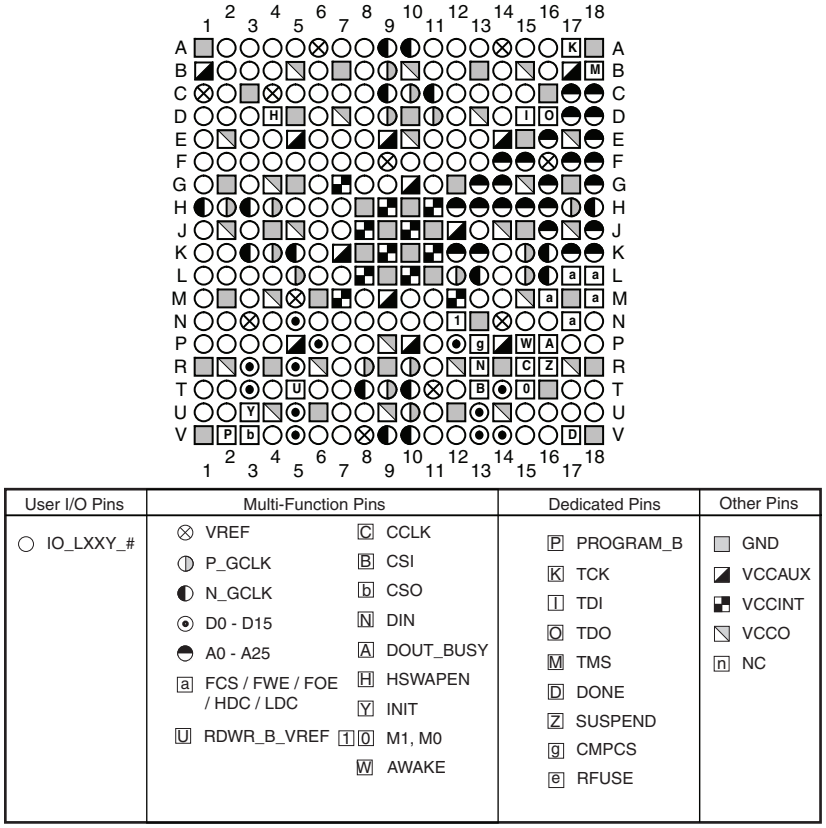


Figure 3-13: **CSG324 Package—LX16 Pinout Diagram**

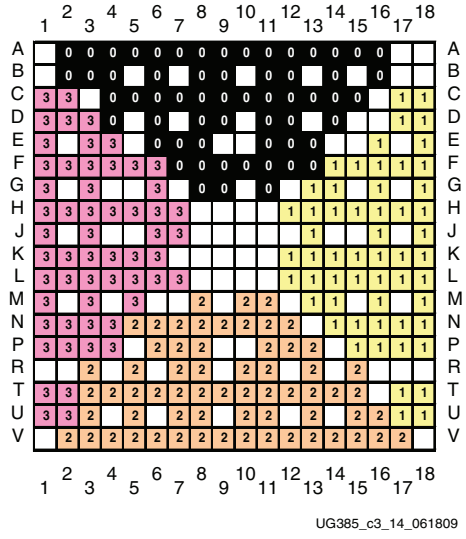
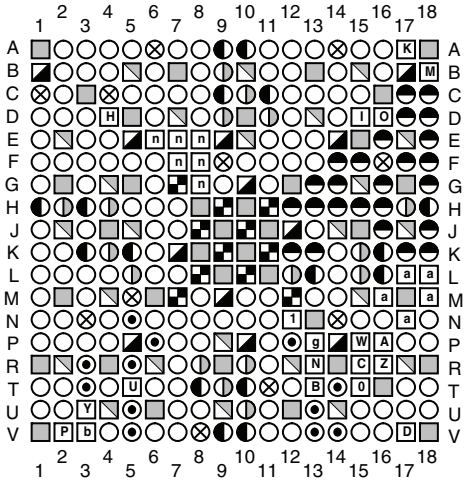


Figure 3-14: **CSG324 Package—LX16 SelectIO Bank Diagram**

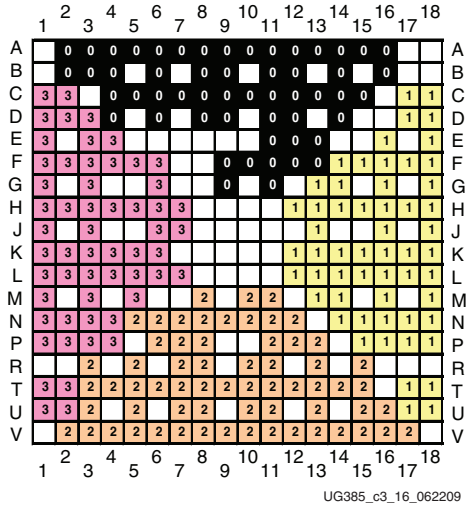
CSG324 Package—LX25



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	◪ VCCAUX
	◐ N_GCLK	b CSO	I TDI	◩ VCCINT
	⊙ D0 - D15	N DIN	O TDO	▧ VCCO
	◓ A0 - A25	A DOUT_BUSY	M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	
	U RDWR_B_VREF	Y INIT	Z SUSPEND	
		1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_15_062209

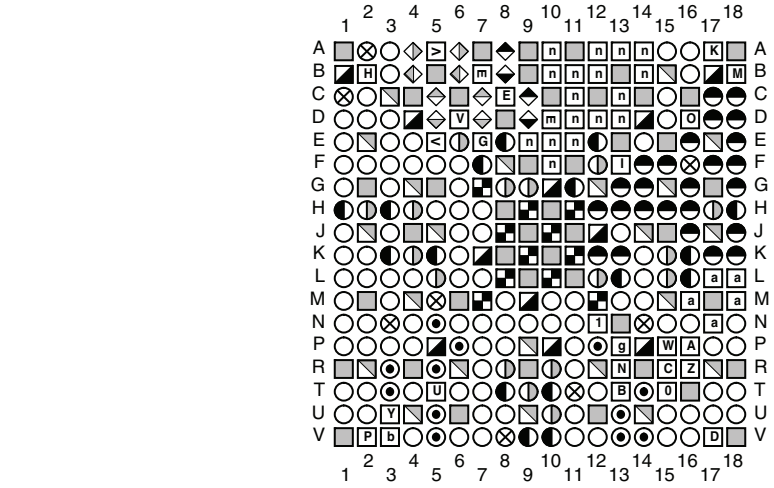
Figure 3-15: **CSG324 Package—LX25 Pinout Diagram**



UG385_c3_16_062209

Figure 3-16: **CSG324 Package—LX25 SelectIO Bank Diagram**

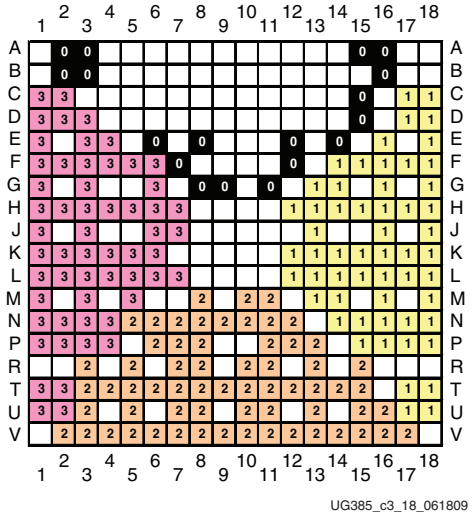
CSG324 Package—LX25T



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	VCCAUX
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	VCCINT
	⊙ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	VCCO
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	
	U RDWR_B_VREF	Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	
		1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_17_061809

Figure 3-17: **CSG324 Package—LX25T Pinout Diagram**



UG385_c3_18_061809

Figure 3-18: **CSG324 Package—LX25T SelectIO Bank Diagram**

CSG324 Package—LX45

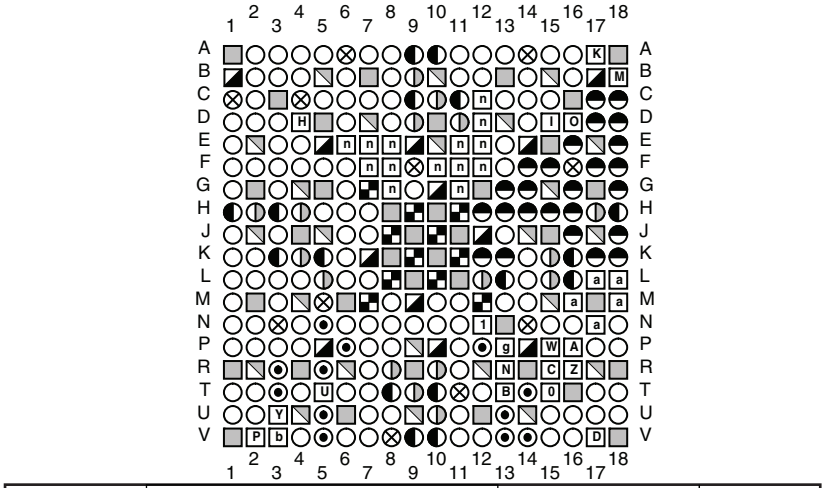


Figure 3-19: **CSG324 Package—LX45 Pinout Diagram**

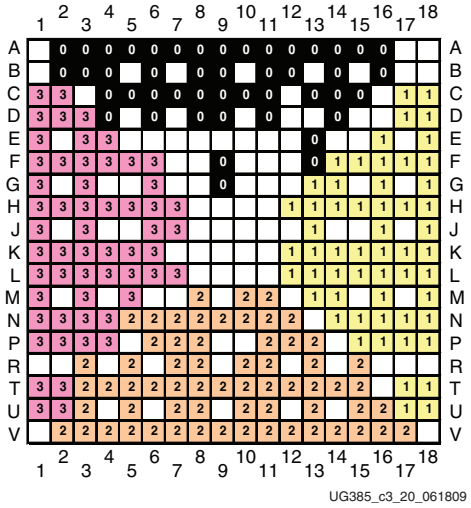
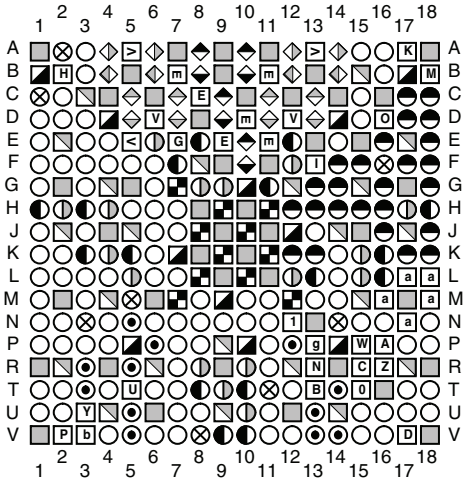


Figure 3-20: **CSG324 Package—LX45 SelectIO Bank Diagram**

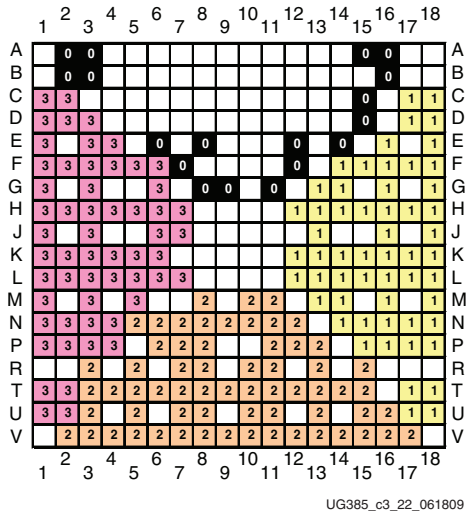
CSG324 Package—LX45T



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	◪ VCCAUX
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	◩ VCCINT
	⊙ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	▨ VCCO
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	
	U RDWR_B_VREF	Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	
		1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_21_061809

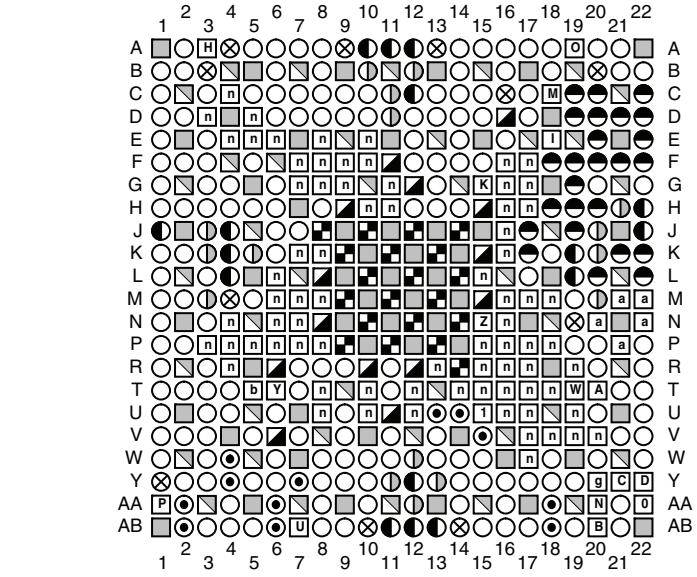
Figure 3-21: **CSG324 Package—LX45T Pinout Diagram**



UG385_c3_22_061809

Figure 3-22: **CSG324 Package—LX45T SelectIO Bank Diagram**

FG(G)484 Package—LX25



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND
	P_GCLK	CSI	TCK	VCCAUX
	N_GCLK	CSO	TDI	VCCINT
	D0 - D15	DIN	TDO	VCCO
	A0 - A25	DOUT_BUSY	TMS	NC
	FCS / FWE / FOE / HDC / LDC	HSWAPEN	DONE	
		INIT	SUSPEND	
	RDWR_B_VREF	M1, M0	CMPCS	
		AWAKE	RFUSE	

UG385_c3_23_061809

Figure 3-23: **FG(G)484 Package—LX25 Pinout Diagram**

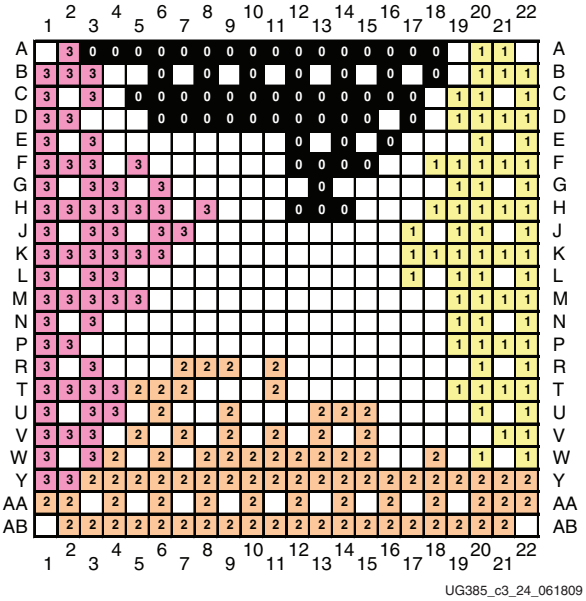
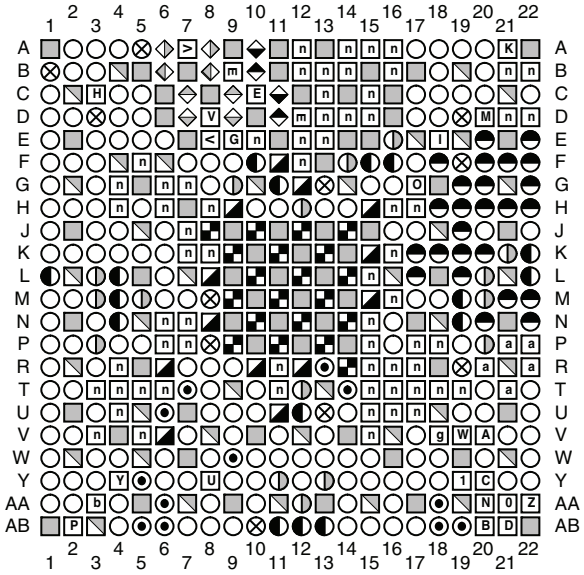


Figure 3-24: **FG(G)484 Package—LX25 SelectIO Bank Diagram**

FG(G)484 Package—LX25T



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	◪ VCCAUX
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	◩ VCCINT
	⊙ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	▧ VCCO
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	n NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	
		Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	
	U RDWR_B_VREF	1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_25_061809

Figure 3-25: **FG(G)484 Package—LX25T Pinout Diagram**

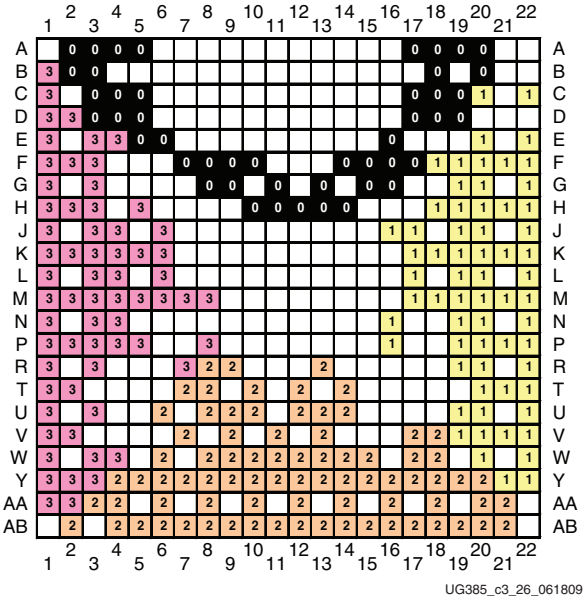
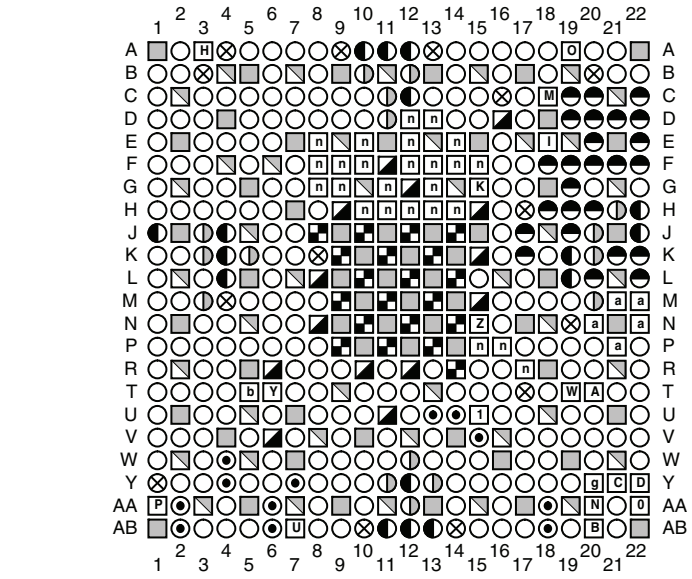


Figure 3-26: **FG(G)484 Package—LX25T SelectIO Bank Diagram**

FG(G)484 Package—LX45



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND
	P_GCLK	CSI	TCK	VCCAUX
	N_GCLK	CSO	TDI	VCCINT
	D0 - D15	DIN	TDO	VCCO
	A0 - A25	DOUT_BUSY	TMS	NC
	FCS / FWE / FOE / HDC / LDC	HSWAPEN	DONE	
		INIT	SUSPEND	
	RDWR_B_VREF	M1, M0	CMPCS	
		AWAKE	RFUSE	

UG385_c3_27_061809

Figure 3-27: **FG(G)484 Package—LX45 Pinout Diagram**

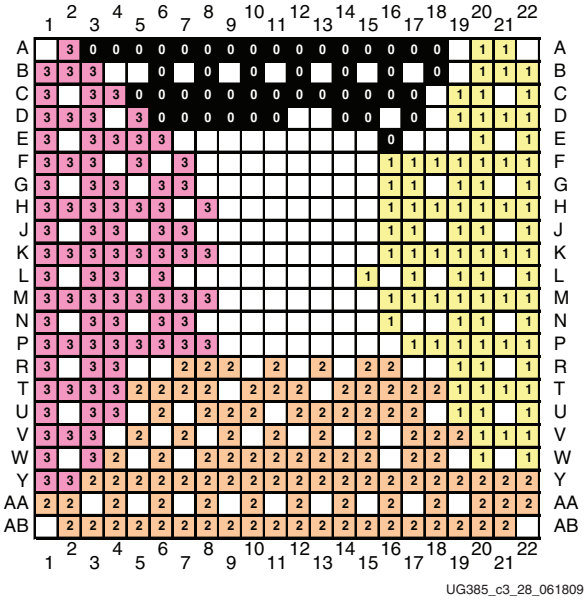


Figure 3-28: **FG(G)484 Package—LX45 SelectIO Bank Diagram**

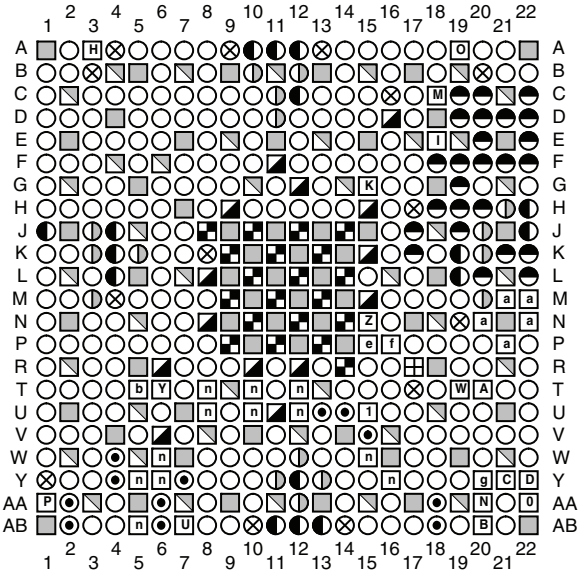
FG(G)484 Package—LX75

Data on the LX75 is not currently available.

Figure 3-29: **FG(G)484 Package—LX75 Pinout Diagram**

Figure 3-30: **FG(G)484 Package—LX75 SelectIO Bank Diagram**

FG(G)484 Package—LX100



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	f VFS
	◐ N_GCLK	b CSO	I TDI	VBATT
	⊙ D0 - D15	N DIN	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	VCCO
	U RDWR_B_VREF	Y INIT	Z SUSPEND	n NC
		1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_31_062209

Figure 3-31: **FG(G)484 Package—LX100 Pinout Diagram**

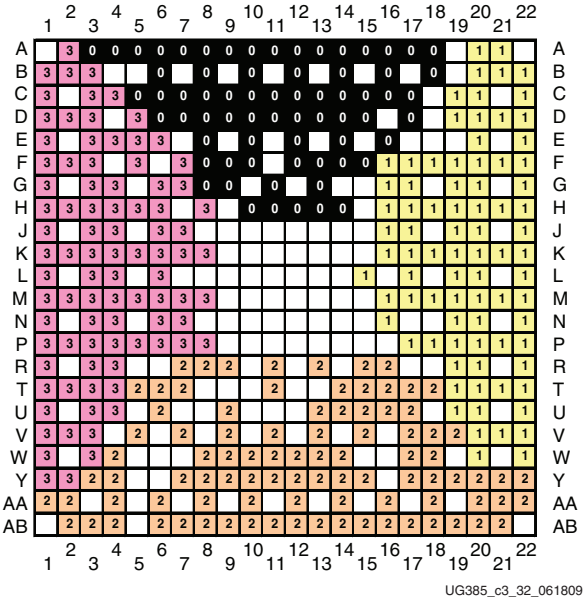
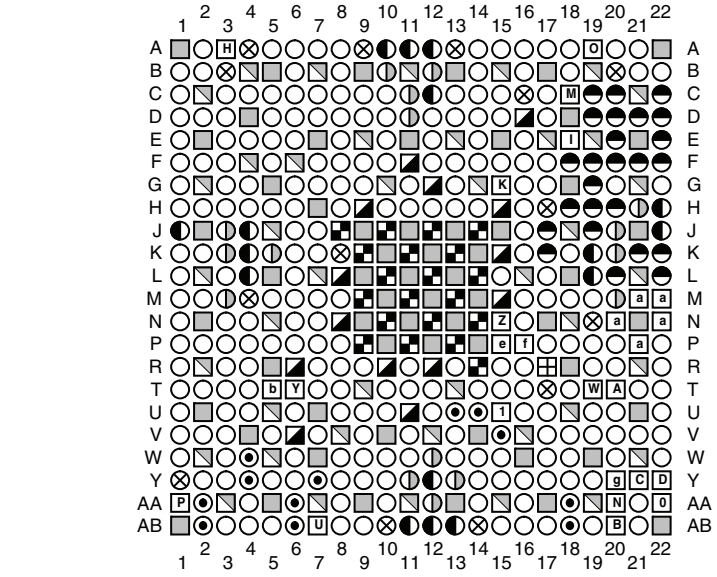


Figure 3-32: **FG(G)484 Package—LX100 SelectIO Bank Diagram**

FG(G)484 Package—LX150



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	f VFS
	◐ N_GCLK	b CSO	I TDI	VBATT
	⊙ D0 - D15	N DIN	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	VCCO
		Y INIT	Z SUSPEND	n NC
	U RDWR_B_VREF	1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_33_062209

Figure 3-33: **FG(G)484 Package—LX150 Pinout Diagram**

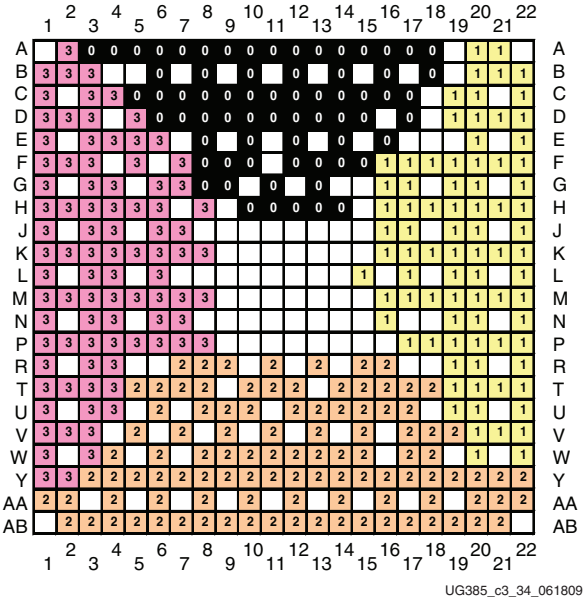
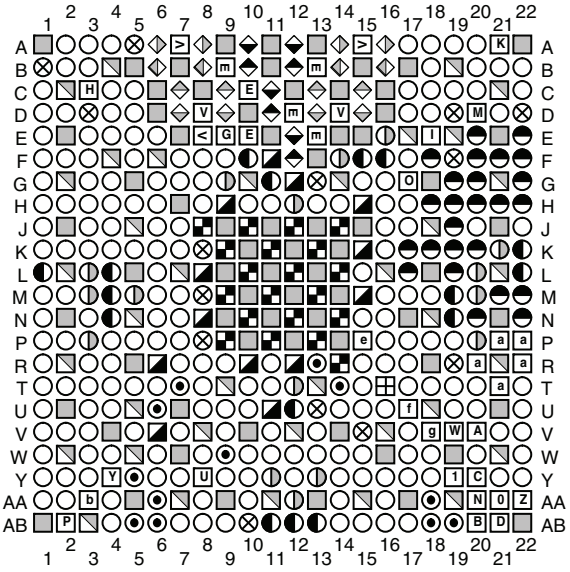


Figure 3-34: **FG(G)484 Package—LX150 SelectIO Bank Diagram**

FG(G)484 Package—LX45T, LX75T, LX100T, and LX150T

Data on the LX75T is not currently available.



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	f VFS
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	VBATT
	⊙ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	VCCO
	U RDWR_B_VREF	Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	n NC
		1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_35_062209

Figure 3-35: **FG(G)484 Package—LX45T, LX75T, LX100T, and LX150T Pinout Diagram**

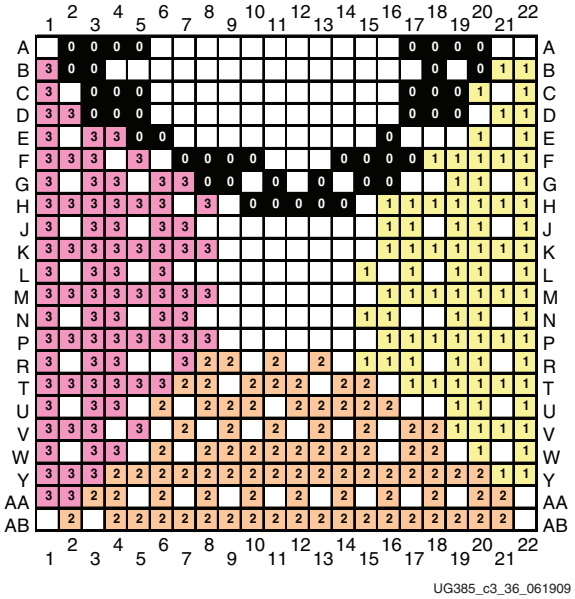


Figure 3-36: **FG(G)484 Package—LX45T, LX75T, LX100T, and LX150T SelectIO Bank Diagram**

CSG484 Package—LX45 and LX75

Data on devices in this package is not currently available.

Figure 3-37: **CSG484 Package—LX45 and LX75 Pinout Diagram**

Figure 3-38: **CSG484 Package—LX45 and LX75 SelectIO Bank Diagram**

CSG484 Package—LX100

Data on devices in this package is not currently available.

Figure 3-39: **CSG484 Package—LX100 Pinout Diagram**

Figure 3-40: **CSG484 Package—LX100SelectIO Bank Diagram**

CSG484 Package—LX150

Data on devices in this package is not currently available.

Figure 3-41: **CSG484 Package—LX150 Pinout Diagram**

Figure 3-42: **CSG484 Package—LX150 SelectIO Bank Diagram**

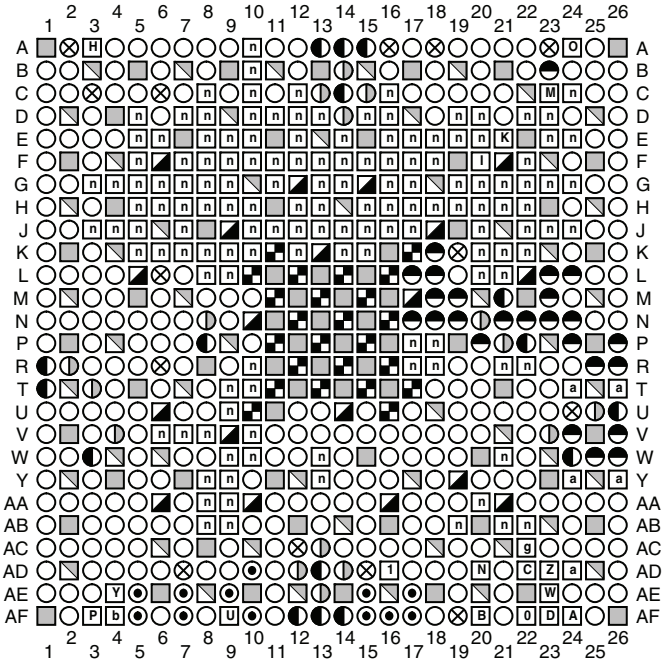
CSG484 Package—LX45T, LX75T, LX100T, and LX150T

Data on devices in this package is not currently available.

Figure 3-43: **CSG484 Package—LX45T, LX75T, LX100T, and LX150T Pinout Diagram**

Figure 3-44: **CSG484 Package—LX45T, LX75T, LX100T, and LX150T SelectIO Bank Diagram**

FG(G)676 Package—LX45



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	VCCAUX
	◐ N_GCLK	b CSO	I TDI	VCCINT
	⊙ D0 - D15	N DIN	O TDO	VCCO
	◓ A0 - A25	A DOUT_BUSY	M TMS	NC
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	
		Y INIT	Z SUSPEND	
	U RDWR_B_VREF	1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_45_061809

Figure 3-45: **FG(G)676 Package—LX45 Pinout Diagram**

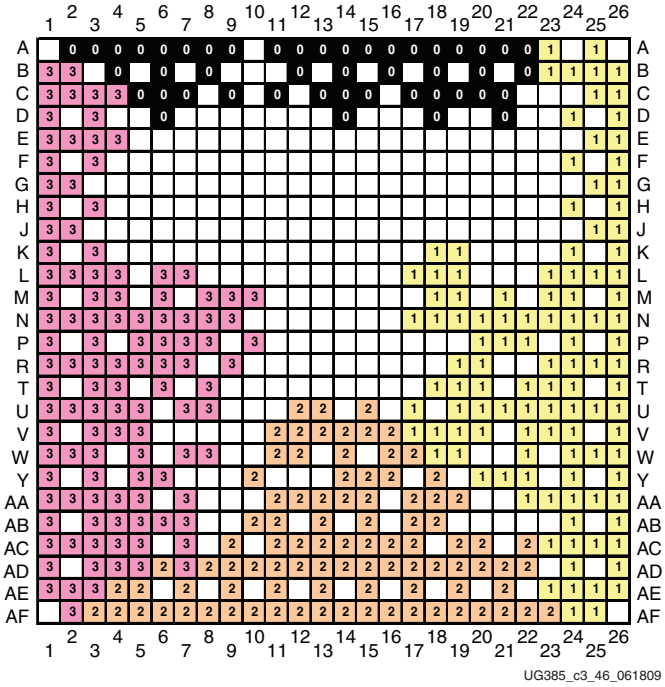


Figure 3-46: **FG(G)676 Package—LX45 SelectIO Bank Diagram**

FG(G)676 Package—LX75

Data on the LX75 is not currently available.

Figure 3-47: **FG(G)676 Package—LX75 Pinout Diagram**

Figure 3-48: **FG(G)676 Package—LX75 SelectIO Bank Diagram**

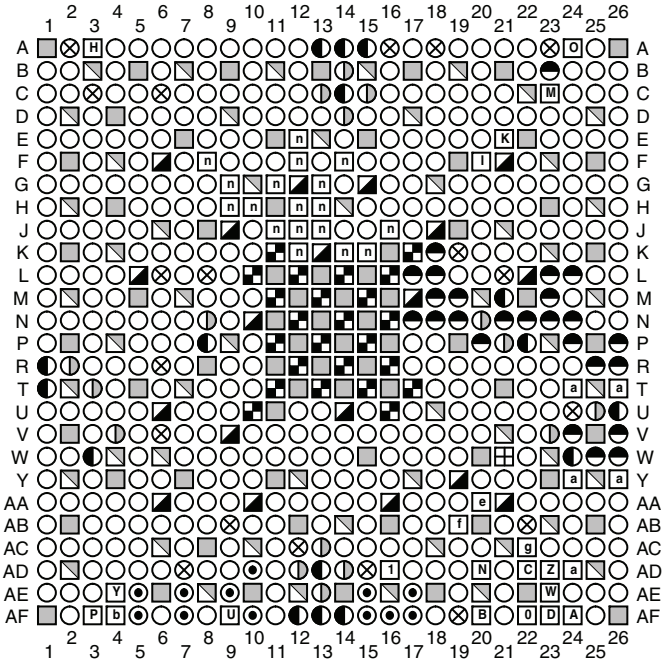
FG(G)676 Package—LX75T

Data on the LX75T is not currently available.

Figure 3-49: **FG(G)676 Package—LX75T Pinout Diagram**

Figure 3-50: **FG(G)676 Package—LX75T SelectIO Bank Diagram**

FG(G)676 Package—LX100



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	f VFS
	◐ N_GCLK	b CSO	I TDI	VBATT
	⊙ D0 - D15	N DIN	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	VCCO
		Y INIT	Z SUSPEND	n NC
	U RDWR_B_VREF	1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_51_062209

Figure 3-51: **FG(G)676 Package—LX100 Pinout Diagram**

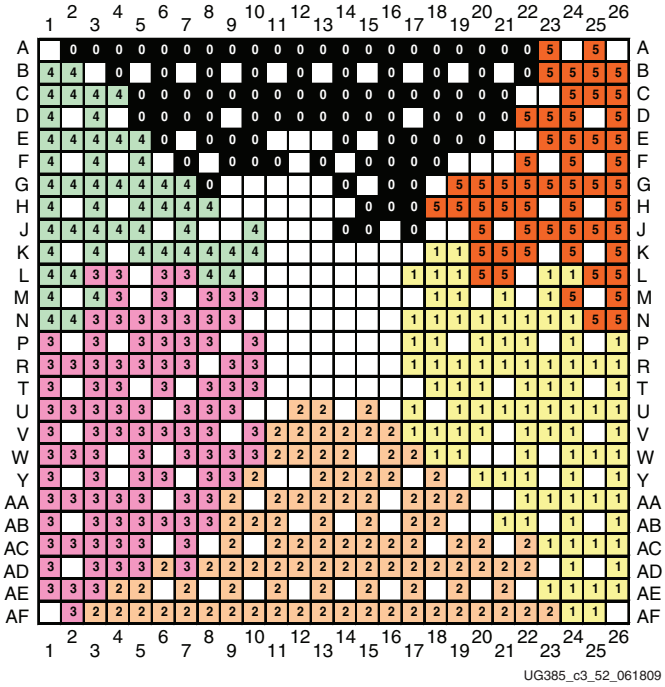
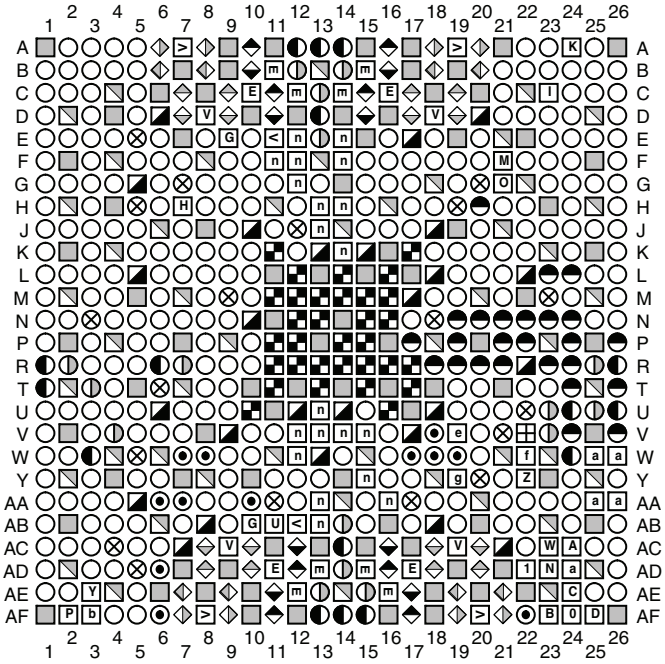


Figure 3-52: **FG(G)676 Package—LX100 SelectIO Bank Diagram**

FG(G)676 Package—LX100T



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	f VFS
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	VBATT
	⊙ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	VCCO
		Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	n NC
	U RDWR_B_VREF	1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_53_062209

Figure 3-53: **FG(G)676 Package—LX100T Pinout Diagram**

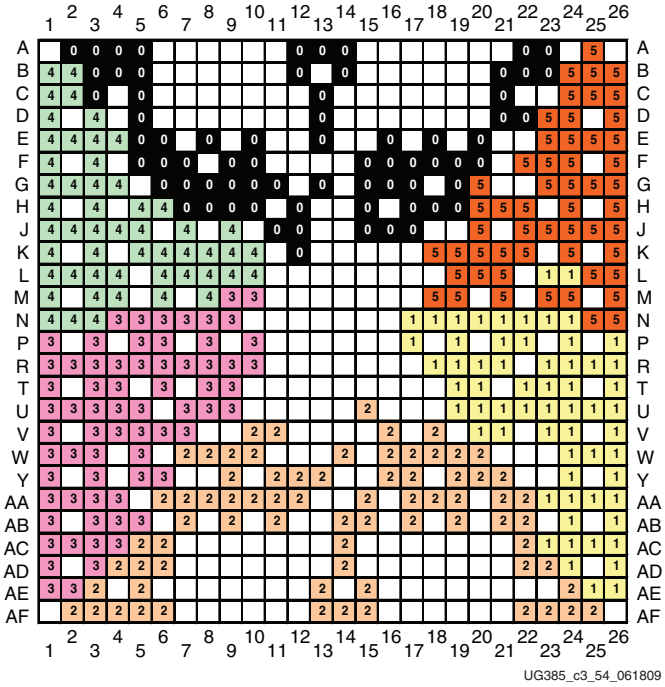
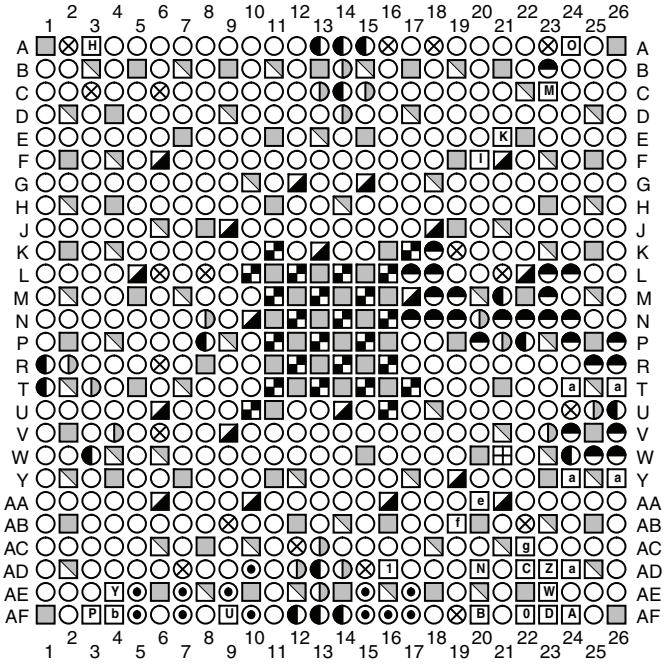


Figure 3-54: **FG(G)676 Package—LX100T SelectIO Bank Diagram**

FG(G)676 Package—LX150



User I/O Pins	Multi-Function Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	K TCK	f VFS
	◐ N_GCLK	b CSO	I TDI	VBATT
	⊙ D0 - D15	N DIN	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	D DONE	VCCO
		Y INIT	Z SUSPEND	n NC
	U RDWR_B_VREF	1 0 M1, M0	g CMPCS	
		W AWAKE	e RFUSE	

UG385_c3_55_062209

Figure 3-55: **FG(G)676 Package—LX150 Pinout Diagram**

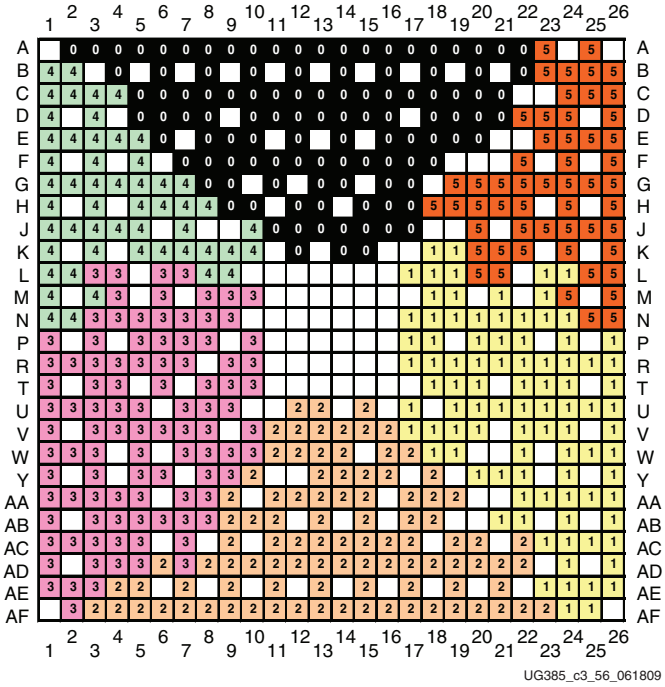
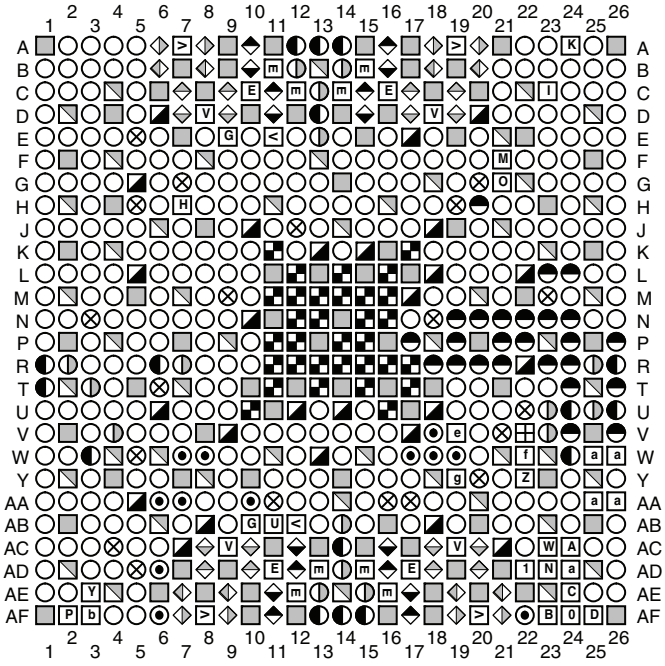


Figure 3-56: **FG(G)676 Package—LX150 SelectIO Bank Diagram**

FG(G)676 Package—LX150T



User I/O Pins	Multi-Function Pins		Transceiver Pins		Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	E MGTAVCC	◇ MGTRXP	P PROGRAM_B	GND
	◑ P_GCLK	B CSI	m MGTAVCCPLL	◇ MGTRXN	K TCK	f VFS
	◐ N_GCLK	b CSO	V MGTAVTTRX	◇ MGTTXN	I TDI	VBATT
	⦿ D0 - D15	N DIN	< MGTAVTTRCAL	◇ MGTTXP	O TDO	VCCAUX
	◓ A0 - A25	A DOUT_BUSY	> MGTAVTTTX		M TMS	VCCINT
	a FCS / FWE / FOE / HDC / LDC	H HSWAPEN	◆ MGTREFCLK (P)		D DONE	VCCO
	U RDWR_B_VREF	Y INIT	◆ MGTREFCLK (N)		Z SUSPEND	n NC
		1 0 M1, M0	G MGTRREF		g CMPCS	
		W AWAKE			e RFUSE	

UG385_c3_57_062209

Figure 3-57: **FG(G)676 Package—LX150T Pinout Diagram**

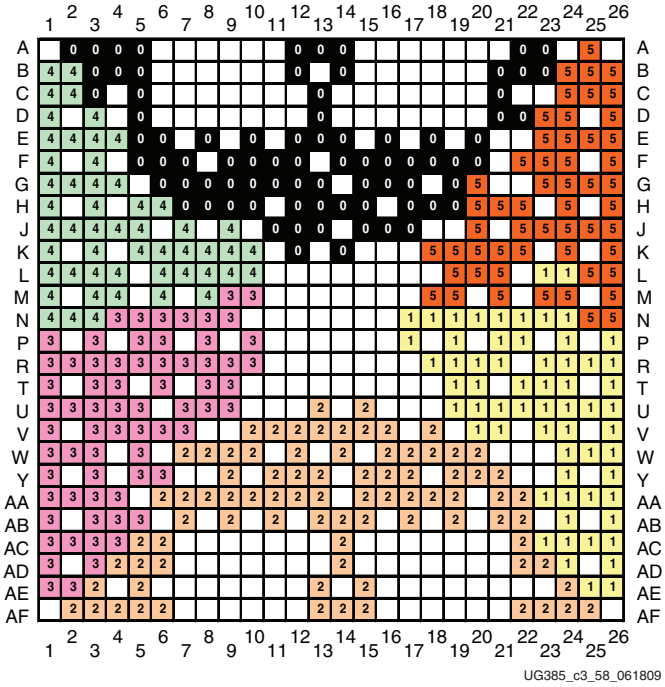


Figure 3-58: **FG(G)676 Package—LX150T SelectIO Bank Diagram**

FG(G)900 Package—LX100T

Data on devices in this package is not currently available.

Figure 3-59: **FG(G)900 Package—LX100T Pinout Diagram**

Figure 3-60: **FG(G)900 Package—LX100T SelectIO Bank Diagram**

FG(G)900 Package—LX150

Data on devices in this package is not currently available.

Figure 3-61: **FG(G)900 Package—LX150 Pinout Diagram**

Figure 3-62: **FG(G)900 Package—LX150 SelectIO Bank Diagram**

FG(G)900 Package—LX150T

Data on devices in this package is not currently available.

Figure 3-63: **FG(G)900 Package—LX150T Pinout Diagram**

Figure 3-64: **FG(G)900 Package—LX150T SelectIO Bank Diagram**

XILINX®

Chapter 4

Mechanical Drawings

Summary

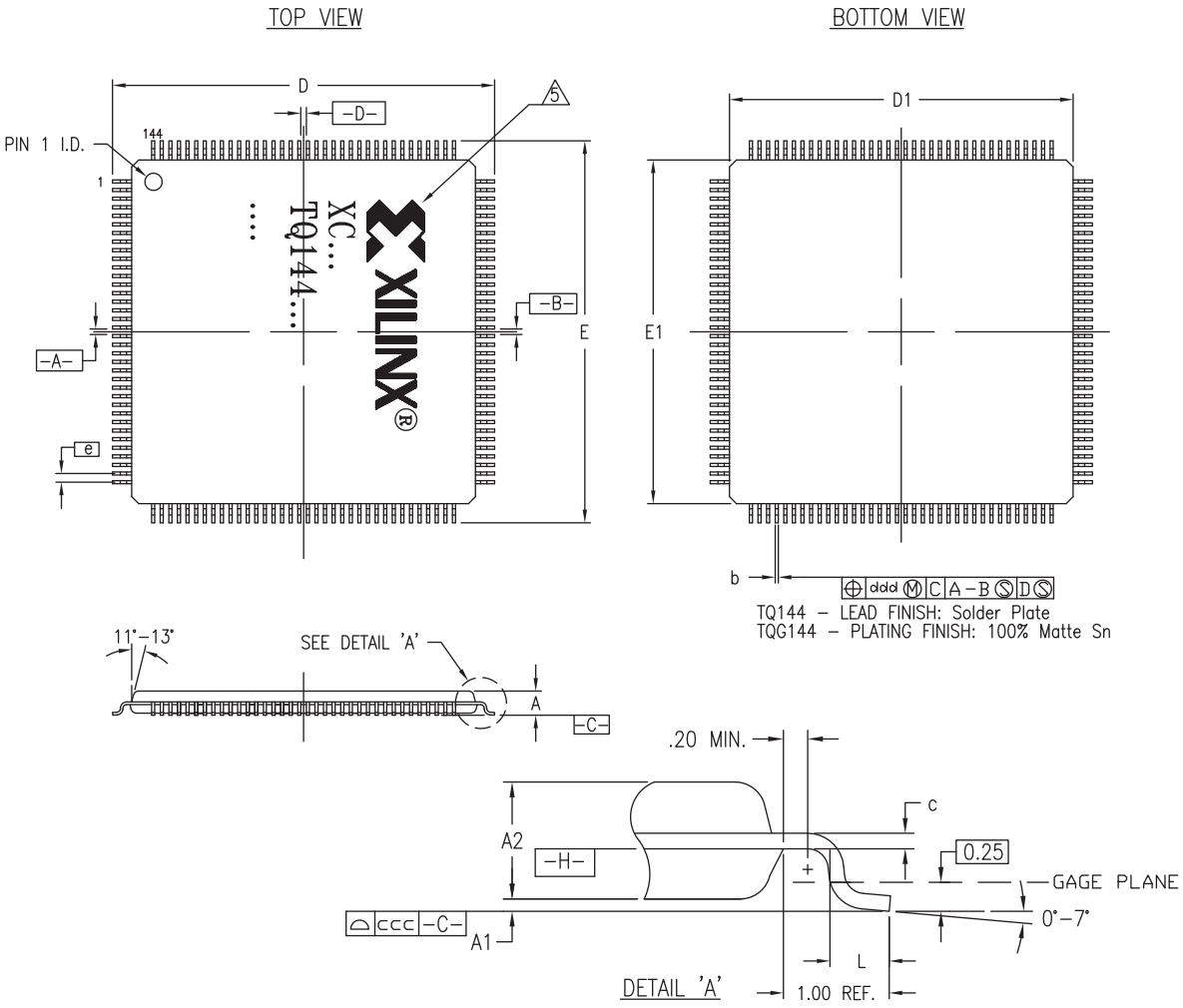
This chapter provides mechanical drawings of the following Spartan-6 FPGA packages:

CPG196 Chip-Scale BGA Package Specifications (0.5 mm Pitch)

This drawing is currently unavailable.

Figure 4-1: **CPG196 Chip-Scale BGA Package**

TQG144 Thin Quad Flat-Pack Package Specifications (0.5 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D/E	22.00 BSC		
D_1/E_1	20.00 BSC		
b	0.17	0.22	0.27
c	0.09		0.20
e	0.50 BSC		
L	0.45	0.60	0.75
ccc			0.08
ddd			0.08

NOTES:

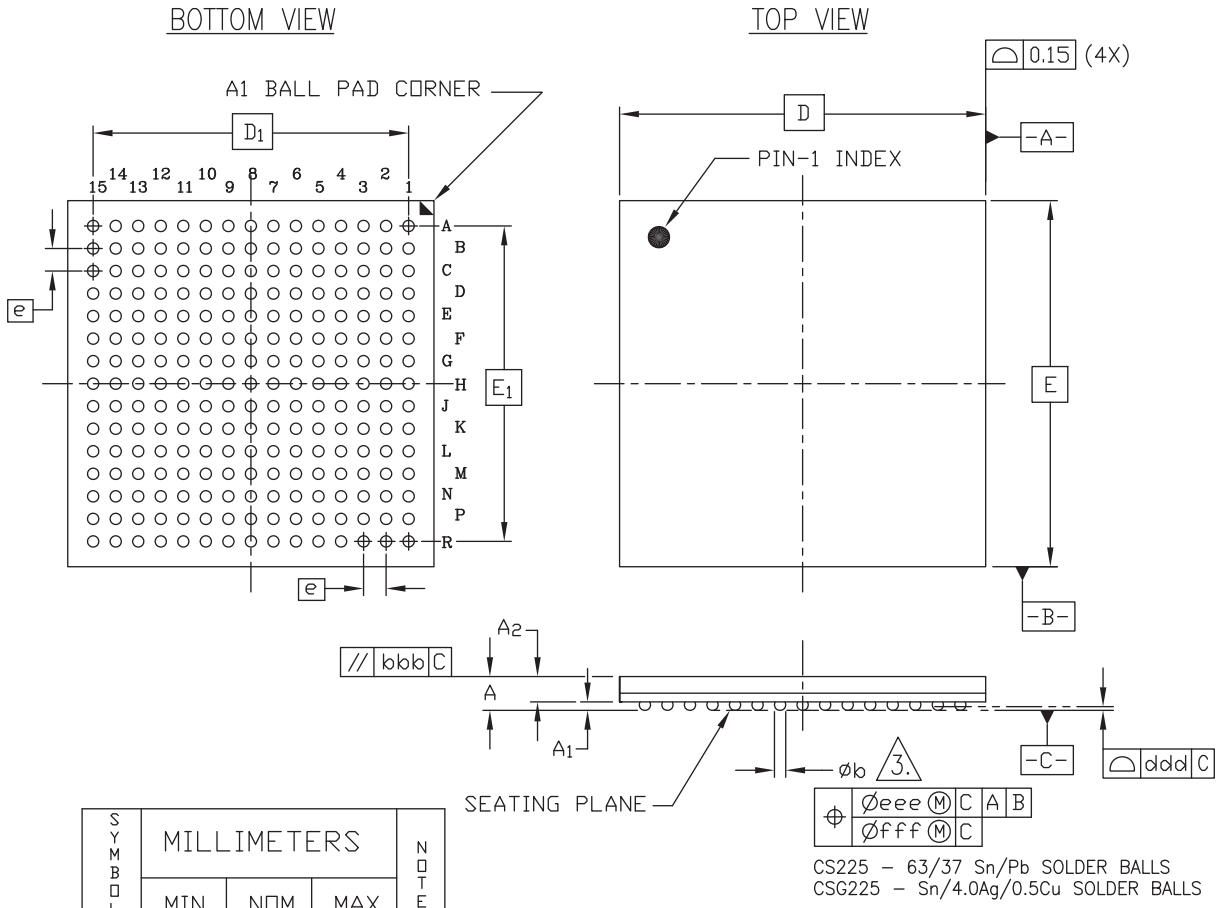
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm EACH SIDE.
3. THE TOP OF PACKAGE MAYBE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.10mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026–BFB

5. MARK ORIENTATION WITH RESPECT TO PIN–1 I.D. IF 2 OR MORE CIRCLES EXIST ON TOP OF THE PACKAGE, USE THE SMALLEST CIRCLE AS PIN–1 I.D.

ug385_c4_02_061709

Figure 4-2: **TQG144 Thin Quad Flat-Pack Package**

CSG225 Chip-Scale BGA Package Specifications (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.40	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.00	
D/E	13.00 BSC			
D_1/E_1	11.20 BSC			
e	0.80 BSC			
øb	0.35	0.40	0.45	3
bbb			0.20	
ddd			0.10	
eee			0.15	
fff			0.08	
M	15			2

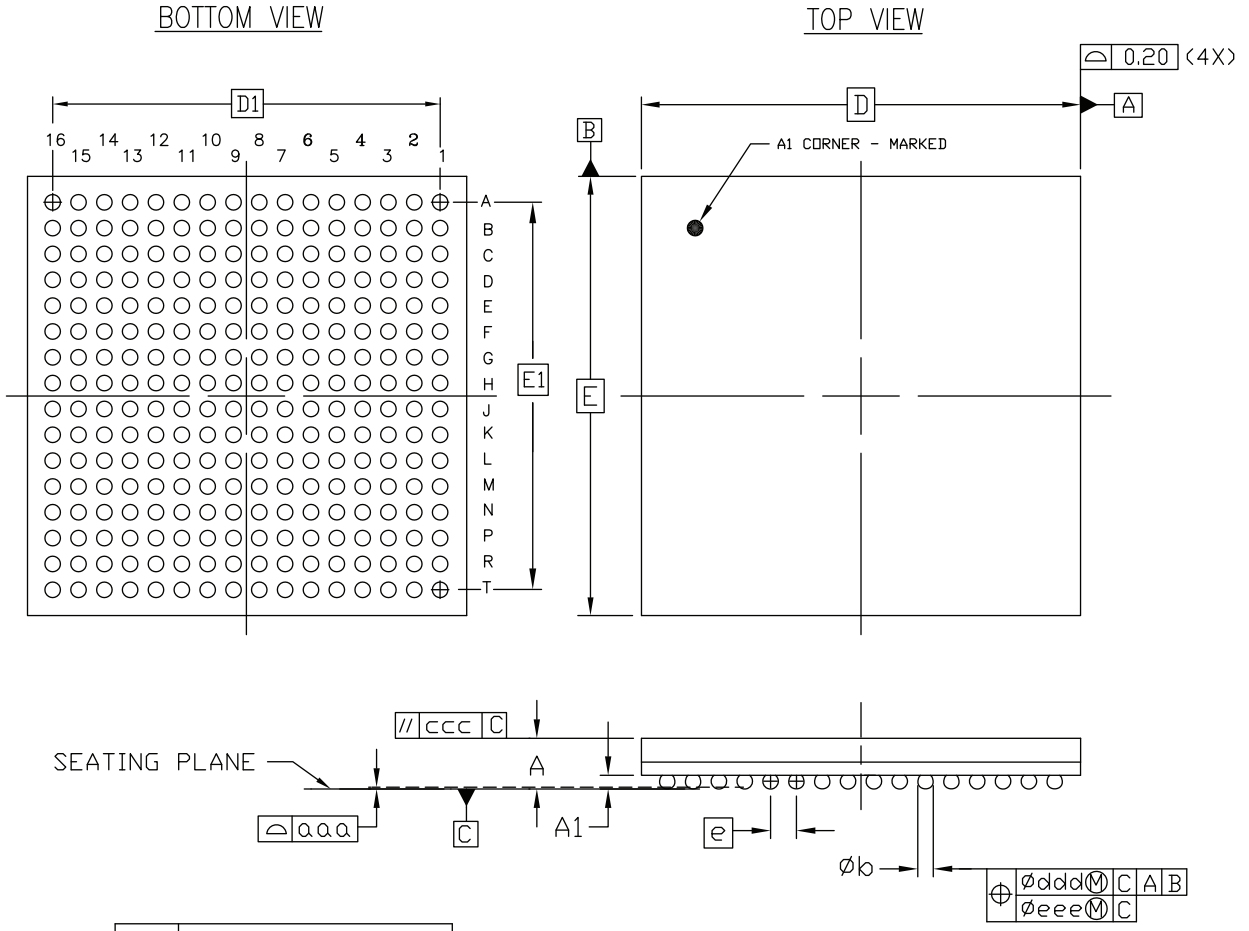
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. CONFORMS TO JEDEC MO–275–HHAC–1.

ug385_c4_03_061709

Figure 4-3: **CSG225 Chip-Scale BGA Package**

FT(G)256 Fine-Pitch Thin BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.40	1.55
A_1	0.30	0.40	0.50
D/E	17.00 BSC		
D_1/E_1	15.00 REF		
e	1.00 BSC		
Øb	0.40	0.50	0.60
aaa			0.15
ccc			0.15
ddd			0.25
eee			0.10
M	16		

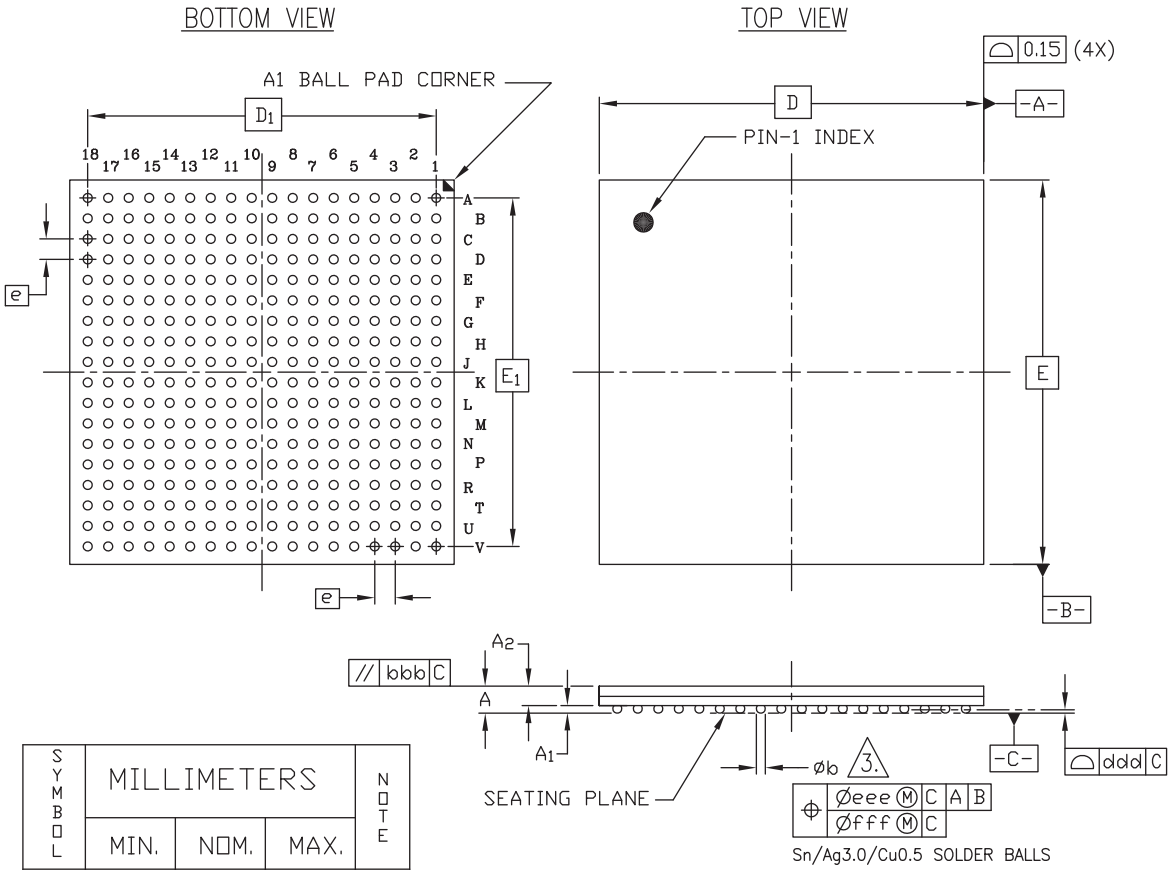
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAF–1 EXCEPT FOR THE SOLDER BALL SIZE.

ug385_c4_04_061709

Figure 4-4: **FT(G)256 Fine-Pitch Thin BGA Package**

CSG324 Chip-Scale BGA Package Specifications (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.50	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.35	0.40	0.45	3
bbb			0.20	
ddd			0.10	
eee			0.15	
fff			0.08	
M	18			2

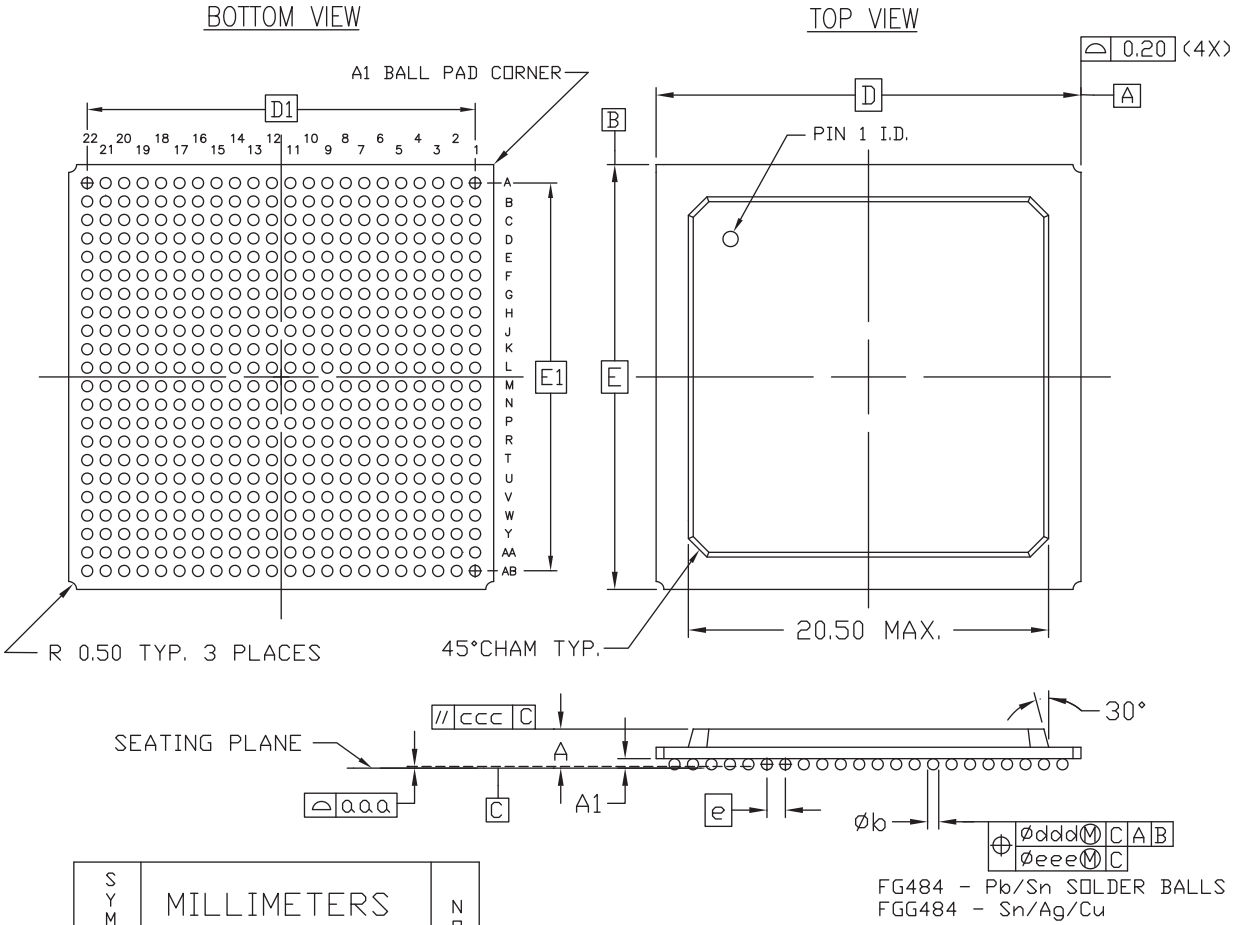
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. CONFORMS TO JEDEC MO–275–KKAC–1.

ug385_c4_05_061709

Figure 4-5: **CSG324 Chip-Scale BGA Package**

FG(G)484 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.60	
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

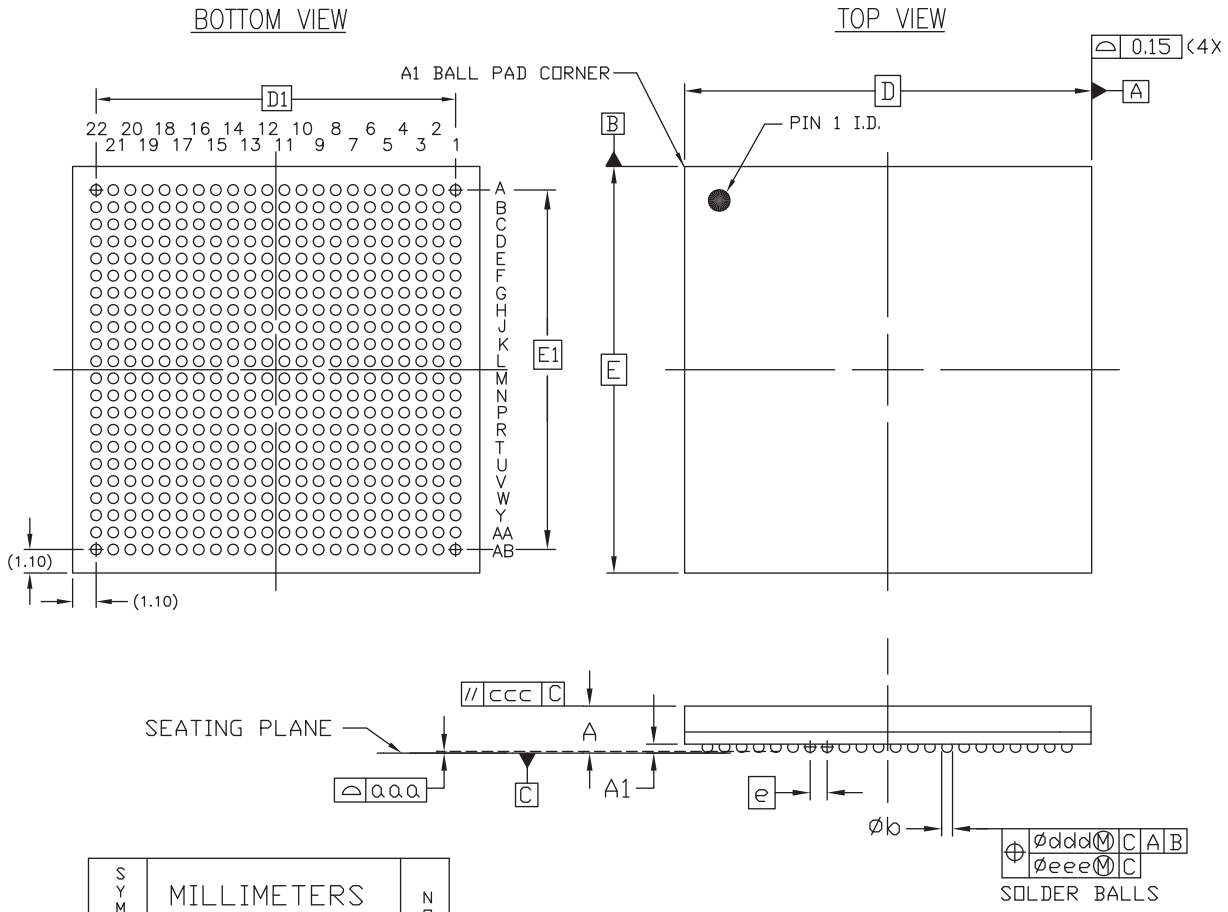
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1.

ug385_c4_06_061709

Figure 4-6: **FG(G)484 Fine-Pitch BGA Package**

CSG484 Chip-Scale BGA Package Specifications (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.57	1.67	1.80	
A_1	0.30	0.38	0.45	
D/E	19.00 BSC			
D_1/E_1	16.80 BSC			
e	0.80 BSC			
Øb	0.40	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	22			2

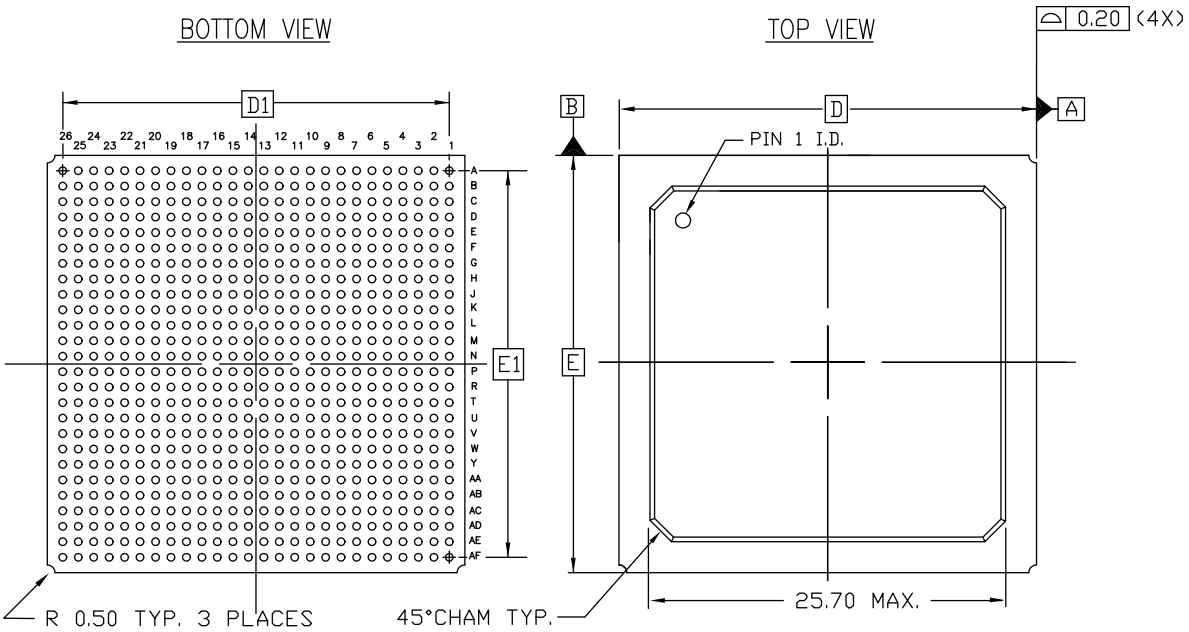
NOTES:

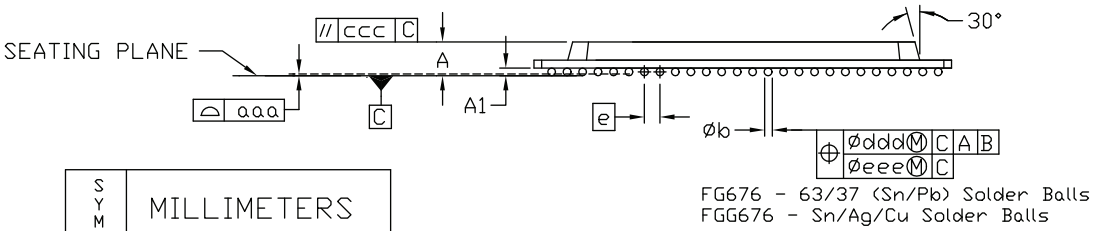
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO–275–PPAA–2.

ug385_c4_07_061809

Figure 4-7: **CSG484 Chip-Scale BGA Package**

FG(G)676 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)





FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

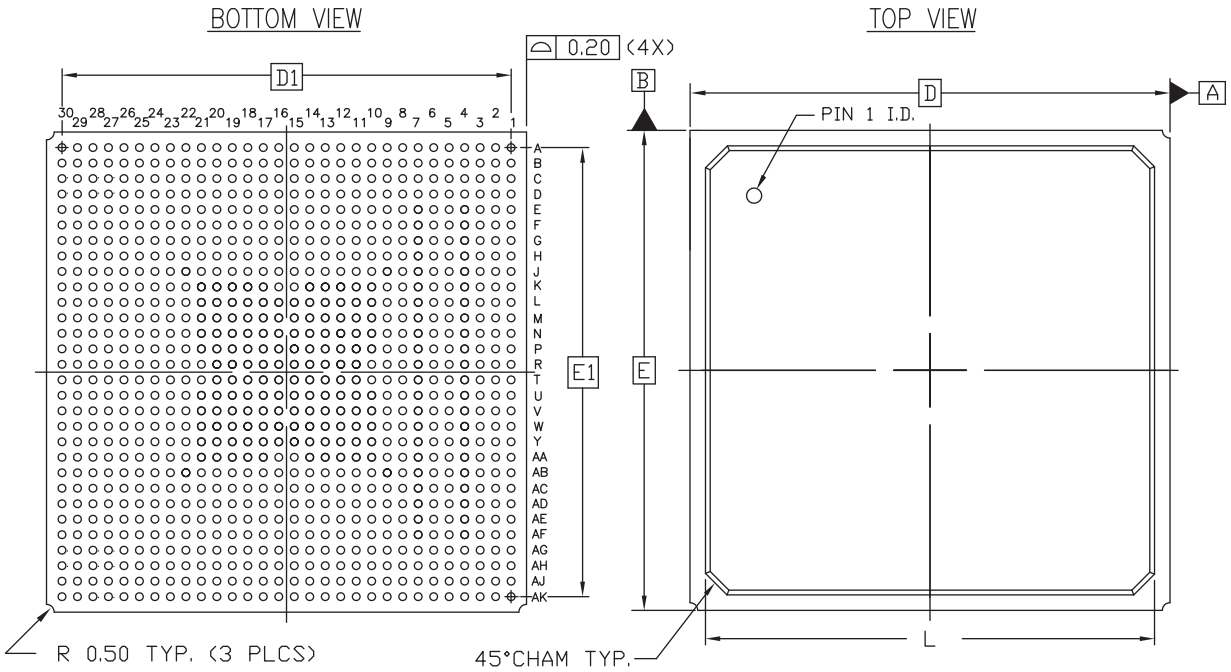
NOTES:

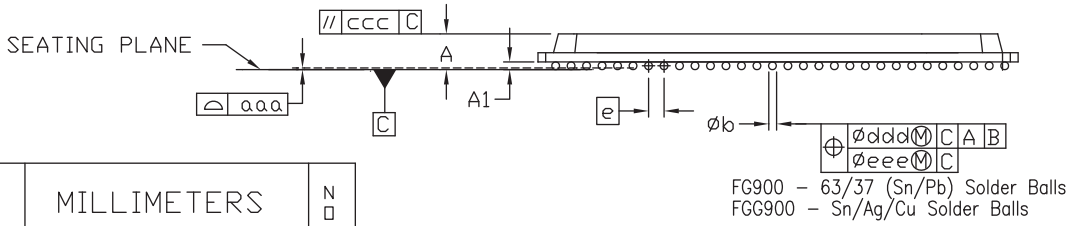
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug385_c4_08_061709

Figure 4-8: **FG(G)676 Fine-Pitch BGA Package**

FG(G)900 Chip-Scale BGA Package Specifications (1.0 mm Pitch)





SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		2.25	2.60	
A_1	0.40	0.50	0.60	
D/E	31.00 BSC			
D_1/E_1	29.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
L			29.05	
M	30			2
REF.	JEDEC MS-034-AAN-1			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.

ug385_c4_09_061809

Figure 4-9: **FG(G)900 Chip-Scale BGA Package**

XILINX®

Chapter 5

Thermal Specifications

Summary

This chapter provides thermal data associated with Spartan-6 FPGA packages. The following topics are discussed:

- Introduction
- Cavity-Up Plastic BGA Packages
- Support for Compact Thermal Models (CTM)
- References

Introduction

Spartan-6 devices are offered in a wide variety of packages. The suite of packages is used to address the various power requirements of the Spartan-6 devices. All Spartan-6 devices are implemented in the 45 nm process technology

All Spartan-6 devices feature versatile SelectIO™ resources that support a variety of I/O standards. They also include DSPs and other traditional features and blocks (such as block RAM) contained in earlier Spartan and Virtex® products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 45 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured Spartan-6 FPGA design that exploits the internal logic speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Spartan-6 devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Table 5-1 shows the thermal resistance data for Spartan-6 devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

- Thermal data is available on the Xilinx website at:
  http://www.xilinx.com/cgi-bin/thermal/thermal.pl.
- Compact package thermal models for these products are available on the Xilinx support download center (under the Device Model tab) at:
  http://www.xilinx.com/support/download/index.htm

Table 5-1: **Thermal Resistance Data—All Devices**

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
CPG196	8 x 8	XC6SLX4						
		XC6SLX9						
		XC6SLX16						
TQG144	20 x 20	XC6SLX4						
		XC6SLX9						
CSG225	13 x 13	XC6SLX4						
		XC6SLX9						
		XC6SLX16						
FT(G)256	17 x 17	XC6SLX9						
		XC6SLX16						
		XC6SLX25						
CSG324	15 x 15	XC6SLX9						
		XC6SLX16	27.8	13.7	8.85	22.5	21.1	20.0
		XC6SLX25						
		XC6SLX25T						
		XC6SLX45						
		XC6SLX45T						
FG(G)484	23 x 23	XC6SLX25						
		XC6SLX25T						
		XC6SLX45						
		XC6SLX45T	19.1	1.00	6.03	14.3	13.0	12.4
		XC6SLX75						
		XC6SLX75T						
		XC6SLX100						
		XC6SLX100T						
		XC6SLX150						
		XC6SLX150T						

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
CSG484	19 x 19	XC6SLX45						
		XC6SLX45T						
		XC6SLX75						
		XC6SLX75T						
		XC6SLX100						
		XC6SLX100T						
		XC6SLX150						
		XC6SLX150T						
FG(G)676	27 x 27	XC6SLX45						
		XC6SLX75						
		XC6SLX75T						
		XC6SLX100						
		XC6SLX100T						
		XC6SLX150						
		XC6SLX150T						
FG(G)900	31 x 31	XC6SLX100T						
		XC6SLX150						
		XC6SLX150T						

Package Strategy

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields.

The substrate is made of a multilayer BT (bismaleimide triazene) epoxy-based material. Power and ground pins are grouped together and the signal pins are assigned in the perimeter format for ease of routing on to the board. The package is offered in a die up format and contains a wirebonded device that is covered with a mold compound.

Package Construction

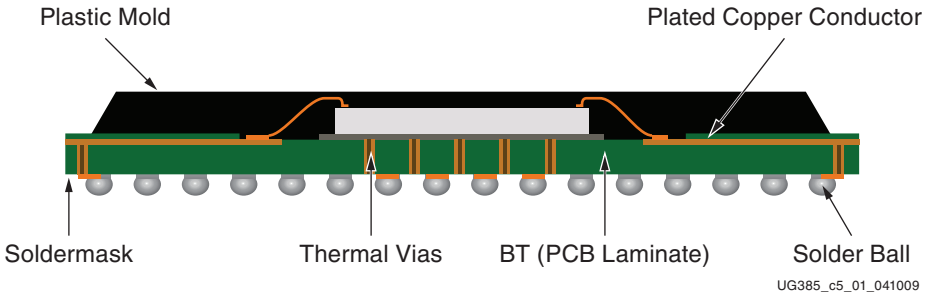


Figure 5-1: **Cavity-Up Ball Grid Array Package**

As shown in the cross section of Figure 5-1, the BGA package contains a wire bonded die on a single-core printed circuit board with an overmold. Beneath the die are the thermal vias which can dissipate the heat through a portion of the solder ball array and ultimately into the power and ground planes of the system circuit board. This thermal management technique provides better thermal dissipation than a standard PQFP package. Metal planes also distribute the heat across the entire package, enabling a 15–20% decrease in thermal resistance to the case.

Key Features/Advantages of Cavity-Up BGA Packages

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Chip Scale Packages

Chip Scale (CSP) packages meet the demands of miniaturization while offering improved performance. Applications for CSP packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption/dissipation must be low. By employing Spartan-6 FPGA CSP packages, system designers can dramatically reduce board real estate. Xilinx CSP packages are rigid BT-based substrates (see Figure 5-2).

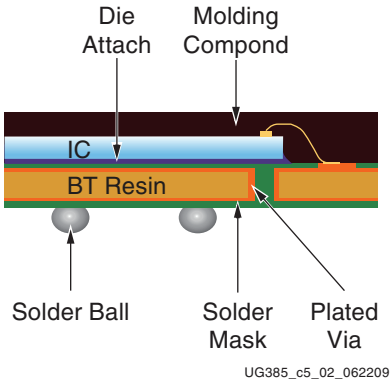


Figure 5-2: **Rigid BT-Based Substrate CSP Packages**

Key Features/Advantages of CSP Packages

- An extremely small form factor which significantly reduces board real estate for such applications as portable and wireless designs and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light-weight package

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for Spartan-6 devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for Spartan-6 FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all Spartan-6 devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-3.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center at: http://www.xilinx.com/support/download/index.htm.

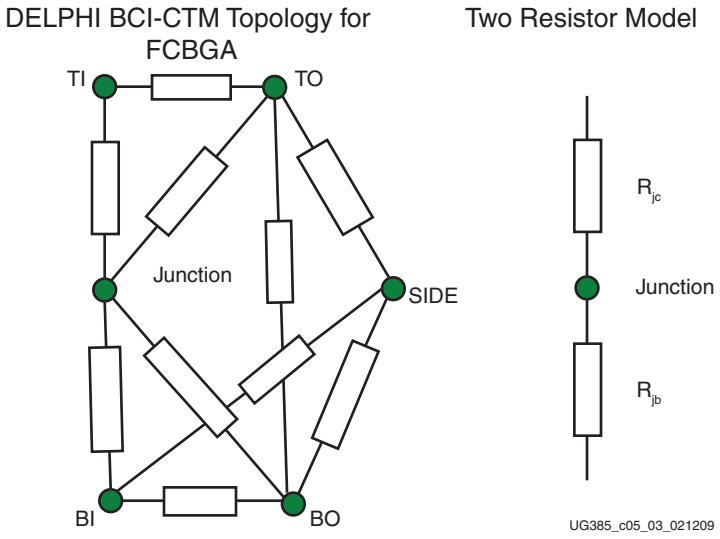


Figure 5-3: **Thermal Model Topologies**

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepack (version 4.2 and above) format.

References

The following websites contain additional information on heat management and contact information.

- http://www.wakefield.com
- http://www.aavidthermalloy.com
- http://www.qats.com

Refer to the following websites for interface material sources:

- Power Devices - http://www.powerdevices.com
- Bergquist Company - http://www.bergquistcompany.com
- AOS Thermal Compound - http://www.aosco.com
- Chomerics - http://www.chomerics.com
- Kester - http://www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Flomerics - Flotherm & FloPCB - http://www.flomerics.com
- Fluent - Icepak - http://www.icepak.com

Chapter 6

Package Marking

All Spartan-6 devices have package top-markings similar to the example shown in Figure 6-1 and explained in Table 6-1.

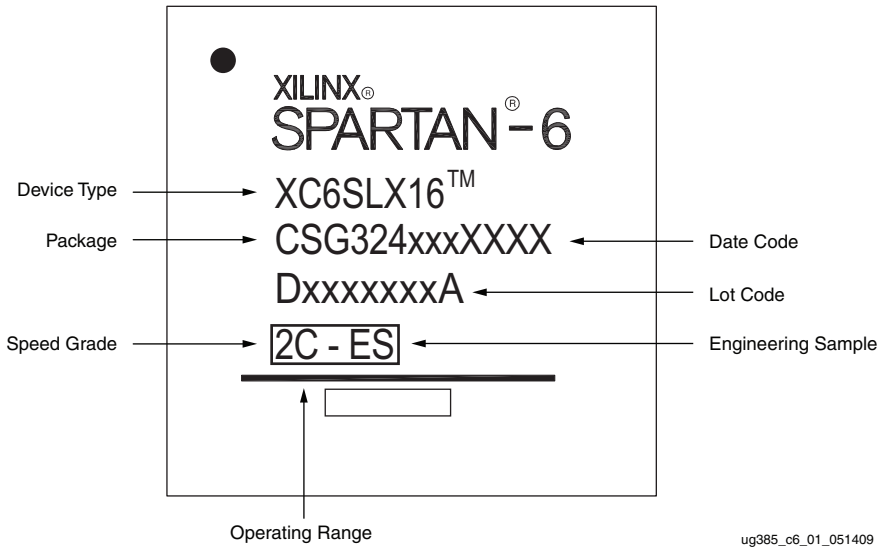


Figure 6-1: **Spartan-6 Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Spartan-6 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree.
3rd Line	Ten alphanumeric characters for Assembly and Lot information. The last digit is usually an *A* or an *M*.

Table 6-1: **Xilinx Device Marking Definition—Example *(Cont'd)***

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	L1I	The *L1I* indicates a lower-power (1.0V core voltage) device with a -1 speed grade in an industrial operating range package.
	2C-xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	2C-ES	The *ES* indicates an Engineering Sample.