PCB Quality Metrics that Drive Reliability (PD 18)

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Information may be changed or updated without notice.

PDC Outline

Section 0: Intro

Section 1: What is reliability and root cause?

Section 2: Overview of failure mechanisms

Section 3: Failure analysis techniques

- **Non-destructive analysis techniques**
- **Destructive analysis**
- **Materials characterization**

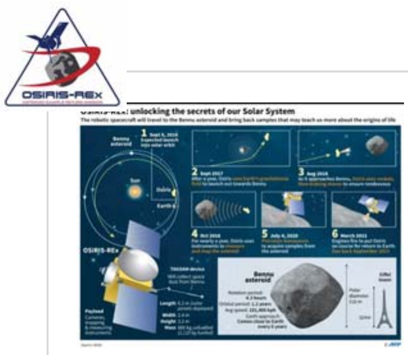
Section 4: Summary and closure

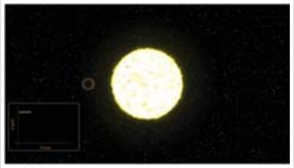
Discussions and case studies of actual failures and subsequent analysis.

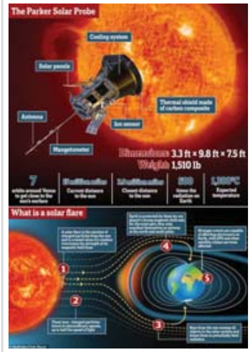
About Me

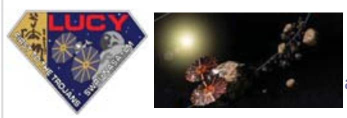
- Member of ~40 IPC Subcommittees and Task Groups. Chair IPC-7092: Design and Assembly Process Implementation for Embedded Components.
- Member of IPC A-Teams
  - ✓ Microvia Weak Interfaces
  - ✓ J-STD-001 X-ray Requirements
  - ✓ IPC-6017 Embedded Circuits Spec
- NRL/CALCE/NASA
- Bachelors/Masters/PhD Metallurgy, Electronics Materials, Risk/Reliability

1. 1-10C Test Coupon and Artwork Generation Task Group
2. 3-11 Laminate Prepreg Materials Subcommittee
3. 3-11G Corrosion of Metal Finishes Task Group
4. 3-12D Woven Glass Reinforcement Task Group
5. 3-12E Base Materials Roundtable Task Group
6. 4-14 Plating Processes Subcommittee
7. 4-33 Halogen-Free Materials Subcommittee
8. 5-21F Ball Grid Array Task Group
9. 5-21H Bottom Termination Components (BTC) Task Group
10. 5-21M Cold Joining Press-fit Task Group
11. 5-22A J-STD-001 Task Group
12. 5-22A-SKELETON J-STD-001 X-Ray Requirements
13. 5-22ARR J-STD-001 Conformal Coating Material & Application Industry Assessment
14. 5-22AS J-STD-001 Space Electronic Assemblies Task Group
15. 5-24B Solder Paste Task Group
16. 5-32A Ion Chromatography Ionic Conductivity Task Group
17. 5-32B SIR and Electrochemical Migration Task Group
18. 5-32E Conductive Anodic Filament (CAF) Task Group
19. 6-10C Plated-Thru Via Reliab.-Accelerated Test Methods
20. 7-12 Microsection Subcommittee
21. 7-23 Assembly Process Effects Handbook Subcommittee
22. 7-24 Printed Board Process Effects Handbook Subcommittee
23. 7-24A Printed Board Process Effects Handbook Task Group
24. 7-31FS IPC WHMA-A-620 Space Electronic Assemblies Addendum Task Group
25. 7-32C Electrical Continuity Testing Task Group
26. 6-10D SMT Attachment Reliability Test Methods TG
27. D-55A Embedded Circuitry Guideline Task Group
28. B-11 3-D Electronic Packages Subcommittee
29. D-13 Flexible Circuits Base Materials Subcommittee
30. D-22 High Speed High Frequency Board Performance Sub-committee
31. D-24C High-Frequency Test Methods Task Group Frequency-Domain Methods
32. D-31B IPC-2221 2222 Task Group
33. D-32 Thermal Stress Test Methodology Subcommittee
34. D-33A Rigid Printed Bd. Performance Specifications TG
35. D-33AS IPC-6012 Aerospace Addendum Task Group
36. D-35 Printed Board Storage and Handling Subcommittee
37. D-55 Embedded Devices Process Implementation Subcommittee
38. D-55-AT IPC-6017A A-Team
39. V-TSL-MVIA-CHEMPR-AT Chemical Processes and Metallurgy A-Team
40. V-TSL-MVIA-SIMMOD-AT Simulation and Modeling A-Team

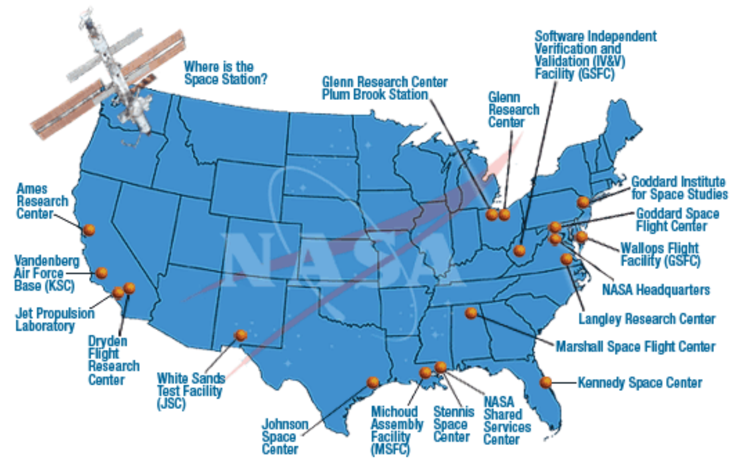








Explore some of the solar system's oldest bodies, a series of asteroids known as the "Trojans



NASA GSFC One World-Class Organization

What makes Goddard one-of-a-kind?

NASA's ***leading science center****, with* ***cross-disciplinary, end-to-end*** *capabilities*

Goddard SPACE FLIGHT CENTER

Executing NASA's **most complex missions**

World leader in ***understanding the Sun's impact on Earth***

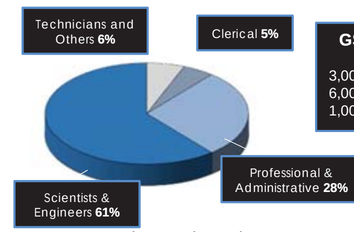
Independent Verification and Validation Facility ***assures NASA's most complex software functions as planned***

Communications backbone *– 98% of NASA's data is transmitted via Goddard infrastructure*

1 of 2 US routes for ISS cargo; *1 of 4 US orbital launch facilities*

Who We Are

THE GODDARD COMMUNITY
More than 10,000 People



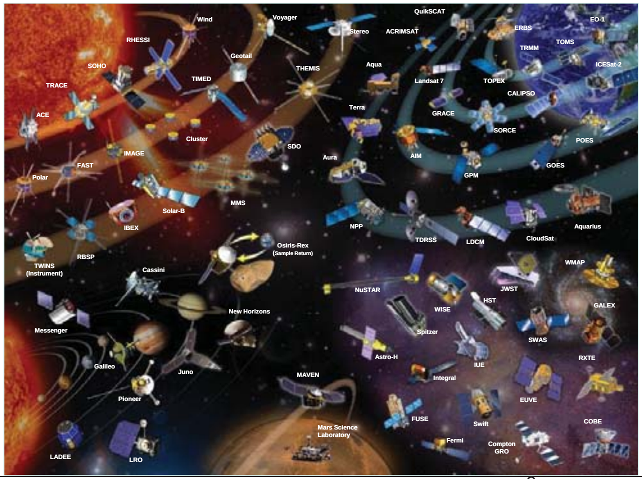
GSFC Workforce

3,000+ Civil Servants
6,000+ Contractors
1,000s of Others*

The Nation's largest community of
scientists, engineers, and technologists

*Including off-site contractors, interns, and Emeritus

GSFC: A Diverse Mission Portfolio



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What is Reliability?

Reliability is the ability of a product to properly function, within specified performance limits, for a specified period of time, under the life cycle application conditions

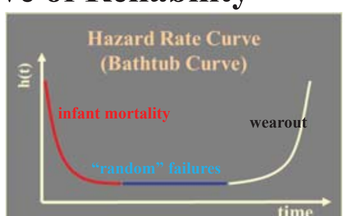
– Within specified performance limits: A product must function within certain tolerances in order to be reliable.

– For a specified period of time: A product has a useful life during which it is expected to function within specifications.

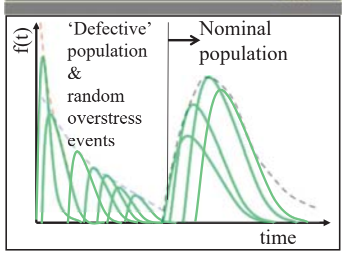
– Under the life cycle application conditions: Reliability is dependent on the product's life cycle operational and environmental conditions.

Physics of Failure Perspective of Reliability

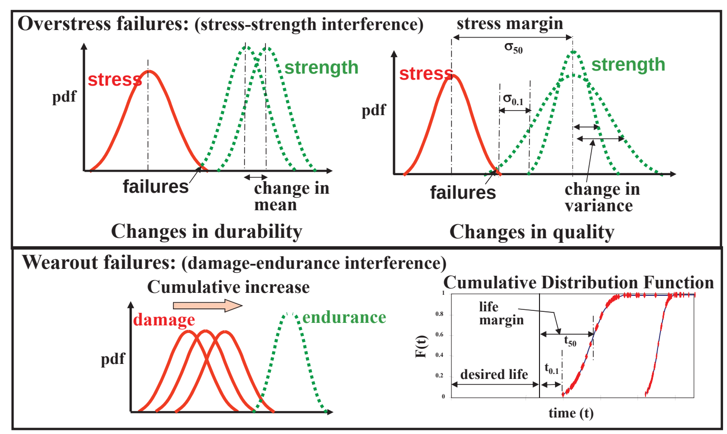
Reliability statisticians are interested in tracking system level failure data during the service life for logistical purposes, and in determining how the hazard rate curve looks.



- PoF reliability engineers are interested in understanding and controlling the individual failures that cause the curve.
- PoF engineers do so through systematic and detailed assessment of
  - influence of hardware configuration and life-cycle stresses…
  - on root-cause failure mechanisms…
  - in the materials at potential failure sites.



Influence of 'Durability' and 'Quality' on 'Reliability'



When a Product Fails, There Are Costs . . .

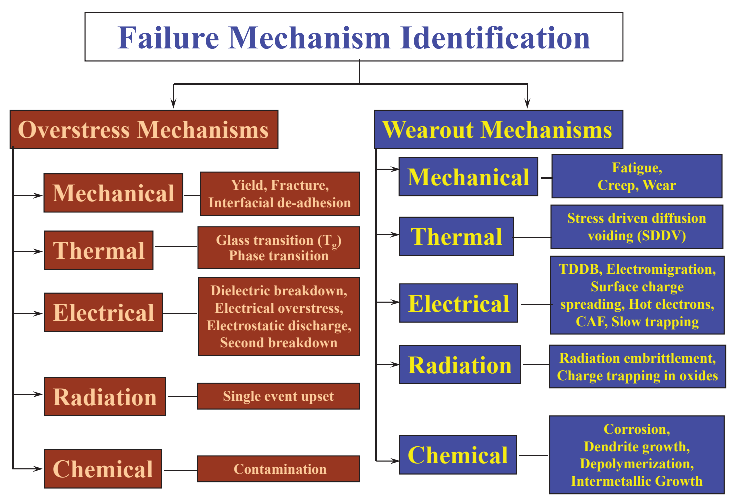
- To the Manufacturer
  - Time-to-market can increase
  - Warranty costs can increase
  - Market share can decrease. Failures can stain the reputation of a company, and deter new customers.
  - Claims for damages caused by product failure can increase
- To the Customer
  - Personal injury
  - Loss of mission, service or capacity
  - Cost of repair or replacement
  - Indirect costs, such as increase in insurance, damage to reputation, loss of market share

Failure Definitions

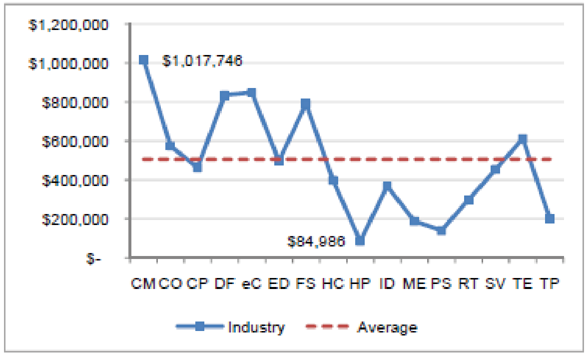
Failure	A product no longer performs the function for which it was intended
Failure Mode	The effect by which a failure is observed.
Failure Site	The location of the failure.
Failure Mechanism	The physical, chemical, thermodynamic or other process that results in failure.
Failure Model	Quantitative relationship between lifetime or probability of failure and loads
Load	Application/environmental condition needed (electrical, thermal, mechanical, chemical...) to precipitate a failure mechanism.

Classification of Failures

- It is helpful to distinguish between two key classes of failure mechanism:
  - *overstress*: use conditions exceed strength of materials; often sudden and catastrophic
  - *wearout*: accumulation of damage with extended usage or repeated stress
- It is also helpful to recognize early life failures:
  - *infant mortality*: failures occurring early in expected life; should be eliminated through process control, part selection and management, and quality improvement procedures



Cost of a Single Unplanned Data Center Outage Across 16 Industries

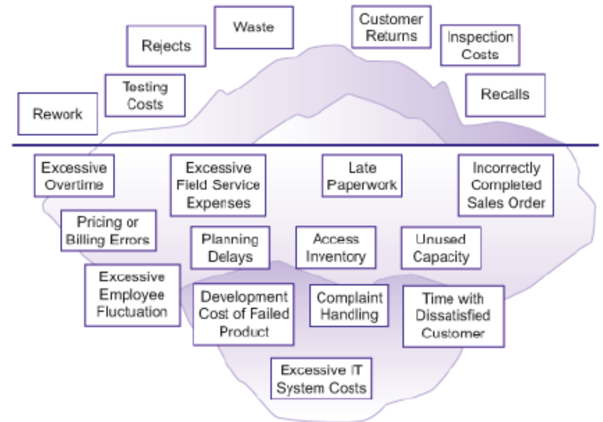


Industry	Code
Communication	CM
Co-location	CO
Consumer	CP
Defense	DF
eCommerce	eC
Education	ED
Financial	FS
Healthcare	HC
Hospitality	HP
Industrial	ID
Media	ME
Public sector	PS
Retail	RT
Services	SV
Technology	TE
Transportation	TP

The average cost of data center downtime across industries was approximately **$5,600 per minute.**

Ref: Ponemon Inst., "Calculating the Cost of Data Center Outages," Feb. 1, 2011.

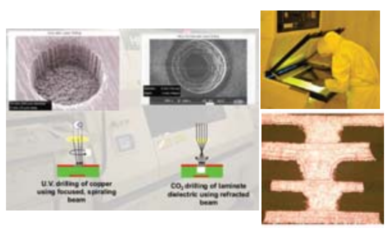
Iceberg Model of Cost of Poor Quality

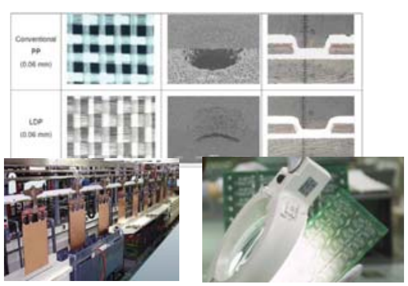


Ref: A. Buthmann, "Cost of Quality: Not Only Failure Costs," iSixSigma.

Quality Assurance Functions

- In today's compressed development cycles where rapid and cost-effective testing and analysis are key, a properly designed and executed quality assurance function (with appropriate reliability analysis) can enable products with robust design margins.





- If the mission conditions are not well understood or the reliability analysis and accelerated testing are not conducted right, cost and schedule impacts, along with unexpected failures will add risk to a Project development cycle.

SOURCE: Industrial Laser Solutions. PCBShop.org

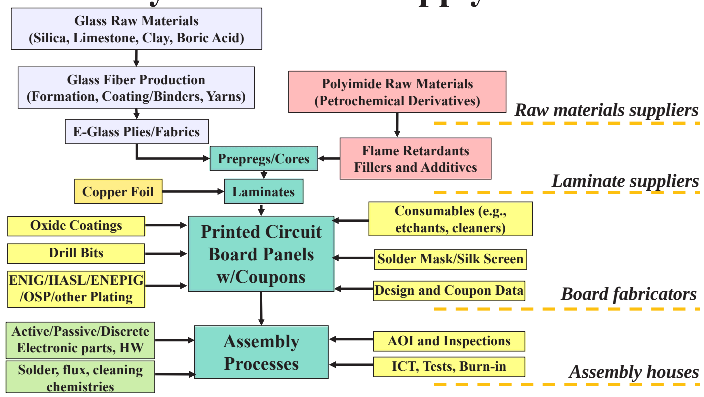
Printed Circuit Boards and Classification

- Printed circuit boards are the baseline in electronic packaging – they are the interconnection medium upon which electronic components are formed into electronic systems.
  - PCB materials are generally glass reinforced organic polyimide (epoxy, BT, ceramic are also used).
- Classified on the basis of
  - Dielectrics used
  - Reinforcement
  - Circuit type
  - Component types
  - Board construction
  - Design complexity

Examples of Bare PCBs

Populated PCBA

Polyimide PCBA Supply Chain*



* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." *Wiley Encyclopedia of Composites* (2011).

Major Constituents of Laminates*

Constituent	Major function (s)	Example material (s)
Reinforcement	Provides mechanical strength and electrical properties	Woven glass (E-grade) fiber
Coupling agent	Bonds inorganic glass with organic resin and transfers stresses across the structure	Organosilanes
Matrix	Acts as a binder and load transferring agent	Polyimide
Curing agent	Enhances linear/cross polymerization in the resin	Dicyandiamide (DICY), Phenol novolac (phenolic)
Flame retardant	Reduces flammability of the laminate	Halogenated (TBBPA), Halogen-free (Phosphorous compounds)
Fillers	Reduces dissipatation (high frequency), thermal expansion and cost of the laminate	Silica, Aluminum hydroxide
Accelerators	Increases reaction rate, reduces curing temperature, controls cross-link density	Imidazole, Organophosphine

* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." *Wiley Encyclopedia of Composites* (2011).

Example: The Glass Treatment Story *

Glass Weave Style

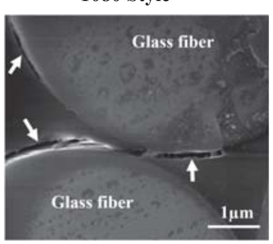
1080 Style

Glass Weave Style

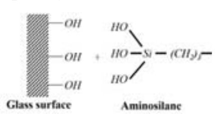
2116 Style

Glass Weave Style

7628 Style



Fiber/resin interphase delamination occurs due poor glass treatment.



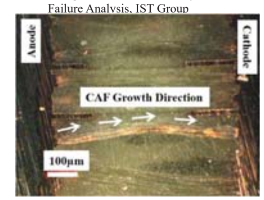
* - Sood, Bhanu, and Michael Pecht. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." *Microelectronics Reliability* (2017).

Printed Circuit Boards Continue to Cause Headaches

- PCB vendors continue to provide high performance materials which are represented to be resistant to conductive anodic filament (CAF), fiber pullout and laminate cracking.
- Yet, PCB quality and reliability continues to suffer due to failures attributed to poor glass/resin adhesion leading to CAF.
- High rates of non-conformances carrying high risk lead to multiple rebuilds causing impactful schedule delays.

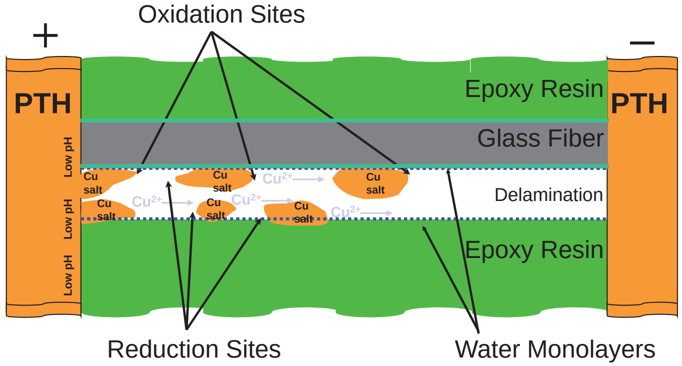
Halogen-free PCB Reliability Test and Failure Analysis, IST Group

Hu, Chaohui. "Study on the factors which affecting the conductive anodic filament reliability for packing substrate." Electronic Packaging Technology (ICEPT), 2017 18th International Conference on. IEEE, 2017.



Sood, Bhanu, and Pecht, Michael. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." Microelectronics Reliability 82 (2018): 235-243.

Formation of Conductive Filaments [1] [2]



CAF is a two step process: $t_{failure} = t_1 + t_2$ $t_1 >> t_2$

t_1 - time for glass/epoxy degradation, t_2 - related to rate of electrochemical reaction

[1]. Rogers, Keith Leslie. An analytical and experimental investigation of filament formation in glass/epoxy composites. Diss. 2005.
[2]. Sood, Bhanu, and Pecht, Michael. "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602.

Glass Fibers and Sizing Agents

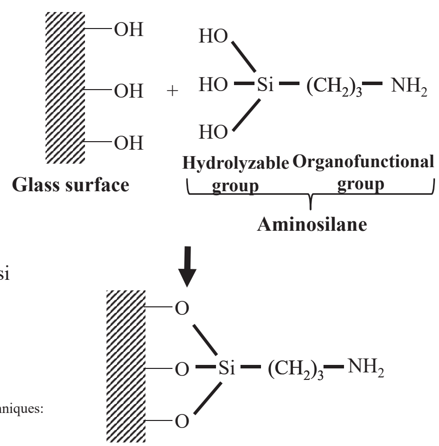
- Coupling agents are part of the sizings, they are functionally graded materials that act as adhesion promoters. [1] [2] [3]
  - Sizing agents are typically composed of antistats, lubricant, surfactant, silanes and film formers.
  - Silane act as molecular bridges between two chemically different materials (glass and epoxy matrix).
  - Organo-functional group bonds to the organic resin and inorganic groups bond to the glass surface.
- Sizing formulation chemistries and their proportions are closely held by glass suppliers and PCB suppliers

  "…we are not allowed to discuss any sizing or glass chemistry related topics outside by company policy. Hope for your understanding…" – Senior Staff Scientist, PPG Glass.
- Optimizing the sizing layer is a complex art involving a compromise of manufacturing, marketing, technical and economic factors.

[1]. Mishra, Debasmita, and Alok Satapathy. "An investigation on the dielectric properties of epoxy filled with glass micro-spheres and boron nitride." (2012).
[2]. Mack, H. Choosing the Right Silane Adhesion Promoters for SMP Sealants, Adhesive and Sealant Council Meeting, Orlando, Fl, Spring 2001. Gelorme, J. D., & Kuczynski, J. (2010).
[3]. U.S. Patent Application No. 12/694,005.

Coupling Agents Used in FR4[1] [2]

- Dow Corning, BGF, Gelest are key suppliers.
- Main silane types are:
  - Aminosilanes
  - Epoxy Silanes
  - Vinyl Silanes
  - Methacryl Silanes
  - Alkylsilane
  - Phenyl Silane
  - Chlorosilane
- Dow Corning Z-6032 tends to dominate the market (Vinylbenzylaminoethylaminopropyltrimethoxysilane).
- Not all supply chains re-validate compatibility with changes in resin [2].

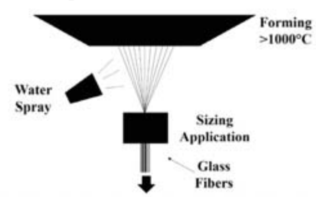


[1] Mittal, K. L., & Pizzi, A. (Eds.). (1999). Adhesion Promotion Techniques: Technological Applications. CRC Press.
[2] Scott Crane (personal communication, November 26, 2018).

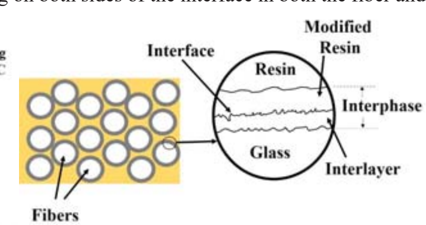
Resin-Glass Interface/Interphase [1] [2]

The region between the glass and resin is a three-dimensional region between the bulk fiber and bulk resin, this includes:

- Area of contact (interface) between the fiber and the matrix
- Region of some finite thickness extending on both sides of the interface in both the fiber and resin matrix (interphase).



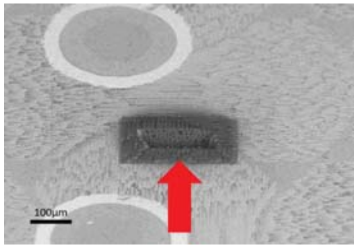
Sizing Application

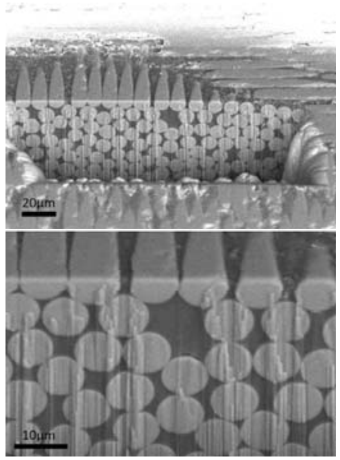


Glass-resin interphase [2]

[1] Drzal, Lawrence T., Michael J. Rich, and Pamela F. Lloyd. "Adhesion of graphite fibers to epoxy matrices: I. The role of fiber surface treatment." The Journal of Adhesion 16.1 (1983): 1-30.
[2] Petersen, Helga Nørgaard, et al. Investigation of sizing-from glass fibre surface to composite interface. Diss. DTU Nanotech, 2017.

FIB Experiments

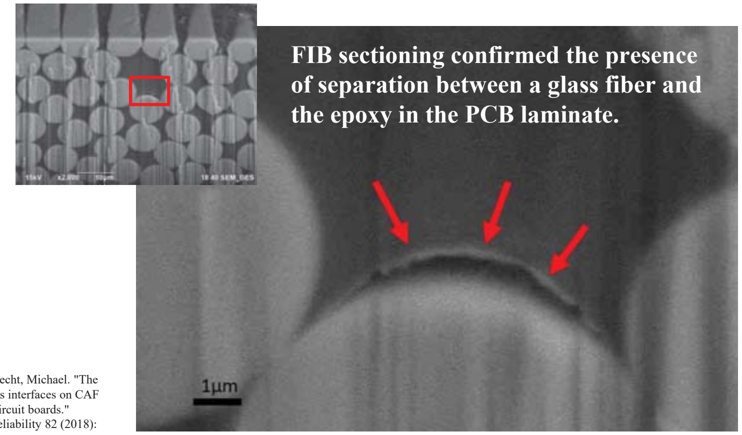




- FIB removes the glass fibers selectively from the earlier mechanical planar microsection.
- Beams with successively lower currents are then used to trim the face of the cut until the interphases of interest are imaged in the SEM.
- Slight adjustments in the position of each trim cut are made based on observation of the progress.

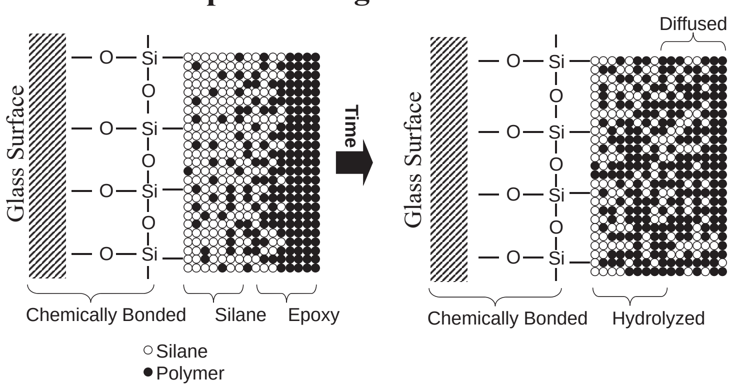
Sood, Bhanu, and Pecht, Michael. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." Microelectronics Reliability 82 (2018): 235-243.

FIB Sections – Glass/Resin Separation



Sood, Bhanu, and Pecht, Michael. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." Microelectronics Reliability 82 (2018): 235-243.

Inter-penetrating Networks [1] [2] [3]

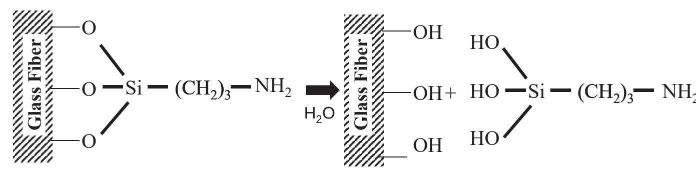


1. Sood, B., & Pecht, M. (2017). The effect of epoxy/glass interphases on CAF failures in printed circuit boards. Microelectronics Reliability.

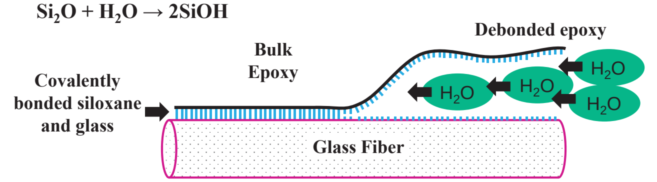
2.Tomlin, Andrew Dermot. "Self-sensing composites: cure monitoring." (2010).

3.Halvorson, Rolf H., Robert L. Erickson, and Carel L. Davidson. "The effect of filler and silane content on conversion of resin-based composite." Dental Materials 19.4 (2003): 327-333.

Hydrolysis of Siloxane Bonds

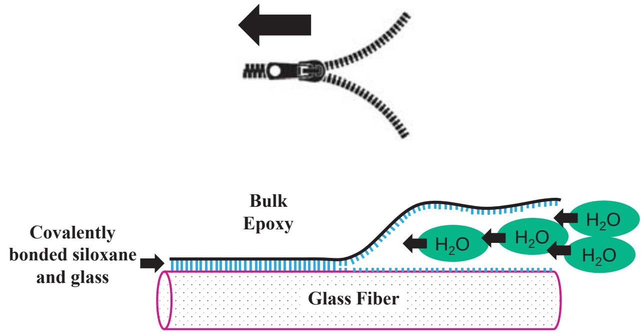


$$Si_2O + H_2O \rightarrow 2SiOH$$



As the PCBs absorb moisture and combined with the residual stresses at the glass-resin interphase, the hydrolysis reaction at the interphase between the glass and resin drives an "unzipping" of the bonded region.

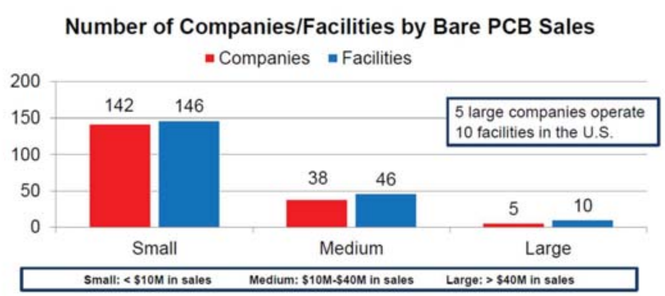
Results of the Hydrolysis



Printed Circuit Board Supplier Capability Overview

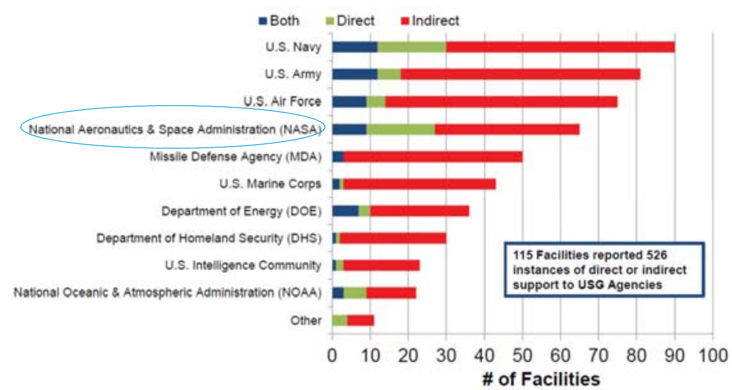
Bare PCB Suppliers*

185 companies operate 202 bare printed circuit board manufacturing facilities in the U.S. - 2015



** - "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.*

Support to U.S. Government Agencies*



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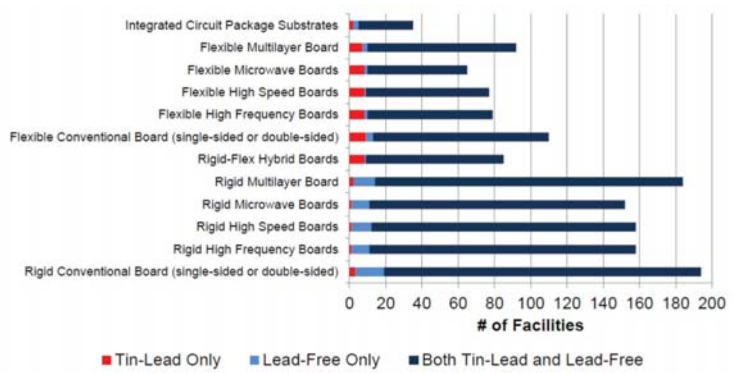
Bare PCB Supplier Capabilities*



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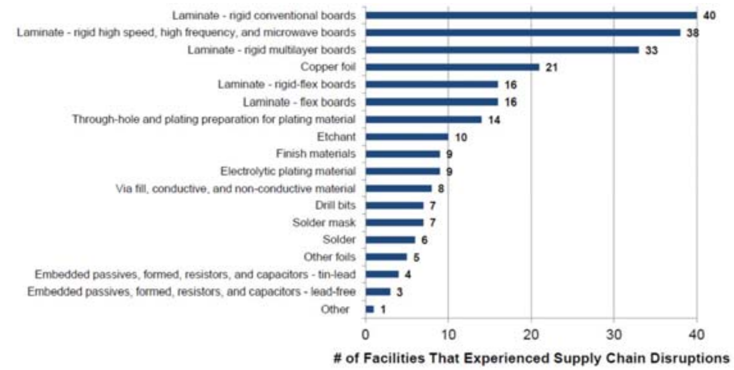
Material Supply Chain Disruptions*



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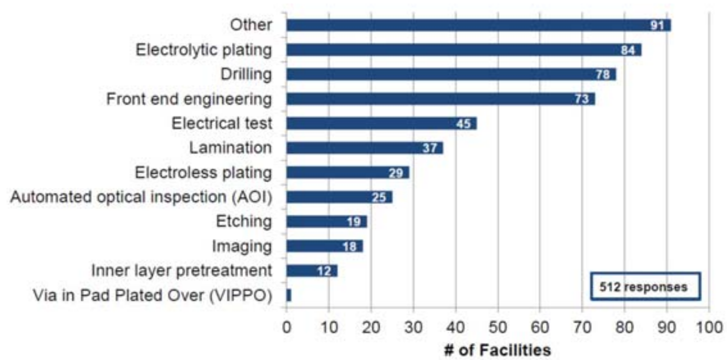
Factors Causing PCB Production Bottlenecks*



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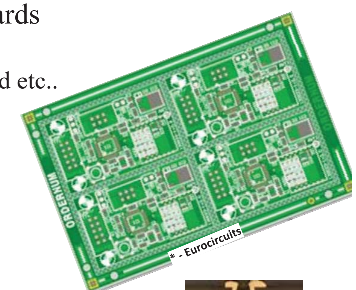
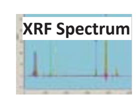
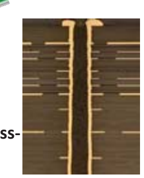
PCB Quality

- In a vast majority of cases, NASA uses IPC standards (e.g., IPC-6012, 6013)
  - IPC-6012 for rigid, IPC-6013 flex, IPC-6018 high speed etc..
- Inspection include:
  - Microsection evaluation (coupons)
  - Surface finish evaluation (coupons)
- Test include:
  - External visual examination
  - Electrical continuity and isolation
  - Solderability (not 100% cases)
  - Cleanliness
    - In some cases MIL, ESA or "in-house" standards are applied.







PTH in Cross-section

Significance of Printed Circuit Board Requirements

- The requirements and coupons are a “front door”.
- Examples:
  - Internal Annular Ring:
    - Egregious violations indicate there may have been a serious problem in development of the board (layup or lamination).
    - Other NCs don’t indicate any risk at all (example: application of IPC-6012 Rev B. v/s IPC-6012 Rev. D)
  - Negative etchback v/s positive etchback:
    - Modern cleaning processes and flight experience result in equal reliability with both etchback conditions or no etchback.
  - Wicking of copper:
    - Requirements are conservative based on broad statistics.
    - A basic analysis of the board layout can indicate directly if there is risk or not, regardless of requirements violations.

PCB Supplier Evaluation Study

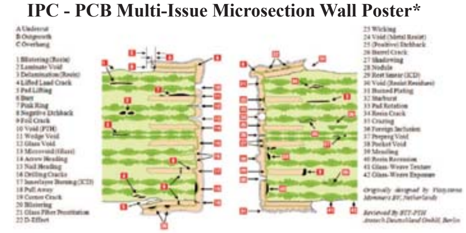
Study Objective

- Evaluate a subset of GSFC PCB suppliers (direct or indirect) and corresponding PCB coupon microsection testing data.
- Develop a methodology for data generation and collection to provide trend analysis
  - Identifies/predicts violation of a process limit criteria (in case of an egregious NC).
- Provide analysis for severity categories of the nonconformance.
- Provide recommendations to the suppliers (i.e. supplier quality engineering, continuous process monitoring, quality metrics definition).

Microsectioning

- Suppliers perform microsectioning and inspect per specifications.
- Secondary GSFC independent microsection analysis yielded 20-30% inspection rejects, caused by:
  - Screening escapes:
    - Test sample quality not consistent
    - Supplier microsection process, inadequate coupons
  - Requirement interpretations
  - Requirements flow-down issues
    - Alternative specifications (MIL, ECSS)
    - Buying heritage and off-the-shelf designs

IPC - PCB Multi-Issue Microsection Wall Poster*



* - https://blog.ipc.org/2010/11/22/pcb-multi-issue-microsection-wall-poster/

Requirements, Nonconformance, Data Generation and Collection

- Present study evaluates only the microsections performed by GSFC.
  - PCB coupon microsection evaluation in accordance to IPC Standard (IPC-6018B Class 3, IPC-6012C Class 3/A).
  - Coupon evaluation reports were generated, identified non-conformances.
- All PCB coupon testing results from all GSFC suppliers were recorded for 3 years (from 2015 – 2017):
  - Data include nonconformance and conformances in accordance with IPC Standards.
  - Total number of data points are approximately 882 jobs.
  - Each job has number of nonconformance with different severity.

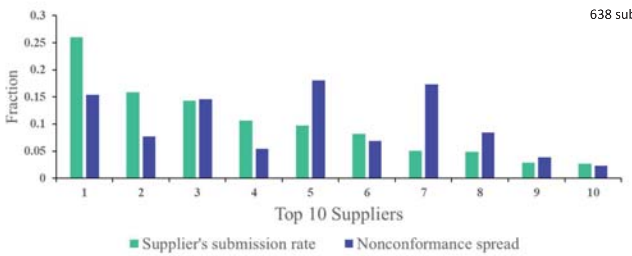
Study Methodology

- Since 2015, received and analyzed 882 PCB coupon submissions from PCB suppliers.
- Top ten suppliers sent 638 submissions.
- Total nonconformance observed: 260

- For each supplier, analyzed nonconformance (s)
  - Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
  - Classifying and analyzing top 5 severity categories.

Data Analysis –Submission and Nonconformance for Supplier

638 submissions



$$\text{Supplier submission rate} = \frac{\text{total submission by individual supplier}}{\text{total submission by all suppliers}}$$

$$\text{Nonconformance spread} = \frac{\text{total nonconformance by individual supplier}}{\text{total nonconformance by all suppliers}}$$

Classification and Analysis - Top 5 Nonconformances

Twenty one distinct conformances observed among the ten suppliers

NC	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greather than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminate cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess of 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil	IPC 6012B Class 3/A
T	Dielectric thickness less than 3.0 mil min	IPC 6012B Class 3/A
U	Laminate void greater than 3.0 mil	IPC 6012B Class 3/A

Common Nonconformances from suppliers

← PCB Suppliers →									
1	2	3	4	5	6	7	8	9	10
A	F	E	K	A	N	E	E	A	E
B	G	D	F	F	O	P	A	F	F
C	H	B	L	D	F	C	D	S	T
D	A	I	J	J	E	D	F	D	U
E	D	J	A	M	P	Q	R	P	R

Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to implement techniques which may eliminate theses nonconformances fro[m] at least 7 suppliers.

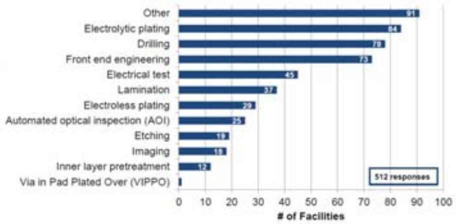
(A) Inner layer separations/inclusions

(D) Separation/inclusions between plating layers

(E) Copper wicking in excess of 2.0 mil

(F) Internal annular ring less than 2.0 mil

(J) ENIG is less than the minimum requirements



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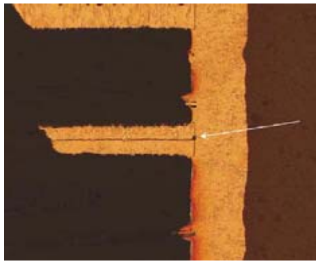
Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in an area where it is not expected.



Risk: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

Inner Layer Separations or Inclusions

Contributors

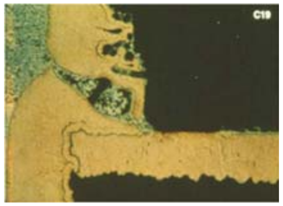
- Improper lamination press or cure cycles whether it be pressure, time, temperature.
- Others include inadequate coverage of inner layer oxide, moisture not completely removed in pre-lamination bake cycle.
- Bad batch of prepreg and or laminate.
- Post-electroless copper cleaning residues, contaminated pretreatment prior to electrolytic plating, or an out-of-control electrolytic copper process.

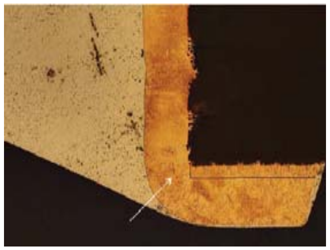
Resolution

- Consistency in drilling processes.
- Reduce the resin content in the stack up.
- Good desmear, with adequate texture.
- Provide adequate copper border for support and resin venting

Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating layer and foil.





Risk: intermittent electrical open or complete opens due to mechanical or thermal stresses.

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

Separation or Inclusions Between Plating Layers

Contributors

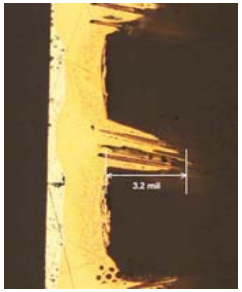
- Incomplete wrap plating
- Overly-aggressive cleaning process
- Insufficient cleaning

Resolution

- Adjust plating parameters
- Optimize cleaning processes

Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.



Risk: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.

1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Copper Wicking in Excess of 2.0 mil

Contributors

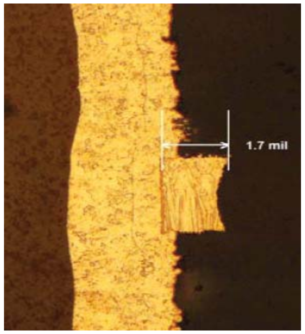
- Dull drill bits or broken drill bits that causes a crack in the laminate.
- Incompatible laminate material
- Insufficient glass etch.
- Poor glass to organic adhesion.

Resolution

- Optimize desmear parameters
- Improve drilling operation (feed and speed).
- Ensure sufficient resin wet-out of glass fibers (siloxane treatment).

Internal Annular Ring Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.



Risk: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.

1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards", Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Internal Annular Ring Less Than 2.0 mil

Contributors

- Drilled-hole pattern not matching the lands on the internal layers (Misregistration).
- Lamination process.
- Prelamination treatments that involve scrubbing or bending may stretch the thin laminate, which will then shrink after it is etched and baked dry.
- Application of specification or drawing notes.

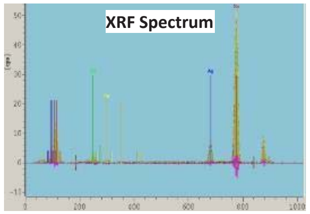
Resolution

- Better material selection of laminate, improved cleanliness, and reduction in the amount of volatiles.
- Confirm whether or not it is operator error.
- Update drawing notes to bring the notes in line with current industry maturity levels.

ENIG (Au or Ni) Less than the Minimum

Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (118 micro-inches for Ni and 2 micro-inches for Au).

Risk: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.



1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

ENIG Less than Minimum

Contributors

- Improper cleaning of surfaces.
- Improper or inadequate rinsing.
- Bath parameters not being followed (pH and chemical).
- Bath temperature too low.
- Copper surface not clean of oil or inhibiting film.

Resolution

- Re-clean copper using chemical cleaners or mechanical
- scrubbing Institute micro-etch step to improve cleaning
- Improve rinsing(Check flow, agitation and water quality)
- Raise temperature per supplier specifications
- Readjust to supplier operational parameters

Summary - PCB Supplier Study

- The test data is analyzed using statistical method to provide trend analysis for all suppliers.
  - Root cause(s) and key contributors are identified.
  - Mitigation plan is included for the root cause of nonconformance.
- Provide recommendations to the supplier's process, identification and prediction of nonconforming process limit criterion, and to improve test standards.
- New technologies (example: smaller annular rings, via-in-pads, thinner laminates or newer plating) are implemented on the basis of supplier maturity and reported NCs.

Failure Analysis

What Causes Products to Fail?

Generally, failures do not "just happen."

Failures may arise during any of the following stages of a product's life cycle:

- → Product design
- → Manufacturing
- → Assembly
- → Screening
- → Testing
- → Storage
- → Packaging
- → Transportation
- → Installation
- → Operation
- → Maintenance

The damage (failure mode) may not be detected until a later phase of the life cycle.

What is Root Cause Analysis?

Root Cause analysis has four major objectives:

- Verify that a failure occurred;
- Determine the symptom or the apparent way a part has failed (the mode);
- Determine the mechanism and root cause of the failure;
- Recommend corrective and preventative action.

While generally synonymous, "Failure analysis" is commonly understood to include all of this except determination of root cause.

What is a Root Cause?

The root cause is the most basic causal factor or factors that, if corrected or removed, will prevent the recurrence of the situation.*

The purpose of determining the root cause(s) is to fix the problem at its most basic source so it doesn't occur again, even in other products, as opposed to merely fixing a failure symptom. Identifying root causes is the key to preventing similar occurrences in the future.

Ref: ABS Group, Inc., *Root Cause Analysis Handbook, A Guide to Effective Incident Investigation*, ABS Group, Inc., Risk & Reliability Division, Rockville MD.

Root Cause Analysis is Different from Troubleshooting

- Troubleshooting is generally employed to eliminate a symptom in a given product, or to identify a failed component in order to effect a repair.
- Root cause analysis is dedicated to finding the fundamental reason why the problem occurred in the first place, to prevent future failures.

From Symptoms to Root Causes

- **Symptoms** are manifestations of a problem; signs indicating that a failure exists.
  - Example: a symptom of printed circuit board failure could be the measurement of open circuits after fabrication.
- **An apparent cause (or immediately visible cause)** is the superficial reason for the failure.
  - Example: the apparent cause of open circuits could be that traces have discontinuities that result in open circuits.
- **Root Cause** is the most basic casual factor(s).
  - Example: the root cause could arise during the manufacturing process if the circuit boards are stacked improperly, resulting in scratches to circuit traces. Another possible root cause could be the presence of contaminants during the copper trace etching process, which resulted in discontinuities in the traces.

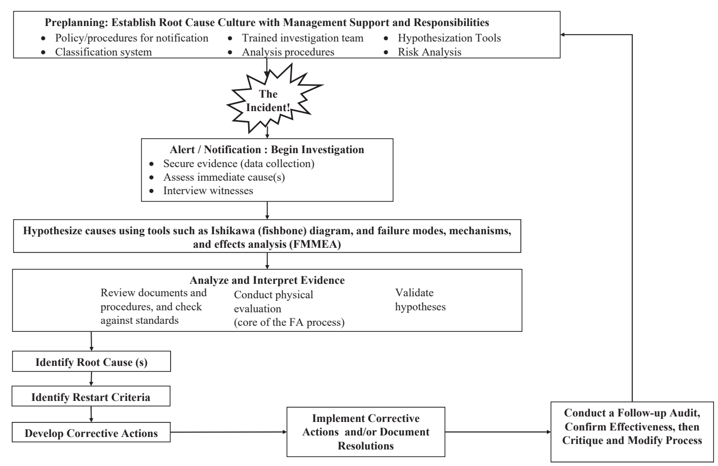
Root Cause Analysis

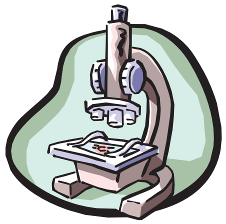
- Root cause analysis is a methodology designed to help:

  1) Describe WHAT happened during a particular occurrence,
  2) Determine HOW it happened, and
  3) Understand WHY it happened.

- Only when one is able to determine WHY an event or failure occurred, will one be able to determine corrective measures, and over time, the root causes identified can be used to target major opportunities for improvement.
- Uncovering ROOT CAUSE may require 7 iterations of "Why?"

Root Cause Analysis Process





Hypothesizing Causes

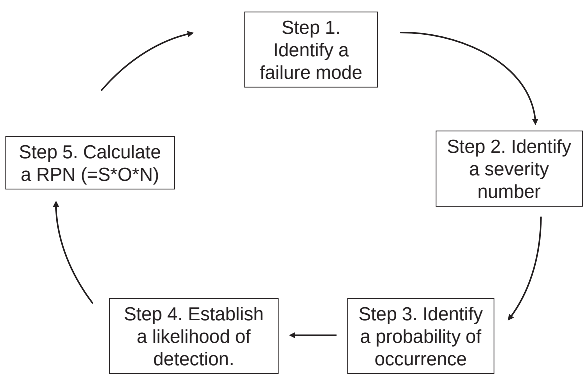
Hypothesizing causes is the process of applying knowledge of risks associated with a product's design and life cycle to the data gathered about the failure event, in order to postulate a root cause.

- Tools for hypothesizing causes:
  - Failure modes, and effects analysis (FMEA)
  - Fault tree analysis (FTA)
  - Cause and effect diagram – Ishikawa diagram (fishbone analysis)
  - Pareto analysis

Tools for Hypothesizing Root Causes

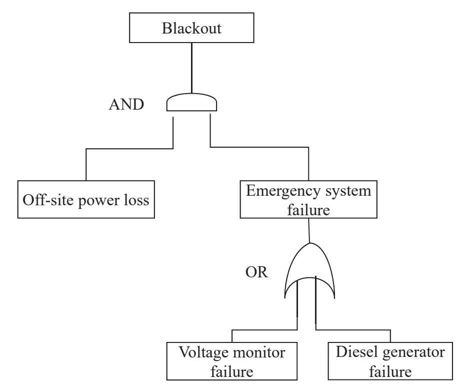
FMEA Methodology

- Failure modes and effects analysis is an approach for identifying all possible failures in a design, a manufacturing or assembly process, or a product or service.
- Knowledge of stresses is combined with failure models to **prioritize failure mechanisms** according to their severity and likelihood of occurrence.

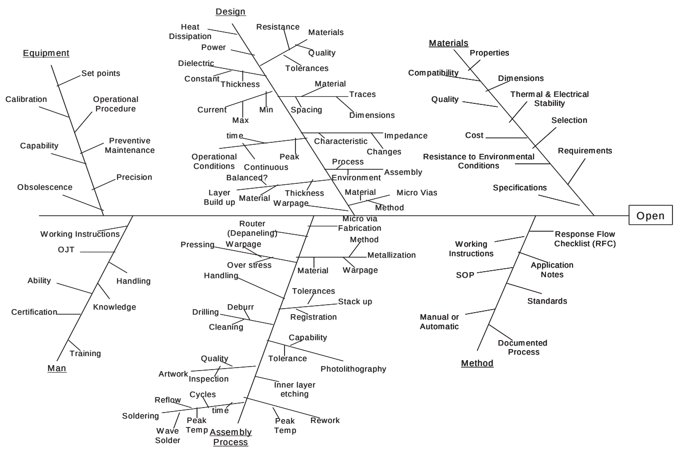


Fault Tree Analysis

- In contrast with the "bottom up" assessment of FMEA, fault-tree is a "top down" analysis that starts qualitatively to **determine what failure modes can contribute to an undesirable top level event**.
- It aims at developing the structure from which simple logical relationships can be used to express the probabilistic relationships among the various events that lead to the failure of the system.

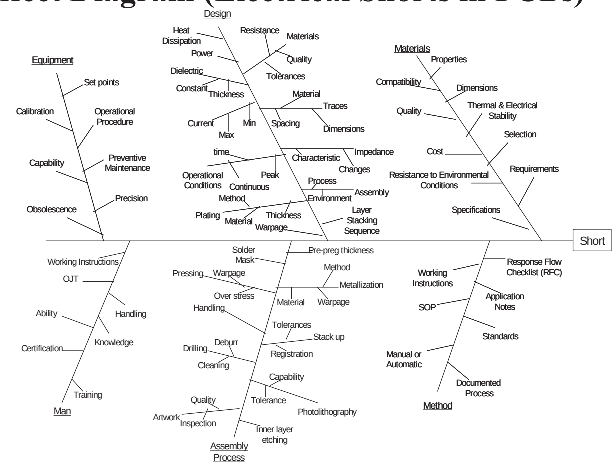


Cause and Effect Diagram (Electrical Opens in PCBs)



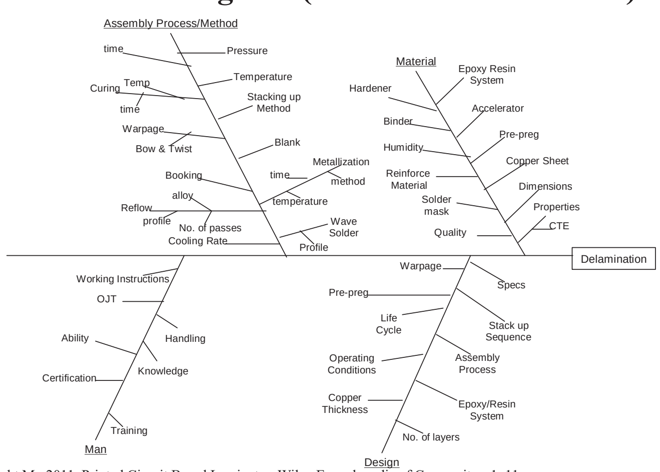
Ref: Coombs C. F. "Printed circuits handbook." Printed Circuits Handbook. McGraw-Hill Professional Publishing (2007).

Cause and Effect Diagram (Electrical Shorts in PCBs)



Ref: Sood B., and Pecht M., 2011. Printed Circuit Board Laminates. Wiley Encyclopedia of Composites. 1–11.

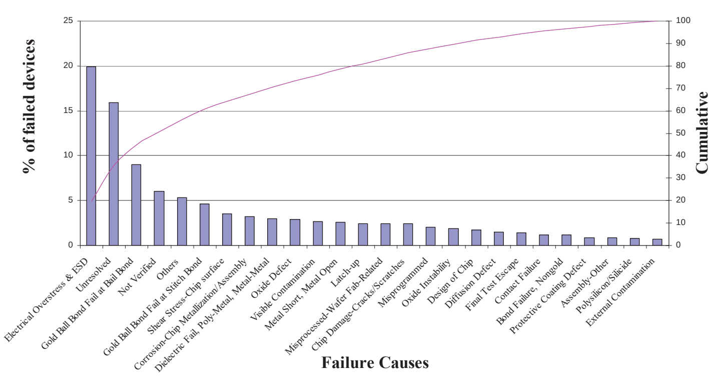
Cause and Effect Diagram (Delamination in PCBs)



Ref: Sood B., and Pecht M., 2011. Printed Circuit Board Laminates. Wiley Encyclopedia of Composites. 1–11.

Pareto Chart Example

- Failure Causes in Electronic Devices -



Ref: Pecht M. and V. Ramappan: "Review of Electronic System and Device Field Failure Returns," *IEEE Transactions on CHMT*, Vol. 15, No. 6, pp. 1160-1164, 1992.

Collecting Supporting Evidence

- Even if a root cause has been hypothesized, additional evidence is often required to assess (i.e., prove or invalidate) the hypotheses formulated.
- Evidence can be gathered by
  – undertaking sample physical evaluation.
  – reviewing documents and procedures against standards, and
  – interviews

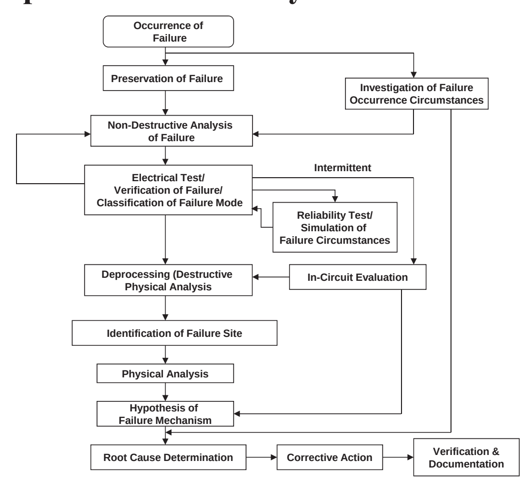
Analysis and Interpretation of Evidence

- Reviewing in-house procedures
  – (e.g., design, manufacturing process, procurement, storage, handling, quality control, maintenance, environmental policy, safety, communication or training procedures)
- …against corresponding standards, regulations, or part- and equipment vendor documentation
  – (e.g., part data sheet and application notes, equipment operating and maintenance manuals)
- ….can help identify causes such as misapplication of equipment, and weakness in a design, process or procedure.
  – Example 1: misapplication of a component could arise from *its use outside the vendor specified operating conditions* (e.g., current, voltage, or temperature).
  – Example 2: equipment (e.g., assembly, rework or inspection equipment) misapplication can result from *uncontrolled modifications or changes* in the operating requirements of the machine.
  – Example 3: a defect may have been introduced due to *misinterpretation* of poorly written assembly instructions.

General Approach Used for Failure Analysis

- The overriding principle of failure analysis is to *start with the least destructive methods and progress to increasingly more destructive techniques.*
- The potential for a nominally non-destructive technique to cause irreversible changes should not be underestimated.
  – For example, the simple act of handling a sample, or measuring a resistance, can cause permanent changes that could complicate analysis further down the line.
- Each sample and failure incidence may require a unique sequence of steps for failure analysis. The process demands an *open mind*, *attention to detail*, and a *methodical approach*.

Example of Failure Analysis Process Flow



Non-Destructive Testing (NDT)

- Visual Inspection
- Optical Microscopy
- X-ray imaging
- X-ray Fluorescence Spectroscopy

- Acoustic microscopy
- Residual gas analysis
- Hermeticity Testing

External Inspection

- Visual inspection of external condition
  - Differences from good samples
  - May require exemplars
- Detailed inspection: appearance, composition, damage, contamination, migration, abnormalities
  - Low power microscope
  - High power microscope
  - Scanning electron microscope (SEM)

Electrical Testing

- Electrical characteristics/performance
- DC test
- Parametrics (current-voltage characteristic)
- Simulated usage conditions
- Electrical probing

Deprocessing: Destructive Physical Analysis (DPA)

- Modification of specimen in order to reveal internal structures and analyze failure site. May involve:
  - Cross-sectioning and metallography
  - Decapsulation or delidding
  - Residual Gas Analysis for internal gases

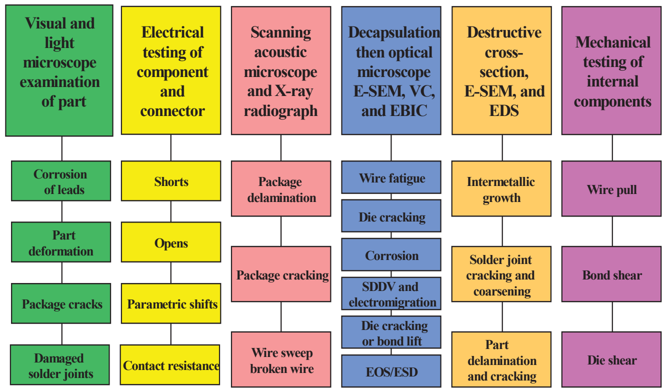
1x Magnification: Before Decapsulation

1x Magnification: After Decapsulation*

Fault Isolation

- Electrical Probing
- Time Domain Reflectometry (TDR)
- Electron Beam Testing
  - – electron beam induced current (EBIC),
  - – voltage contrast (VC),
  - – cathodoluminescence (CL)
- Emission Microscopy
- Scanning Probe Microscopy
- Thermal Analysis

Physical Analysis of Failure Site



Root Cause Identification

- Testing may be needed to determine the effect of hypothesized factors on the failure.
- A design of experiment (DoE) approach is recommended to incorporate critical parameters and to minimize the number of tests.
- This experimentation can validate a hypothesized root cause.

Failure Mechanisms

Review: Failure Definitions

Failure	A product no longer performs the function for which it was intended
Failure Mode	The effect by which a failure is observed.
Failure Site	The location of the failure.
Failure Mechanism	**The physical, chemical, thermodynamic or other process that results in failure.**

In principle, it should be possible to develop a **failure model** for a specific failure mechanism, expressing the likelihood of failure (time-to-failure, probability of failure, strength, etc.) as a function of the stresses and characteristics of the material.

Review: Classification of Failures

Key classes of failure:

– ***overstress*****:** use conditions exceed strength of materials; often sudden and catastrophic

– ***wearout*****:** accumulation of damage with extended usage or repeated stress

– *infant mortality*: failures early in expected life; typically related to quality issues.

Examples of Failure Models

Failure Mechanism	Failure Sites	Relevant Stresses	Sample Model
Fatigue	Die attach, Wirebond/TAB, Solder leads, Bond pads, Traces, Vias/PTHs, Interfaces	Cyclic Deformations (Δ T, Δ H, Δ V)	Nonlinear Power Law (Coffin-Manson)
Corrosion	Metallizations	M, ΛV, T, chemical	Eyring (Howard)
Electromigration	Metallizations	T, J	Eyring (Black)
Conductive Anodic Filament Formation	Between Metallizations	M, ΛV	Power Law (Rudra)
Stress Driven Diffusion Voiding	Metal Traces	σ, T	Eyring (Okabayashi)
Time Dependent Dielectric Breakdown	Dielectric layers	V, T	Arrhenius (Fowler-Nordheim)

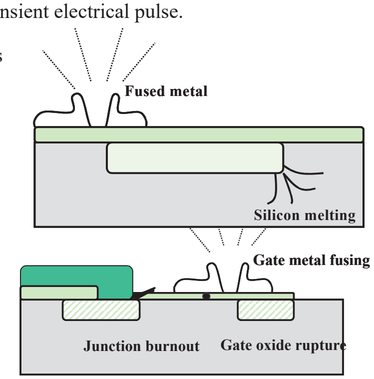
Δ:	Cyclic range	V:	Voltage
Λ:	gradient	M:	Moisture
T:	Temperature	J:	Current density
H:	Humidity	σ:	Stress

ESD/EOS Induced IC Failure Modes and Sites

Electrostatic discharge (ESD)/Electrical overstress (EOS) damage to an electrical circuit occurs due to electrical or thermal overstress during a transient electrical pulse.

Electrically, ESD and EOS can manifest as
- Opens
- Shorts
- Increased leakage
- Parametric shift

Physically, ESD and EOS can cause
- Melted bonding wires
- Molding compound burning
- Junction failure
- Gate oxide breakdown
- Discoloration
- Contact spike



Lee, T. W., 'ESD and EOS- There Is a Difference', *Commercialization of Military and Space Electronics Conference*, pp. 49-65, 2002.

Board Level Failures (examples)

Plated Through Hole (PTH)/Via
1. Fatigue cracks in PTH/Via wall
2. Overstress cracks in PTH/Via wall
3. Land corner cracks
4. Openings in PTH/Via wall
5. PTH/Via wall-pad separation

Electrical
6. Electrical overstress (EOS)
7. Signal interruption (EMI)

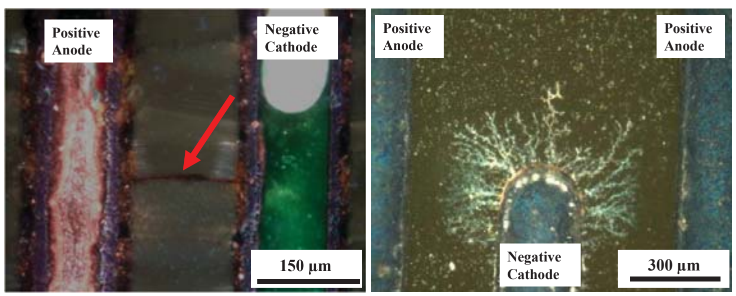
Board
8. CAF (hollow fiber)
9. CAF (fiber/resin interface)
10. Electrochemical migration
11. Buckling (warp and twist)

Copper Metallization
12. Cracks in internal trace
13. Cracks in surface trace
14. Corrosion of surface trace

Assembly Level Failures (examples)

Solder Interconnect
- Poor Solderability/Wettability
  - Tombstoning; Can accelerate other solder failure mechanisms
- Overstress Interconnect Failures
  - Solder Fracture (accelerated by intermetallic formation)
- Wearout Interconnect Failures
  - Solder Fatigue, Solder Creep
- Solder Bridging
- Component Failure due to Handling

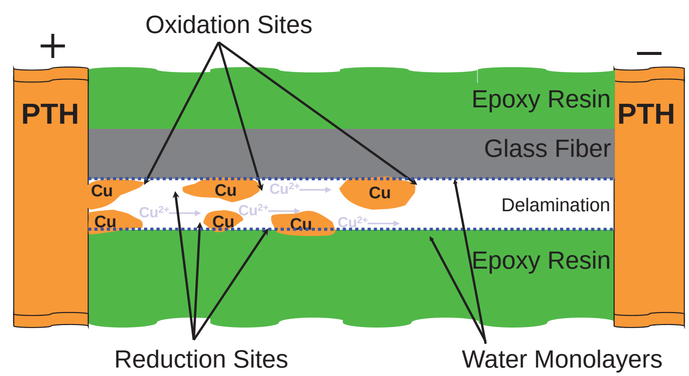
ECM: Surface and Sub-surface Mechanisms



ECM	Conductive Anodic Filament (CAF)	Dendritic Growth
Growth Direction	Anode to cathode	Cathode to anode
Filament Composition	Metallic salt	Pure metal
Growth Position	Internal	Surface

Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards." and Zhan, Sheng, Michael H. Azarian, and Michael Pecht. "Reliability of printed circuit boards processed using no-clean flux technology in temperature–humidity–bias conditions." Device and Materials Reliability, IEEE Transactions on 8.2 (2008): 426-434.

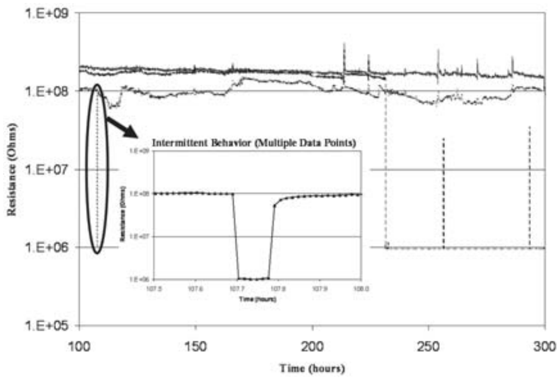
Formation of Conductive Filaments [1] [2]



A two step process: $t_{failure} = t_1 + t_2$ $t_1 >> t_2$

1. Rogers, K. L. (2005). An analytical and experimental investigation of filament formation in glass/epoxy composites (Doctoral dissertation).
2. Sood, B., & Pecht, M. (2011). Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants. Journal of Materials Science: Materials in Electronics, 22(10), 1602-1615.

PTH-PTH (6 mil) 10V, 85° C/85% RH [1]



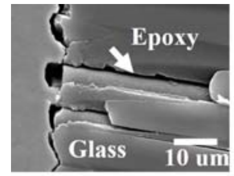
Factors
- Voltage gradient
- Humidity
- Conductor spacing
- Ion concentration in epoxy resin

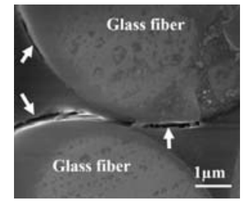
Contributors
- Fiber/resin separation
- Thermal excursions
- Hollow fibers
- Wicking
- Drilling damage

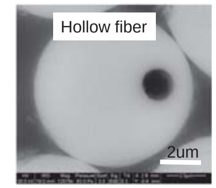
[1] Sood, B., & Pecht, M. (2011). Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants. Journal of Materials Science: Materials in Electronics, 22(10), 1602-1615.

Importance of the Epoxy/Glass Interface [1] [2]

Path formation for CAF is often along the glass fiber to epoxy matrix interphase.







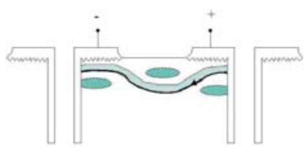
Path formation step (t_1) for CAF is eliminated when hollow glass fibers are present.

Fiber/resin interphase delamination occurs due to CTE mismatch (shear) induced weakening or bond degradation.

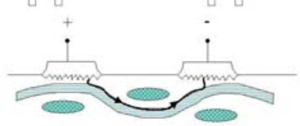
[1] IPC-9691, User guide for the IPC-TM-650, method 2.6.25, conductive anodic filament (CAF) resistance and other internal electrochemical migration testing.
[2] Shukla, A. (1997). Hollow fibers in woven laminates. Print Circ Fab, 20(1), 30-32.

CAF Paths

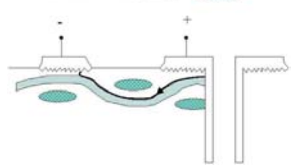
A. Between two plated-through holes (PTHs)



B. Between two traces

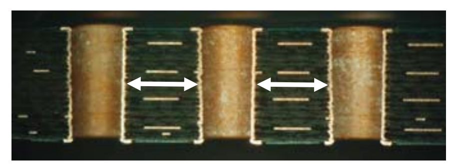


C. Between a trace and a plated-through hole (PTH)

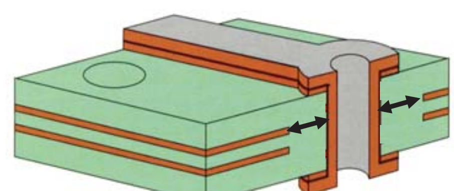


Ref: Rogers, Keith, et al. "Conductive filament formation failure in a printed circuit board." Circuit World 25.3 (1999): 6-8.

Factors Affecting CAF: PCB Internal Conductor Spacings



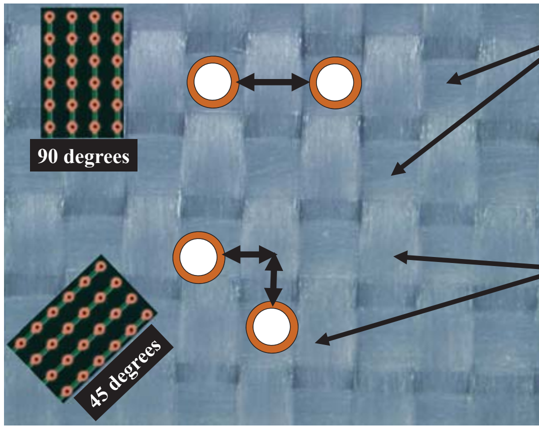
PTH-to-PTH spacings



PTH to plane spacings

Ref: Rogers, Keith, et al. "Conductive filament formation failure in a printed circuit board." Circuit World 25.3 (1999): 6-8.

Factors Affecting CAF: Board Orientation Respective to Fabric Weave

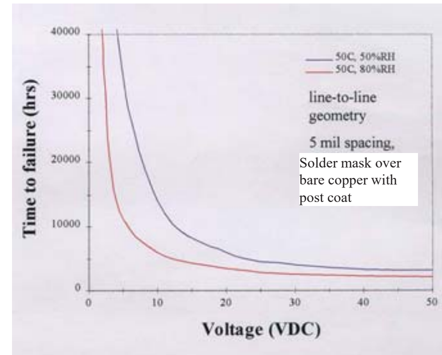


The initial set of parallel fiber bundles, known as the warp, lie in the machine direction

A second set of parallel fiber bundles, known as the fill or weft, is woven through the first set

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

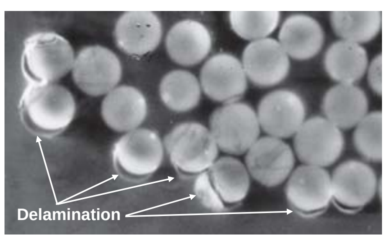
Effect of Voltage and Humidity on Time to Failure



Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Fiber/Resin Interface Delamination

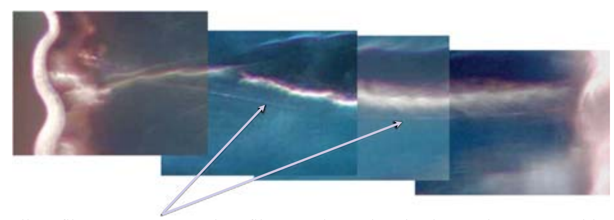
Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (ratio of 1 to 12).



Delamination can be prevented/resisted by selecting resin with lower CTE's and optimizing the glass surface finish. Studies have shown that the bond between fiber and resin is strongly dependent upon the fiber finish.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Hollow Fibers

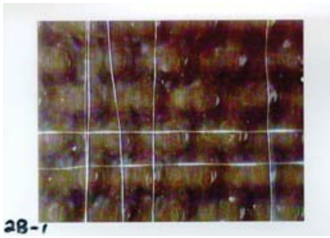


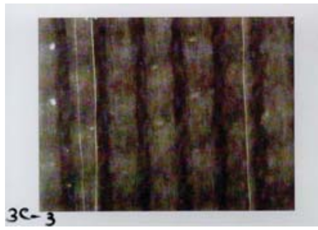
Hollow fibers are vacuous glass filaments in E-glass laminates that can provide paths for CAF.

With the appearance of hollow fibers inside the laminates, CAF can happen as a one step process. In this case, the number of hollow fibers inside the laminates is most critical to reliability.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Images of Hollow Fibers



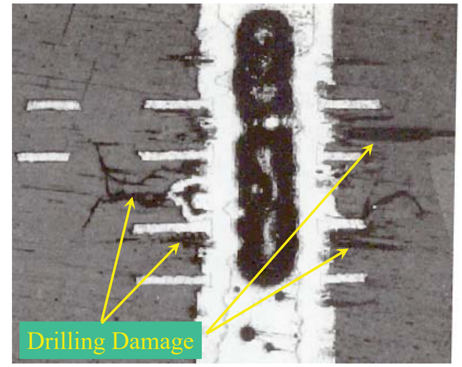


Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Drilling

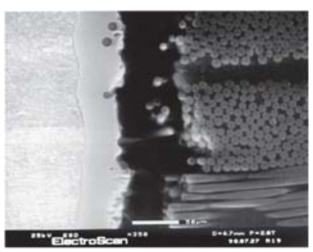
Drilling damage can accelerate CAF through

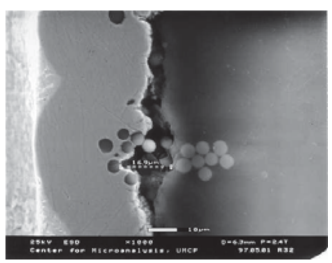
- Fiber/resin delamination,
- Creation of paths for moisture to accumulate
- Wicking due to cracking of the board material



Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

PTH-Resin Separation



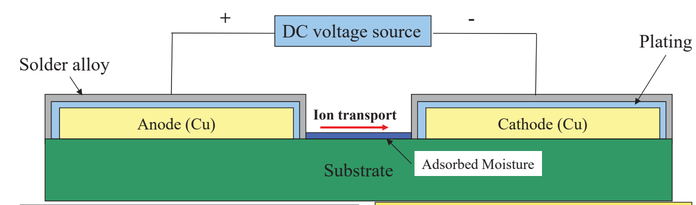


In both of these SEM pictures, a separation can be seen at the copper plating to fiber epoxy resin board interface. These gaps provide an accessible path for moisture to accumulate and CAF to initiate. These voids can be adjacent to inner-layer copper foil or to the PTH barrel and normally result from contraction of the epoxy (resin recession) due to the heat of thermal stress.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Background on Dendritic Growth

Dendritic Growth is a form of electrochemical migration (ECM) involving the growth of conductive filaments on or in a printed circuit board (PCB) under the influence of a DC voltage bias. [IPC-TR-476A]



Necessary Conditions for ECM

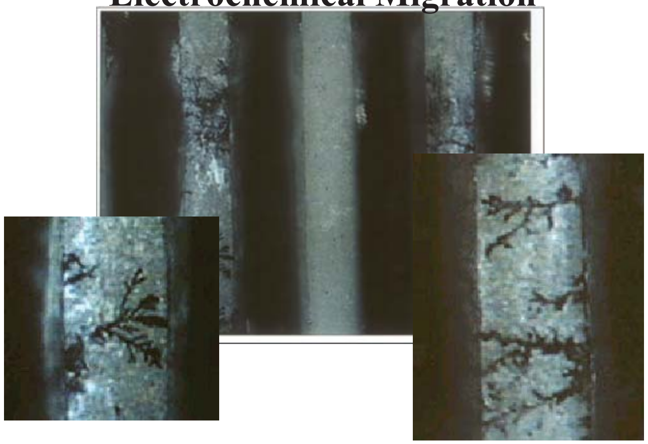
- Electrical carriers (ions).
- A medium, usually water, to dissolve the ionic materials and sustain them in their mobile ionic state.
- Electrical potential between the electrodes to establish an ionic current in the liquid medium.

Stages of ECM

- Path formation
- Electrodissolution
- Ion transport
- Electrodeposition
- Filament growth

He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." *IPC printed circuit Expo, APEX & Designer summit proceedings.*

Electrochemical Migration



Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

Contaminants

- Halide residues, such as chlorides and bromides, are the most common accelerators of dendritic growth.
- Chlorides are more detrimental, but easier to clean
- Bromides can resist cleaning; often require DI water with saponifier
- In general, an increased risk of ECM will tend to occur once the levels of chloride exceed 10μg/in^2 or bromide exceeds 15μg/in^2
- Rapid failure can occur when contaminant levels exceed 50μg/in^2

Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

What Are the Sources of Contaminants?

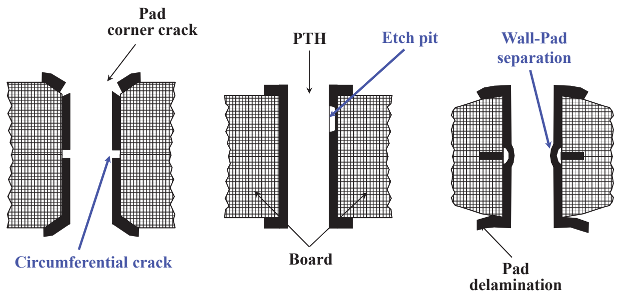
- Board Manufacturing
  - Flame-proofing agents
  - Copper plating deposits
  - Etchants
  - Cleaners
  - Fluxes (for HASL coatings)
  - Poorly polymerized solder masks
  - "Fingerprints"
- Assembly
  - Fluxes
  - Solder paste residues
  - "Fingerprints"
- Environmental
  - Liquid (i.e., salt spray)
  - Gaseous (i.e., Cl_2)

Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

Plated Through Hole (PTH) Failures

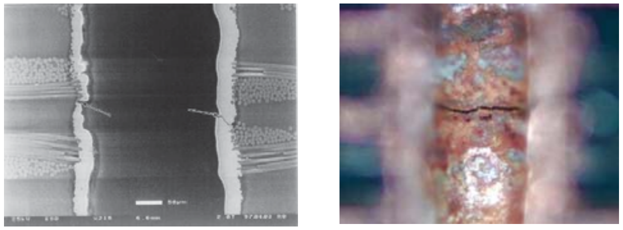
1. Circumferential cracking
   - Single event overstress
   - Cyclic fatigue
2. Openings (voids, etch pits)
   - Accelerate circumferential cracking
3. Wall-Pad Separation
   - Also known as "breakout of internal lands" or "plated-barrel separation"

PTH Failures (cont.)



Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

1. Circumferential Cracking – Single Event Overstress



Since the difference in the coefficient of thermal expansion (CTE) of the copper plating and the resin system in the PWBs is at least a factor of 13, stress exerted on the plated copper in the plated-through holes in the z-axis can cause cracking.

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Single Event Overstress (cont.)

- Failure Mode
  - Complete electrical open
- Failure History
  - Primarily occurs during assembly; may not be detected until after operation
- Root-Causes
  - Excessive temperatures during assembly
  - Resin Tg below specification
  - Insufficient curing of resin
  - Outgassing of absorbed moisture
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Insufficient mechanical properties of deposited copper
  - Plating voids
  - Etch pits
  - Insufficient PTH wall thickness

Design Considerations to Avoid Fatigue Damage in PTHs

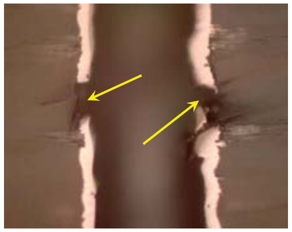
- PTH Spacing
  - Decreasing spacing improves mechanical reliability
- Aspect Ratio
  - Decreasing board thickness more effective than increasing hole diameter
- Plating Thickness
  - Increasing leads to increasing in fatigue strength
- Nonfunctional Internal Pads
  - Minimal effect. Results in localized stress relief; most effective when results in elimination of resin-rich areas

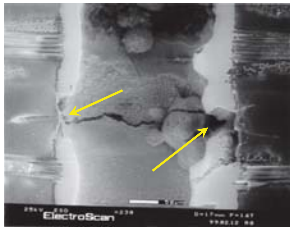
Ref: Kapur, Kailash C., and Michael Pecht. Reliability engineering. John Wiley & Sons, 2014.

Root-Cause Analysis of Circumferential Fatigue Cracking

- Failure Mode
  - Intermittent to complete electrical open
- Failure History
  - Requires an environment with temperature cycling; often occurs after extended use in the field (“child” or “teenage” mortality)
- Root-Causes
  - Resin CTE below specification
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Customer use exceeds expected environment
  - Insufficient mechanical properties of deposited copper
  - Presence of overstress crack
  - Plating voids
  - Etch pits (“mouse bites”)
  - Insufficient PTH wall thickness

2. Openings in PTH Walls


Optical micrograph of cross section of PTH with etch damage

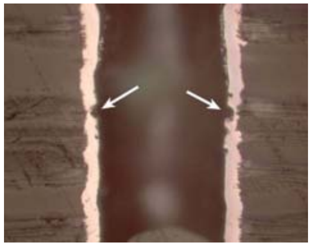


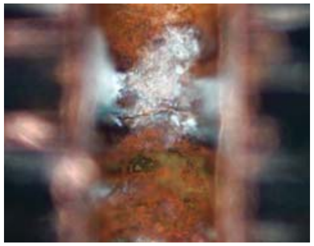
Electron micrograph of same PTH shown on left

Overetching can cause electrical opens or induce overstress circumferential cracking

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Evidence of Overetching


Optical micrograph of cross section of PTH with etch damage (bright field)


Optical micrograph of cross section of PTH with etch damage (dark field)

Evidence of overetching can include reduced plating thickness and discoloration of PTH barrel walls

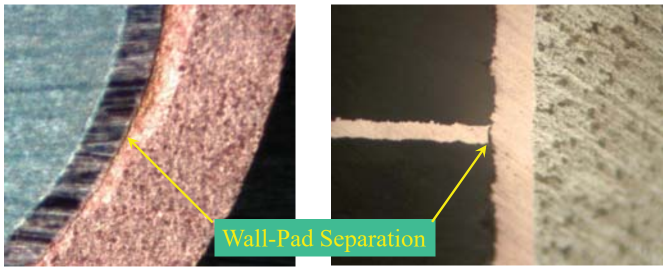
Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Opening in PTH/Via

- Failure Mode
  - Complete electrical open
- Failure History
  - Often occurs during assembly; may not be detected until after operation
- Root-Causes
  - Openings in PTH’s/Vias are etch pits or plating voids and often occur because the following manufacturing processes are not optimized:
    - Drilling
    - Desmear/Etchback
    - Electroless copper plating or direct metallization
    - Electrolytic copper plating
    - Tin resist deposition
    - Etching
  - Openings can also occur due to poor design (i.e., single-sided tenting of vias, resulting in entrapment of etchant chemicals)

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

3. PTH/Via Wall-Pad Separation



Optical micrograph of cross section perpendicular to the PTH axis

Optical micrograph of cross section parallel to the PTH axis

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

PTH/Via Wall-Pad Separation

- Failure Mode
  - Intermittent or complete electrical open
- Failure History
  - Will primarily only occur during assembly
- Root-Causes
  - Insufficient Curing of Resin.
  - Outgassing of absorbed moisture
  - Excessive temperatures during assembly
  - Resin CTE or Resin Tg below specification
  - Number of nonfunctional lands (only useful for failures during assembly)
  - Drilling process resulting in poor hole quality
  - Insufficient desmearing process.
  - Substandard processes or materials in electroless copper plating

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

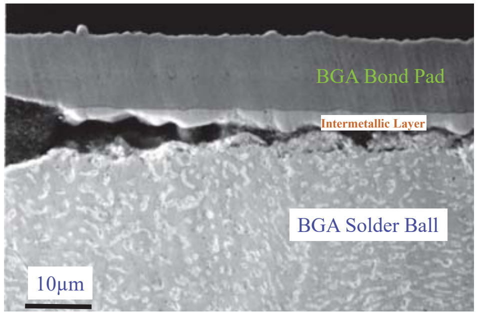
Failure Mechanisms due to Handling

- Affects leadless components
  - Ball grid arrays (BGAs), Flip Chip on Board
- Affects brittle components
- Insidious
  - Failures due to handling tend to difficult to screen and intermittent in nature
  - Often occur after testing

When Do Handling Failures Occur?

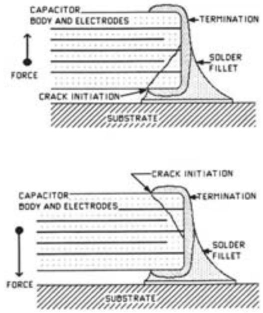
- Assembly
  - Transfer of product between lines; during rework
- Heatsink Attachment
  - Use of screws
- Connector Insertion
  - Large press-fit connectors; daughter boards into mother boards
- Electrical Testing
  - Bed-of-Nails testing can bend local areas
- Packaging
- Transportation
- Customer Site
  - Slot insertion

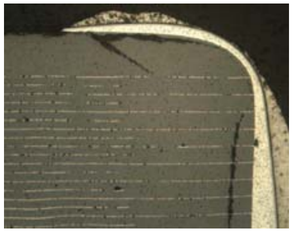
Evidence of Damage Due to Handling -- BGAs



Ref: SEM Lab.

Evidence of Damage – Ceramic Capacitors





Keimasi, Mohammadreza, Michael H. Azarian, and Michael G. Pecht. "Flex Cracking of Multilayer Ceramic Capacitors Assembled With Pb-Free and Tin–Lead Solders." Device and Materials Reliability, IEEE Transactions on 8.1 (2008): 182-192.

Intermittent Failures

- An intermittent failure is the loss of some function in a product for a limited period of time and subsequent recovery of the function.
- If the failure is intermittent, the product's performance before, during, or after an intermittent failure event may not be easily predicted, nor is it necessarily repeatable.
- However, an intermittent failure is often recurrent.

Ref: Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674.

No Fault Found

- No-Fault-Found (NFF): Failure (fault) occurred or was reported to have occurred during product's use. The product was tested to confirm the failure, but the testing showed "no faults" in the product.
- Trouble-Not-Identified (TNI): A failure occurred or was reported to have occurred in service or in manufacturing of a product. But testing could not identify the failure mode.
- Can-Not-Duplicate (CND): Failures that occurred during manufacture or field operation of a product cut could not be verified or assigned.
- No-Problem-Found (NPF): A problem occurred or was reported to have occurred in the field or during manufacture, but the problem was not found during testing.
- Retest-OK: A failure occurred or was reported to have occurred in a product. On retesting the product at the factory, test results indicated that there was no problem.

Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674.

The Impact of Intermittents

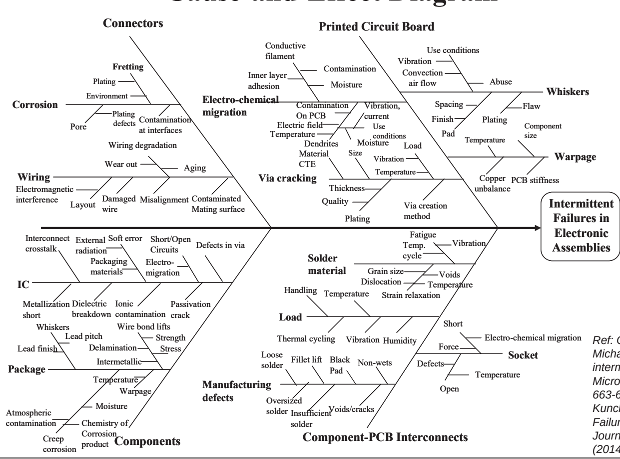
- Can not determine root cause and thus the reason for the failure (NFF)
- Reliability modeling analysis can be faulty
- Potential safety hazards
- Decreased equipment availability
- Long diagnostic time and lost labor time
- Complicated maintenance decisions
- Customer apprehension, inconvenience and loss of customer confidence
- Loss of company reputation
- Increased warranty costs
- Extra shipping costs

NFF Test Sensitivities

Testing has five possible outcomes:

- Test can say it is good when it is good.
- Test can say it is bad when it is bad.
- Test can say it is good when it is bad.
- Test can say it is bad when it is good.
- Test can be inconsistent.

Intermittent Failures in Electronic Assemblies
Cause-and-Effect Diagram



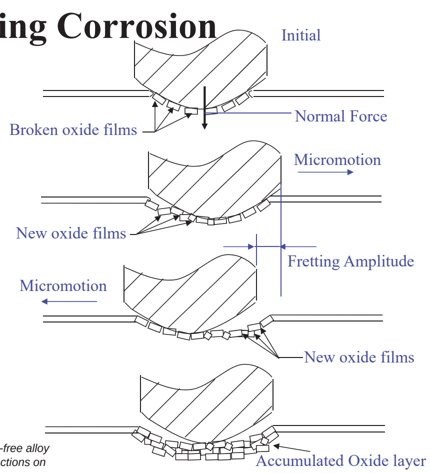
Ref: Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674 and Bakhshi, Roozbeh, Surya Kunche, and Michael Pecht. "Intermittent Failures in Hardware and Software." Journal of Electronic Packaging 136.1 (2014): 011014.

Characteristics of Intermittent Failures

- May indicate that a failure has occurred. Intermittent failure may be due to some extreme variation in field or use conditions.
- May indicate the imminent occurrence of failure.
- May not leave a failure signature making it difficult to isolate the site.

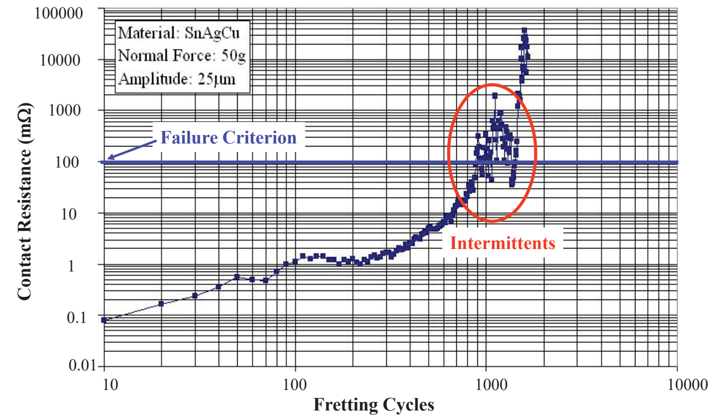
Example: Intermittent Failures Due to Fretting Corrosion

- Tin alloys are soft metals on which a thin but hard oxide layer is rapidly formed.
- Being supported by a soft substrate, this layer is easily broken and its fragments can be pressed into the underlying matrix of soft, ductile tin-lead alloy.
- The sliding movements between contact surfaces break the oxide film on the surface and expose the fresh metal to oxidation and corrosion.
- The accumulation of oxides at the contacting interface due to repetitive sliding movements causes contact resistance to increase, leading to contact open.
- Tin based lead-free solders are expected to show similar fretting corrosion susceptibility as tin-lead solder coatings.



Ref: Wu, Ji, and Michael G. Pecht. "Contact resistance and fretting corrosion of lead-free alloy coated electrical contacts." Components and Packaging Technologies, IEEE Transactions on 29.2 (2006): 402-410.

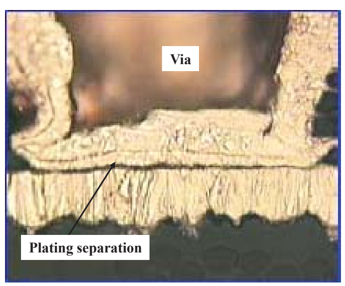
Electrical Contact Resistance vs. Fretting Cycles



Ref: Wu, Ji, and Michael G. Pecht. "Contact resistance and fretting corrosion of lead-free alloy coated electrical contacts." Components and Packaging Technologies, IEEE Transactions on 29.2 (2006): 402-410 and Antler, Morton, and M. H. Drozdowicz. "Fretting corrosion of gold-plated connector contacts." Wear 74.1 (1981): 27-50.

Intermittent Failure Due to Improper Micro-via Plating in PCB

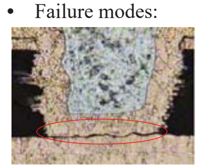
- A computer graphics OEM was experiencing intermittent failures on printed circuit boards with chip scale packages (CSPs) and ceramic ball grid array packages (CBGAs).
- High magnification metallurgical microscope imaging of micro-etched cross sections of micro-vias in the printed circuit board showed a separation of the via plating from the target pad [Nektek Inc. Service Report, 2004].
- The plating separation was found to be the cause of intermittent failure.



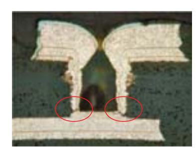
Plating separation at base of micro via [Nektek Inc. Service Report]

Known µvia Failures in the Literature

- Failure modes:

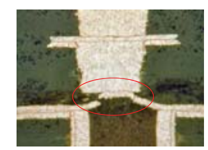


Interfacial separations [1]



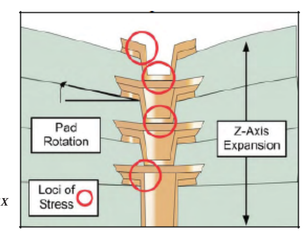
Barrel cracks [3]

Corner/knee cracks [1]



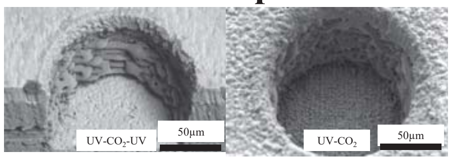
Target pad cracks [2]

- Failures can be caused by
  - CTE mismatch driven thermomechanical stresses
  - Design – stacked/staggered
  - Laser parameters
  - Processes and chemistries



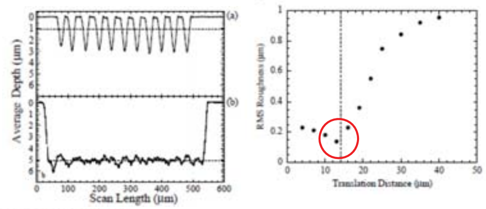
[1] B. Birch, "Reliability Testing for Microvias in Printed Wire Boards", Circuit World, Vol 35, No. 4, pp.3 – 17, 2009
[2] Heer, Hardeep, and Ryan Wong. "Reliability of stacked microvia." Proc. IPC APEX Technical Conference. 2014.
[3] Lesniewski, Thomas. "Effects of dielectric material, aspect ratio and copper plating on microvia reliability." Proc. IPC APEX Technical Conference. 2014.
[4] Magera, J, "Copper Filled Microvias The New Hidden Threat Links of Faith Are Not Created Equally", IPC APEX 2019.
[5] Baccam J, "Microvia Reliability", IPC High Reliability Forum 2018.

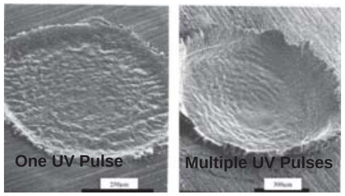
Impact of Laser Scan Parameters

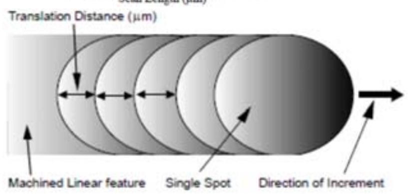


Pattern Plated Cu + Alternative Oxide

Core Construction



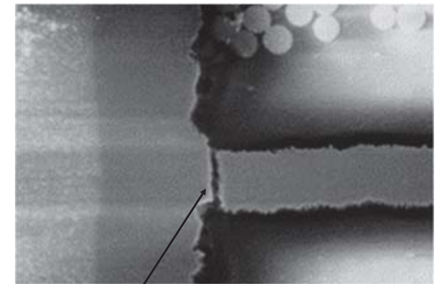




1. Sood, Bhanu, Craig B. Arnold, and Alberto Pique. "Depth and surface roughness control on laser micromachined polyimide for direct-write deposition." Micromachining and Microfabrication Process Technology VIII. Vol. 4979. International Society for Optics and Photonics, 2003.
2. Duley, W. W., UV Lasers: effects and applications in materials science, Cambridge University Press, 1996.
3. Magera, J, "Copper Filled Microvias The New Hidden Threat Links of Faith Are Not Created Equally", IPC APEX 2019.

Example: Intermittent Failure Due to Open Trace in PCB

- Open trace can also cause intermittent failures in PCB under environmental loading conditions.
- Under thermal cycling or vibration loading, the open trace may reconnect with intermittent electrical continuity observations.

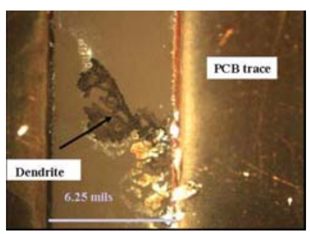


Open Trace

Ref: A Study in Printed Circuit Board (PCB) Failure Analysis, Part 2, Insight Analytical Labs, Inc

Example: Intermittent Failures Due to Electro-chemical Migration (Surface Dendrites)

- Electrochemical migration (ECM) can cause shorts due to the growth of conductive metal filaments in a printed wiring board (PWB).
- Surface dendrites can form between the adjacent traces in the PWB under an applied voltage when surface contaminants and moisture are present.
- It is often difficult to identify the failure site because the fragile dendrite structure will burn upon shorting, often leaving no trace of its presence.

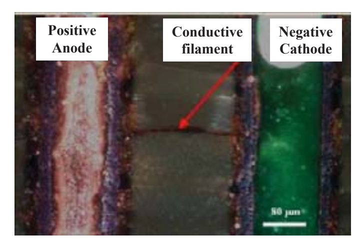


Dendritic growth during an ECM test

Ref: Zhan, Sheng, Michael H. Azarian, and Michael Pecht. "Reliability of printed circuit boards processed using no-clean flux technology in temperature–humidity–bias conditions." Device and Materials Reliability, IEEE Transactions on 8.2 (2008): 426-434.

Example: Intermittent Failures Due to Electro-chemical Migration (Conductive Anodic Filament Formation)

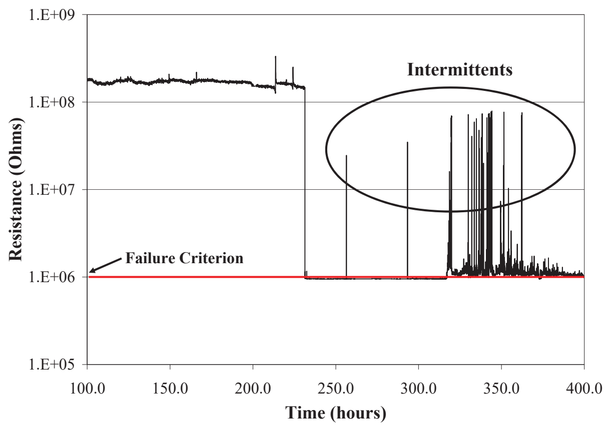
- Conductive filament is formed internal to the board structure.
- In CAF, the filament is composed of a metallic salt, not neutral metal atoms as in dendritic growth.
- One of distinct signatures of CAF failures is intermittent short circuiting. The conductive filament bridging the two shorted conductors can blow out due to the high current in the filament, but can form again if the underlying causes remain in place.



A conductive filament bridging two plated through holes in a PWB

Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards."

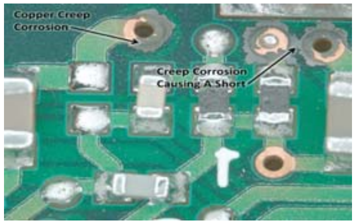
Electrical Resistance vs. Time Due to CAF



Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards."

Example: Intermittent Failures Due to Creep Corrosion

- Definition
  - Creep corrosion is a mass transport process in which solid corrosion products migrate over a surface.
- Failure mode
  - On IC packages, creep corrosion can eventually result in electrical short or signal deterioration due to the bridging of corrosion products between isolated leads.
  - Depending on the nature of the environment, the insulation resistance can vary and cause intermittents.

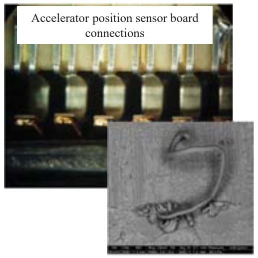


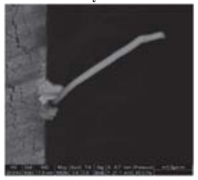
Ref: Thesis "Reliability challenges in airside economization and oil immersion cooling", Jimil Shah, 2016.

Intermittent Failures Due to Tin Whiskers

Failed relay due to tin vapor arcing

Whiskers on the armature of a relay



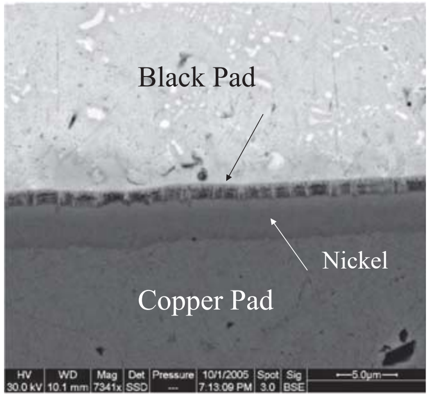


Tin whisker on the edge of an acceleration position sensor board connection terminal of a 2002 Toyota Camry

- Whiskers are elongated single crystals of Sn which grow spontaneously out of the surface. Internal stresses within the plated deposit drives growth.
- Tin (and other conductive) whiskers or parts of whiskers may break loose and bridge isolated conductors, resulting in an intermittent short circuit. These field failures are difficult to duplicate or are intermittent because at high enough current the conductive whisker can melt, thus removing the failure condition. Alternatively, disassembly or handling may dislodge a failure-producing whisker.
- Failure analysis concluded that tin whiskers initiated the current surge to the ground. Once a whisker bridged a terminal stud to the armature, plasma arcing could occur with enough voltage and current to damage the relay.

1. Davy, Gordon. "Relay Failure Caused by Tin Whiskers." (2002).
2. Sood, Bhanu, Michael Osterman, and Michael Pecht. "Tin whisker analysis of Toyota's electronic throttle controls." Circuit World 37.3 (2011): 4-9.
3. Leidecker, H., L. Panashchenko, and J. Brusse. "Electrical failure of an accelerator pedal position sensor caused by a tin whisker and investigative techniques used for whisker detection." 5th International tin whisker symposium. 2011.

Intermittent Failures Due to Black Pad



- The 'Black Pad' phenomenon in Electroless Nickel over Immersion Gold (ENIG) board finish manifests itself as gray to black appearance of the solder pad coupled with either poor solderability or solder connection, which may cause intermittent electrical 'opens.'
- Bulwith et al. [2002] identified numerous Ball Grid Array (BGA) package intermittent electrical open failures to be black pad related.

Zeng, Kejun, et al. "Root cause of black pad failure of solder joints with electroless nickel/immersion gold plating." Thermal and Thermomechanical Phenomena in Electronics Systems, 2006. ITHERM'06. The Tenth Intersociety Conference on. IEEE, 2006.

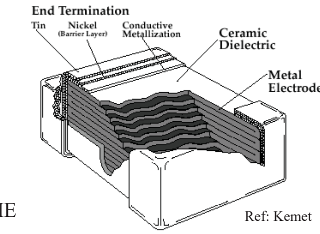
CASE STUDY*

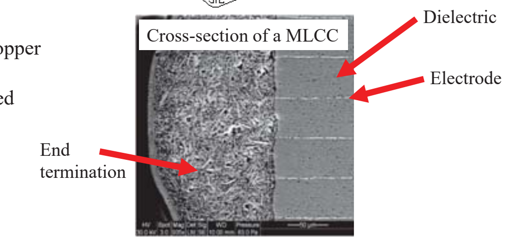
Failure Analysis of Multilayer Ceramic Capacitor (MLCC) with Low Insulation Resistance

*Adapted from:
1. Shrivastava, A., Sood, B., Azarian, M., Osterman, M., & Pecht, M. (2010, June). An investigation into a low insulation resistance failure of multilayer ceramic capacitors. In Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th (pp. 1811-1815). IEEE.
2. Brock, Garry Robert. "The Effects of Environmental Stresses on the Reliability of Flexible and Standard Termination Multilayer Ceramic Capacitors." PhD diss., 2009.

MLCC Construction

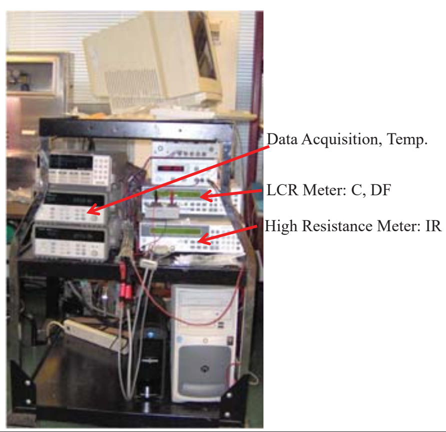
- Ceramic Dielectric
  - Typically comprised of compounds made with titanium oxides
  - ➢ $BaTiO_3$ ("X7R") for this study
- Electrodes
  - Base metal consisting of nickel (BME)
  - ➢ Precious metal consisting of silver/ palladium (PME
- End Termination
  - Standard termination consists of silver or copper coated with nickel and tin
  - ➢ Flexible termination consists of a silver filled polymer coated with nickel and tin



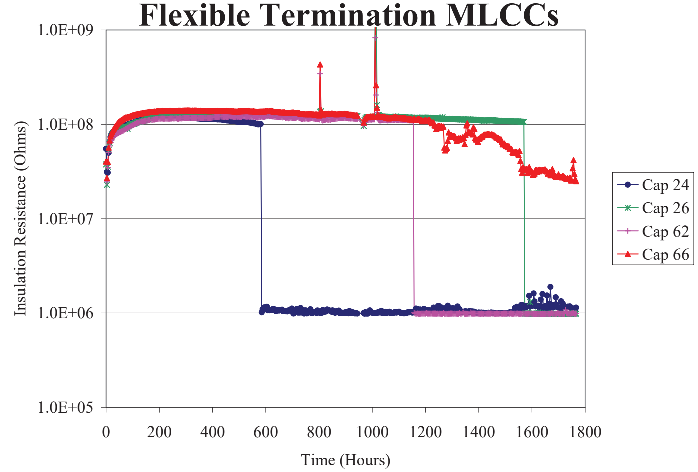


Loading Conditions: Temperature-Humidity-Bias

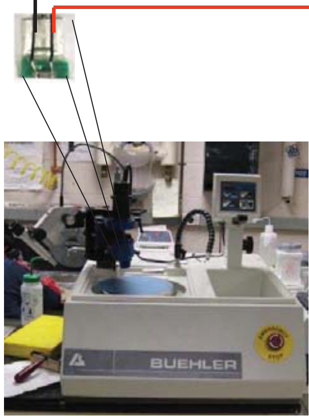
- A Temperature-Humidity-Bias (THB) test was performed for 1766 hours at 85° C and 85% RH, at the rated voltage of 50V.
- Capacitance, Dissipation Factor (DF) and Insulation Resistance (IR) were monitored during the test.
- A 1 MΩ resistor was placed in series with each of the MLCCs.
- The MLCCs were size 1812 and soldered to an FR-4 printed circuit board using eutectic tin-lead solder.



IR Test Data for Failed Flexible Termination MLCCs

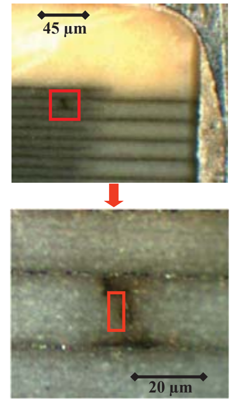


THB Failure Analysis Methodology for Biased MLCCs

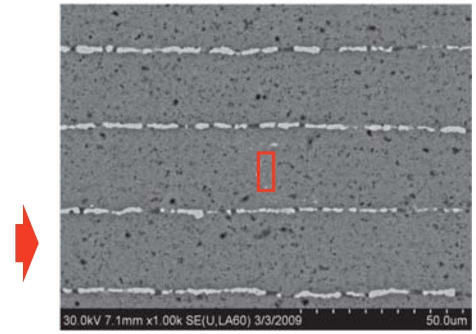


- A Buehler MPC 2000 (with 9 micron lapping film) was used to cross-section the MLCC.
- The MLCC (on a PCB) was mounted to a fixture using wax.
- Wires were soldered to the board, along with a 1 kΩ series resistor.
- Resistance was monitored with a multimeter as the sample was moved ~5 microns at a time while checking for a resistance change.
- Epoxy was added under the part to prevent buildup of metal debris, which could cause an inaccurate resistance value.

Metal Migration Between Electrodes

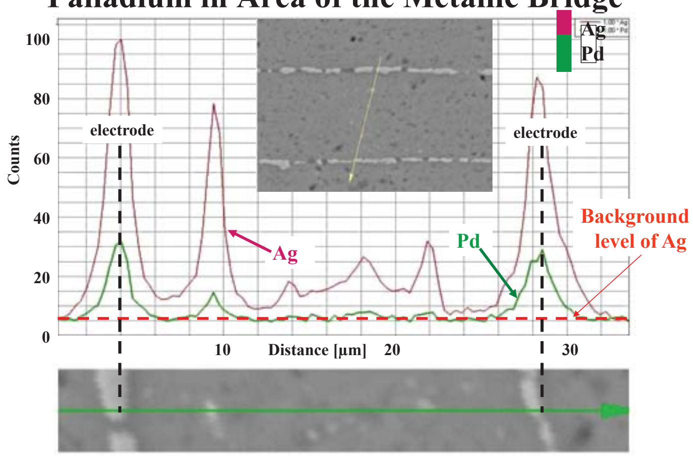


Optical Micrographs of Cross-section

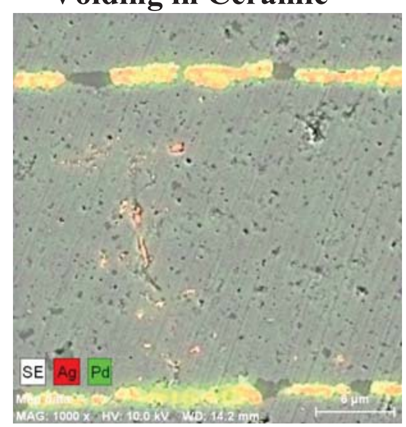


SEM Image of Cross-section

EDS Line Scan Showing Silver and Palladium in Area of the Metallic Bridge



EDS Map Showing Silver Migration and Voiding in Ceramic



Failure Mechanism

- Metal migration was found in several of the failed MLCCs.
- Voids in the ceramic, without silver or palladium, were also found close to the conduction path.
- The failure mechanism was electrochemical co-migration of silver and palladium, aided by porosity in the dielectric.

Non-Destructive Techniques

- Electrical Testing
- Scanning Acoustic Microscopy (SAM)
- X-ray Inspection
- X-ray Fluorescence (XRF)
- Optical Inspection

Electrical Testing of Components and Printed Circuit Boards

Electronic Testing Equipment

- Digital meters
  - Multimeters
  - Specialized parametric meters, such as LCRs, high resistance meters, etc.
- Oscilloscopes, Spectrum Analyzers
- Curve tracer/Parameter Analyzers
- Time Domain Reflectometers
- Automated Test Equipment (ATE)

Digital Multimeters

- Typically provide:
  - Voltage (DC, AC rms)
  - Resistance (2 wire)
  - Current
- Other common options:
  - Resistance (4 wire)
  - Frequency or count
  - Diode voltage
  - Capacitance
  - Temperature
  - Datalogging

Agilent 34401A

LCR Meters and Impedance Analyzers

- Variable AC voltage and frequency.
- Used to characterize
  - Capacitors
  - Inductors
  - Transformers
  - Filters
  - Dielectric materials (e.g., PCB substrates)

Agilent 4263B

High Resistance Meters

- Typically measure:
  - Leakage current
  - Insulation resistance
- Common applications:
  - Insulation resistance of dielectrics (capacitors, substrates)
  - Surface insulation resistance of PCBs

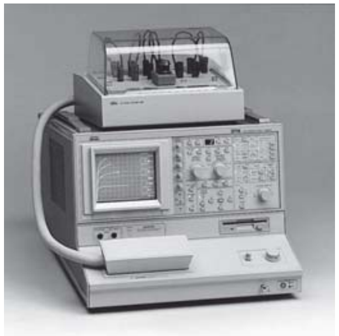
Agilent 4339B

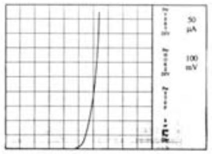
Oscilloscopes and Spectrum Analyzers

- Digital scopes allow:
  - Waveform storage
  - Capture of transients
  - Waveform measurements
  - Math (e.g., FFT)
  - Complex triggering
- Spectrum analyzers are used for frequency domain measurements.

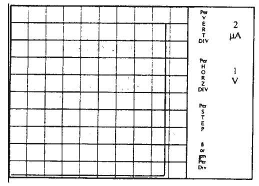
Agilent 54601

Curve Tracer or Parameter Analyzer

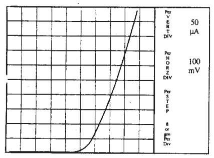




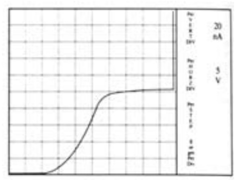
Normal I-V curve



Normal I-V curve



Abnormal I-V curve (due to the presence of a series resistance)



Abnormal I-V curve – Ionic Contamination (Reverse Bias)

- Low frequency display of voltage versus current

Automated PCB Test Equipment

- Dedicated Wired Grid – test probes wired to the grid. High cost.
- Universal Grid (“Bed of Nails”) –Low cost, reusable. Spring loaded or rigid test probes in mechanical contact to the grid.
- Flying Probe or Fixtureless System with moveable single or double probes. Expensive. Empirical techniques applied on capacitance /impedance data to determine a good board. Good for micro products. Issues with pad damage.

Scanning Acoustic Microscopy

Common Applications

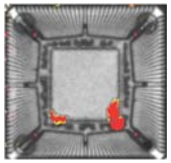
Defects specific to IC packages include:

- Delamination at wirebonds, substrate metallization, dielectric layers, element attaches, and lid seals.
- Die-attach field-failure mechanisms induced by improper die mounting and de-adhesion.
- Delamination of the molding compound from the leadframe, die, or paddle
- Molding compound cracks
- Die tilt
- Voids and pinholes in the molding compound and die attach

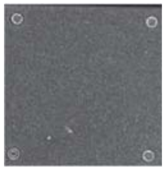
Other applications:

- Flip Chips
- Bonded Wafers
- Printed Circuit Boards
- Capacitors
- Ceramics
- Metallic
- Power Devices/Hybrids
- Medical Devices
- Material Characterization

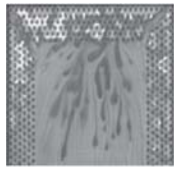
Common Applications



Die Top Delamination

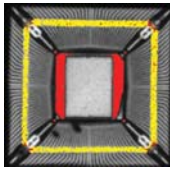


Mold compound voids

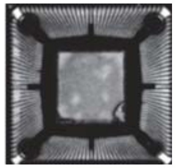


Flip Chip Underfill Voids

Die Tilt, B-Scan



Die Pad delamination

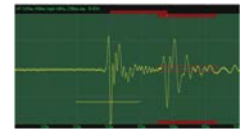


Die Attach Voids

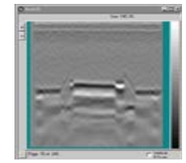
Ref: Moore, T. M. "Identification of package defects in plastic-packaged surface-mount ICs by scanning acoustic microscopy." ISTFA 89 (1989): 61-67 and Briggs, Andrew, ed. Advances in acoustic microscopy. Vol. 1. Springer Science & Business Media, 2013.

Scanning Acoustic Modes

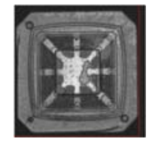
A-Scan: Raw ultrasonic data. It is the received RF signal from a single point (in x,y).



B-Scan: Line of A-scans. (Vertical cross-section)



C-Scan: Data from a specified depth over the entire scan area. (Horizontal cross-section).



Limitations of the Techniques

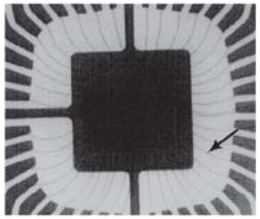
- Materials and interfaces of interest have to be flat (i.e., not useful on solder balls or joints unless at a flat interconnection sites.
- Materials have to be relatively homogeneous (not practical for PWB internal examination, hence not applicable for BGAs on PWB substrates, but allowable for BGAs on ceramic).
- Metals tend to interfere with the acoustic signal (i.e., unable to examine underneath of metal layers such as a copper die paddle or an aluminum heat sink. The copper metallization on PWBs is another hindrance for their internal examination).
- Operator needs to be highly skilled to correctly acquire and interpret data.
- Since resolution and penetration depth are inversely related, a trade off must be made.

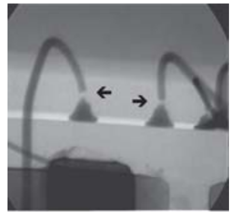
X-ray Radiography

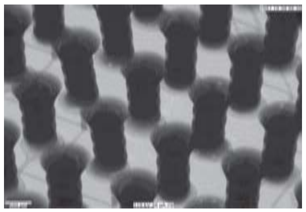
Applications and Examples

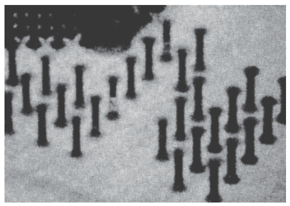
Typical applications include:

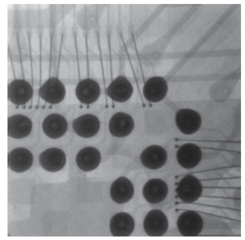
- Internal structures of electronic devices
- Connection techniques (Flip Chip, µBGA, BGA, MCM, COB)
- Inner layers of PCBs



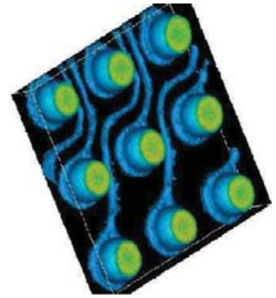




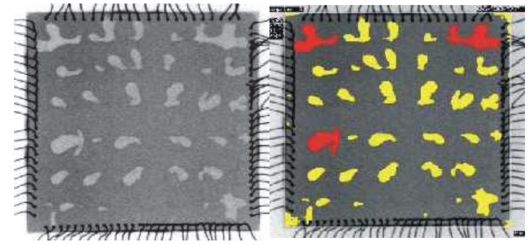




Applications: CT Visualization and Software



The computed tomography (CT) technique enables 3-dimensional inspection of planar components as seen in this BGA assembly.



Use of voiding calculation software enables the estimation of voided area observed in die attach. Given a nominal size area, voids can be color coded for easier visualization of areas larger than or smaller than these dimensions. The yellow represent normally sized voids, whereas, the red ones are larger.

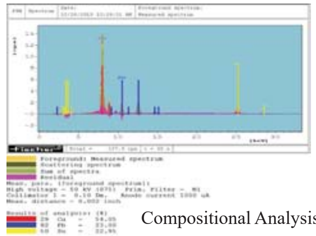
Limitations of X-ray Techniques

- Although considered a non-destructive test, X-ray radiation may change the electrical properties of sensitive microelectronic packages such as EPROMS, and hence should not be used until after electrical characterization has been performed on these devices.
- For samples on or below thick metal layers such as large heat sinks as seen in power devices, X-ray imaging is more difficult and requires high voltages and currents.
- Magnification using contact X-ray equipment can only be done externally by a magnified view of the 1:1 photo, or from an enlarged image of the negative. Hence, resolution will decrease as the image is enlarged.
- The operator may have to experiment with voltage settings and exposure times, depending on the type of sample and film used, to obtain proper contrast and brightness in the photos.

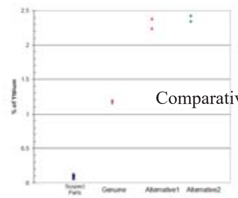
X-Ray Fluorescence (XRF)

Types of Analysis

- Spectrum analysis to determine the elements and the composition of an unknown sample.
- Material analysis for bulk samples (one layer sample)
- Thickness analysis to determine the thickness and the composition of different layers.
- Pure element and alloy standards (such as Ni, Cu, Ag, Sn, Au, Pb and SnAgCu or SnPb alloys) can be used to calibrate the spectrometer.

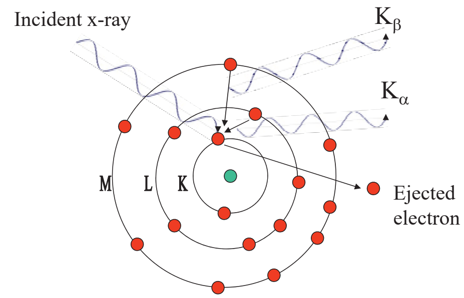


Compositional Analysis



Comparative Analysis

Background on X-Ray Fluorescence



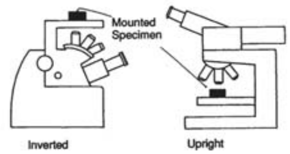
- Incident x-ray is incident on sample
- Core electron is ejected
- Electron from outer shell falls down to fill up the vacancy
- X-ray photon is emitted (energy equal to the difference between the two levels involved in the transition), which is characteristic of the element and the electronic transition

Conclusion

- XRF is a powerful tool to analyze composition and coating thickness on a variety of electronic products
- A non-destructive tool, does not require sample preparation, provides quick analysis results
- Users should be aware of the issues related to the automated analysis software

Visual Inspection

External Visual Inspection



Higher power light optical microscopes

- Inverted
- Upright

Low power stereo macroscope (up to 65x)
- Overview
- Package level
- PCB level

Typical stereo macroscope

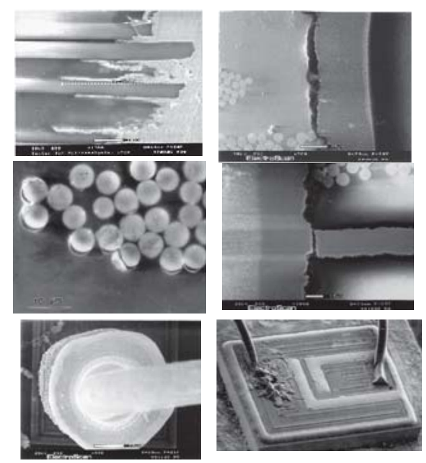
Analytical Techniques

- Environmental Scanning Electron Microscopy (ESEM)
- Energy Dispersive Spectroscopy (EDS)
- Thermo-mechanical Analysis
- Microtesting (Wire Pull, Ball Bond and Solder Ball Shear, Cold Bump Pull)
- Decapsulation / Delidding
- Dye Penetrant Inspection (Dye and Pry)

Scanning Electron Microscopy

Applications and Examples

- Excessive wicking of copper in PTHs of a PWB
- Separation at the interface between the copper plating and the fiber epoxy resin board interface
- Fiber/resin interface delamination
- Corrosion and intermetallic growth at the bondpad under the gold ball bond
- Stress-driven diffusive voiding and hillock formation of Al metallization lines
- Metallization corrosion
- Wirebond fracture
- Passivation cracking
- Delamination at the die/die paddle interface
- Dendritic growth
- Electrostatic discharge/electrical overstress
- Wire fatigue
- Solder fatigue



Applications

- By eliminating the need for a conductive coating, SEM allows imaging of delicate structures and permits subsequent energy-dispersive X-ray spectroscopy (EDS) compositional analysis.
- An ESEM (a variant of SEM) can image wet, dirty, and oily samples. The contaminants do not damage the system or degrade the image quality.
- The ESEM can acquire electron images from samples as hot as 1500ºC because the detector is insensitive to heat.
- ESEM can provide materials and microstructural information such as grain size distribution, surface roughness and porosity, particle size, materials homogeneity, and intermetallic distribution.
- ESEM can be used in failure analyses to examine the location of contamination and mechanical damage, provide evidence of electrostatic discharge, and detect microcracks.

Limitations

- Large samples have to be sectioned to enable viewing in a SEM or an E-SEM, due to the limited size of the sample chamber.
- Only black and white images are obtained. Images can be enhanced with artificial color. Thus, different elements in the same area, having close atomic numbers may not be readily distinguished as in optical viewing.
- Samples viewed at high magnifications for extended periods of time can be damaged by the electron beam (e.g., fiber/resin delamination can be initiated this way).
- Areas having elements with large atomic number differences are not easily viewed simultaneously; increasing the contrast to view the low atomic number element effectively makes the high atomic number element appear white, while decreasing the contrast allows a clear view of the high atomic number element, the image of the low atomic number element is drastically compromised.
- Variations in the controllable pressure and gun voltage can allow samples to appear differently. Lower pressure and voltage give for more surface detail; the same surface can look smoother by just increasing the pressure. Therefore, sample comparisons before and after experiments, especially cleaning treatments should always be examined under the same conditions.
- Image quality is determined by scan rate; the slower the scan rate, the higher the quality. However, at lower scan rates, the image takes a longer time to be fully acquired and displayed. Therefore, sample movement appears visually as jerky motions. A trade off must be made between image quality and visual mobility.

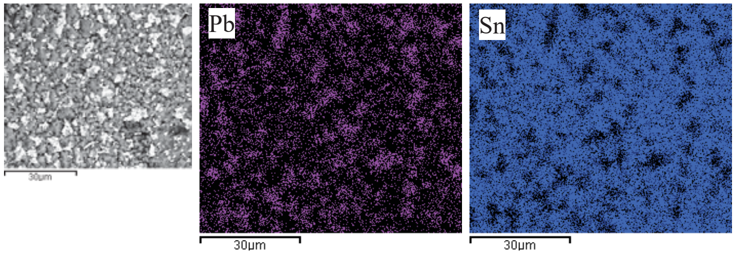
X-ray Spectroscopy

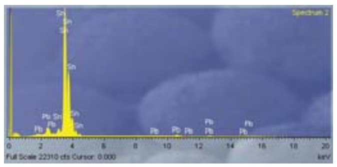
Applications

X-ray analysis can be used to detect:

- Surface contamination (chlorine, sulfur)
- Presence of native oxides
- Corrosion
- Concentrations of phosphorus, boron, and arsenic
- Compositional analysis (i.e., Sn to Pb ratio)
- Conductive filament formation
- Intermetallic growth
- Elemental distribution using mapping techniques

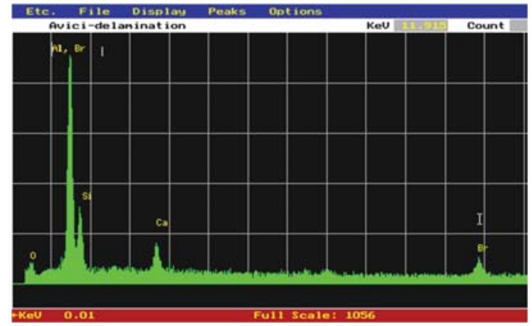
X-ray Mapping





An X-ray mapping of Tin (Sn) distribution (right) and Lead (center) in a eutectic solder. The associated spectrum is shown on left bottom.

Acquired Spectrum Using EDS



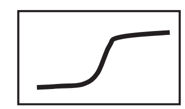
The bromine and aluminum peaks overlap, at 1.481 and 1.487 KeV respectively. It is not clear, using EDS, whether or not aluminum is in this sample. Bromine is present, as evidenced by its second identified peak at 11.91 KeV. The elemental KeV values can be found on most periodic tables.

Limitations of EDS

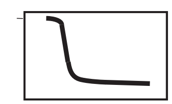
- Resolution is limited, therefore it is possible to have uncertainties for overlapping peaks (i.e., tungsten overlap with silicon and lead overlap with sulfur)
- Cannot detect trace elements
- Limited quantitative analysis
- No detection of elements with atomic number < 6
- If a Beryllium window is used, cannot detect light elements such as carbon, nitrogen and oxygen with atomic number < 9
- Specimen must be positioned in such a manner that an unobstructed path exists from the analysis site to the detector.

Thermal Analysis Techniques

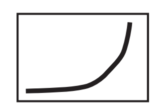
- DSC – Differential Scanning Calorimetry
  - Measures changes in heat capacity
  - Detects transitions
  - Measures Tg, Tm, % crystallinity



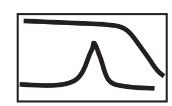
- TGA – Thermogravimetric Analysis
  - Measures changes in weight
  - Reports % weight as a function of time and temperature
  - Helps determine composition



- TMA – Thermomechanical Analysis
  - Measures changes in postion
  - Detects linear size changes
  - Calculates deflection, CTE, and transition temperature



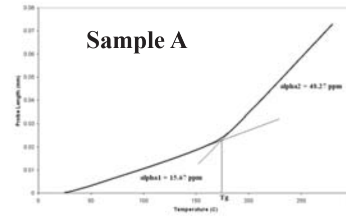
- DMA – Dynamic Mechanical Analysis
  - Measures changes in stiffness
  - Measure deformation under oscillatory load
  - Determines moduli, damping, and transition temperature



Thermal Techniques - Use

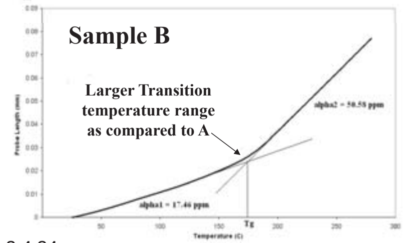
- All techniques are destructive to the sample
  - Sample will be heated above transitions
  - Will have to be cut to fit in instrument
- All techniques use small samples
  - 10 mg or so for DSC and TGA
  - Samples from 5 to 40 mm long for TMA and DMA

TMA (Samples A and B)*



- Coefficient of thermal expansion before glass transition temperature (alpha 1) and after glass transition temperature (alpha 2) is determined.
- Glass transition temperature (Tg) is also determined.

- Constant stylus force applied on the sample: 2 mN.
- Typical scan setup:
- Hold 1 minute at 25 C.
- Heating from 25° C to 280° C at 20° C/minute.



* - Sample preparation and test refer to IPC TM-650 2.4.24

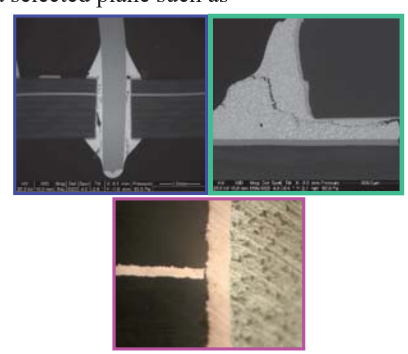
Metallographic Sample Preparation*

*- Adapted from Buehler Limited/ITW

What Is Micro-sectioning of Printed Circuit Board?

Technique used to evaluate printed wiring board quality by exposing a cross-section at a selected plane such as

- **Plated through-holes**
- Plating thickness
- Via
- **Soldered connections**
- Delamination in PCB
- **Inner layer connections**



Primary Purpose of Micro-sectioning

- To monitor the processes rather than to perform final inspection because it makes no sense to add value to a product that is already rejectable!
- Therefore, the objective is to detect any deviations from normal in the manufacturing processes as early as possible to avoid adding value to a defective product. Corrections to the process should then be made as soon as possible.

Goal of Specimen Preparation

Reveal the true microstructure of all materials

- ➢ Induce no defects during specimen preparation
- ➢ Obtain reproducible results
- ➢ Use the least number of steps in the shortest time possible
- ➢ Achieve a cost effective operation

Preparation Steps

'Each step is equally important"

- ➢ Documentation
- ➢ Sectioning
- ➢ Mounting
- ➢ Grinding and Polishing
- ➢ Visual Examination
- ➢ Etching
- ➢ Analysis

Documentation

- ➢ Process data: vendor, material, batch #, part #, sampling
- ➢ Description of specimen orientation, location, cut area, Macro image
- ➢ Type of analysis and defect, area of interest
- ➢ Record mounting, polishing, etching parameters
- ➢ Record microstructure data: inclusions, porosity, grain size, etc.

Sectioning

- Equipment
- Blade, wheel (SiC, alumina, diamond)
- Load
- Blade RPM
- Feed rate
- Coolant
- Delicate materials may require encapsulation or chuck padding for holding

Methods

Method	Comments
Shearing	Severe torsion damage to an undetermined distance adjacent to the cutting edges
Hollow punch (Saved hole)	Convenient, and rapid but limited to boards 0.08" thick or less
Routing	Rapid and versatile with moderate damage but noisy and hard to control.
Band saw	Rapid, convenient moderate damage and easy to control when a 24-32 pitch blade is used at 3500-4500 ft./min.
Low speed saw	Least damage of any method allowing cuts to be made even into the edge of the plated through-hole barrel. However, it is too slow for high volume micro-sectioning.
Precision table saw	Least destructive method of removing specimens from component mounted boards for soldered connection analysis

Sectioning damage

Method	Type of damage	Possible depth
Shearing	Deep mechanical damage	5 mm
Band / hack saw lubricated not cooled	Moderate thermal and mechanical damage	2.5 mm
Dry abrasive cutting	Moderate to severe thermal damage	1.5 mm
Wet abrasive cut-off saw	Minimal thermal and mechanical damage	250 µm
Diamond / precision saw	Minimal thermal and mechanical damage	50 µm

Mounting Principles

- Sample encapsulated in epoxy, acrylic or other compound
- Sample edges protected during polishing process
- Delicate samples protected from breakage
- Smooth mount edges increase life of polishing surfaces
- Allows automation and ability to prepare multiple samples simultaneously
- Uniform pressure on mount maximizes surface flatness
- Safety

Mounting Method Selection

Castable (cold) mounting
•Resin/hardener selection
•Vacuum
•Additives for edges, conductivity

Compression (hot) mounting
• Compound selection
• Pressure
• Heat

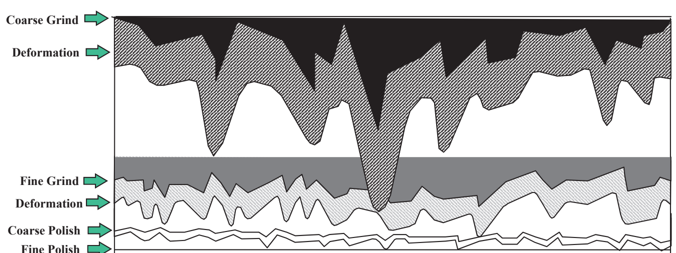
Specimen characteristics to consider:
•Softening/melting temperature
•Sample thickness, ability to withstand pressure
•Brittleness, friability
•Porosity
•Hardness & abrasion resistance relative to mounting compound
•Importance of edge retention

Potting Compounds

Resin of Choice?…EPOXY!

- **Low shrinkage and moderate hardness are important for microelectronics.**
  - **Less surface relief**
  - **Better edge protection**
- **Uncured epoxy typically has low viscosity for filling small cavities.**
- **Epoxy can be cast while under vacuum. This enhances its cavity filling ability.**

Damage



<u>Incremental Removal of Damage</u>
Each abrasive step leaves deformation. As abrasive size is reduced, less deformation is left behind.

Grinding Steps

- The initial grinding surface depends on the condition of the cut surface – more damaged surfaces require coarser first-step grinding
- For excessive damage, re-sectioning with an abrasive or precision saw is recommended
- A single grinding step is adequate for most materials sectioned with an abrasive or precision saw
- Softer materials require multiple grinding steps and smaller abrasive size increments
- Remove damage with progressively smaller abrasive particle sizes
- With decreasing particle size:
  1. Depth of damage decreases
  2. Removal rate decreases
  3. Finer scratch patterns emerge

Polishing Principles

- Further refinement of ground surface using resilient cloth surfaces charged with abrasive particles
- Depending on material characteristics, cloth selected may be woven, pressed or napped
- Commonly used abrasives are diamond and alumina
- The polishing process consists of one to three steps that:
  1. Remove damage from the last grinding step
  2. Produce progressively finer scratches & lesser depth of damage
  3. Maintain edges and flatness
  4. Keep artifacts to an absolute minimum

Time

- Each step must remove the surface scratches and sub-surface deformation from the previous step
- Increase time to increase material removal
- Smaller increments in abrasive size require shorter times at each step
- Increases in surface area may require longer times
- Too long times on certain cloths can produce edge rounding and relief

Additional Considerations

- Bevel mount edges to increase cloth life
- Clean specimens and holder between steps to prevent cross contamination of abrasives
- Ultrasonic cleaning may be required for cracked or porous specimens
- Dry thoroughly with an alcohol spray and a warm air flow to eliminate staining artifacts
- Remove polishing debris by rinsing cloth surface after use to increase cloth life

Final Polishing Principles

- Removes remaining scratches, artifacts and smear
- Produces a lustrous, damage-free surface
- Maintains edge retention
- Prevents relief in multiphase materials

Etching Principles

- Etching is a process of controlled corrosion
- Selective dissolution of components at different rates reveals the microstructure
- Completion of etching is determined better by close observation than timing
- Etching is best performed on a freshly polished surface before a passive layer can form
- A dry surface produces a clearer etched structure than a wet one
- An under-etched surface may be re-etched but an over-etched surface requires re-polishing

Etching Techniques

- Immersion – sample immersed directly into etchant solution
  - Most commonly used method
  - Requires gentle agitation to remove reaction products
- Swab – polished surface swabbed with cotton ball soaked with etchant
  - Preferred method for materials in which staining is a problem
- Electrolytic – chemical action supplemented with electric current
  - Attack controlled by chemical selection, time, amps

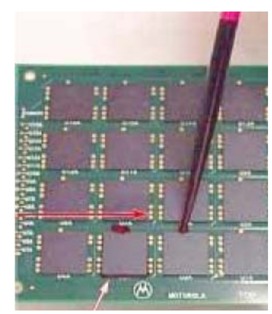
PWB Etchants (For Copper)

- Equal parts 3% H_2O_2 and ammonium hydroxide, swab for 3 to 10 seconds, use fresh etchant to reveal grain boundaries of plating and cladding copper material.

- 5 g $Fe(NO_3)_3$, 25 mL HCl, 70 mL water, immerse 10 – 30 seconds, reveals grain boundaries very well.

Dye Penetrant (Dye and Pry)

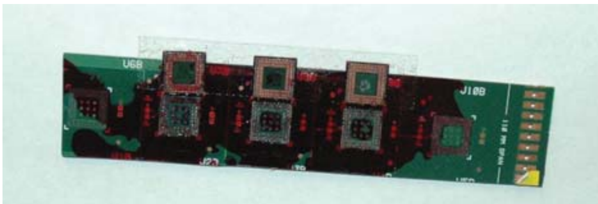
- Identify failed components (electrical measurement)
- Boards are immersed in stripping agent (Miller-Stephenson MS-111) for 25 min at room temperature to remove the solder mask. IPA can be used for a final rinse. Dry in air.
- Dye is applied to the board (DYKEM steel red layout fluid) with a pipette. Important: Flip the board, so that the dye flows into the cracks
- Place boards in vacuum for 5 minutes so that the dye penetrates into fine cracks that otherwise would be blocked by trapped air pockets. A strong vacuum pressure is not important for this process (Typical 220 mm Hg)
- Place the board on a hot plate for 30min 80° C to dry the dye (as prescribed by DYKEM).



Picture: "Solder joint failure analysis" **Dye penetrate technique BY TERRY BURNETTE and THOMAS KOSCHMIEDER**

Dye and Pry Steps

- Flex the board with a pair of pliers until the components peel away.
- Remove the components with tweezers and fix with double sided tape on the board, because it is important to see the component side and the substrate side to identify the failure site.

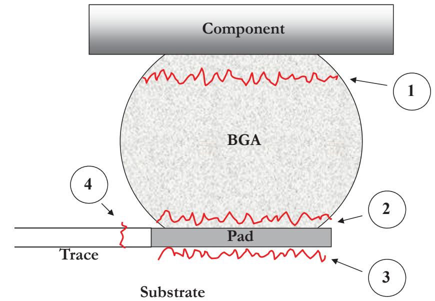


Picture: "Solder joint failure analysis" **Dye penetrate technique**
BY TERRY BURNETTE and THOMAS KOSCHMIEDER

Potential Nonconformities

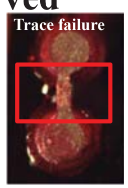
(For BGAs)

1. Solder Fail (component side)
2. Solder Fail (substrate side)
3. Pad Lift
4. Trace Fail



Dye and Pry: Failure Sites Observed

(a) Failure on board side



(b) Trace failure

(b) Failure on component side

(d) Pad crater

Focused Ion Beam Etching

FIB Introduction

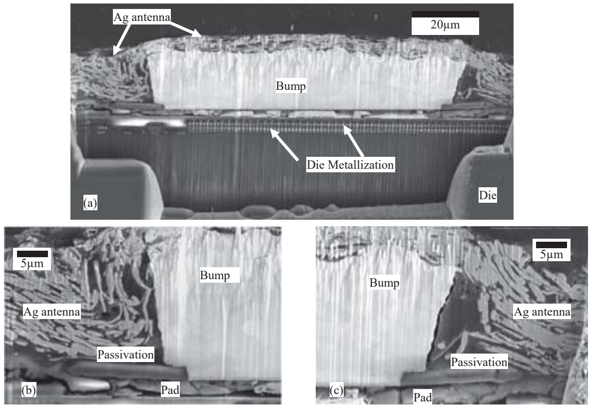
- Focused ion beam (FIB) processing involves directing a focused beam of gallium ions onto a sample.
- FIB etching serves as a supplement to lapping and cleaving methods for failure. The beam of ions bombarding the sample's surface dislodges atoms to produce knife-like cuts.

FIB Cross-section of Bumps

SEM image of a die-bump interface after FIB etching. Overview of the interface in

(a) shows the bump, die and silver antenna,

(b) and (c) show close up of the bump at two sides.



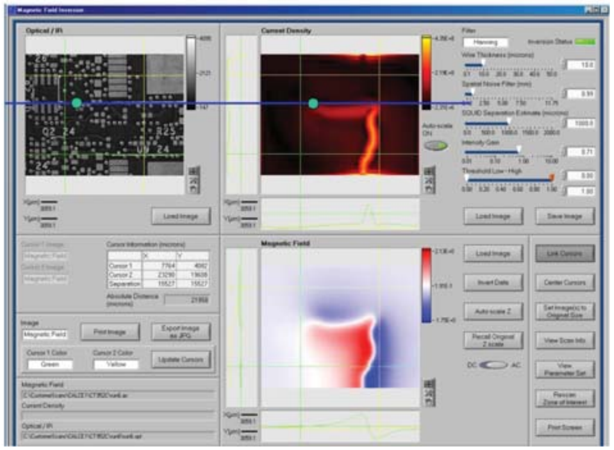
Ref: Sood, Bhanu, et al. "Failure site isolation on passive RFID tags." Physical and Failure Analysis of Integrated Circuits, 2008. IPFA 2008. 15th International Symposium on the. IEEE, 2008.

Focused Ion Beam Limitations

- Equipment is relatively expensive
- Large scale cross-sectional analysis is impractical since the milling process takes such a long time
- Operator needs to be highly trained
- Samples could be damaged or contaminated with gallium
- Different materials are etched at different rates, therefore uniform cross-sectioning using ion milling is not always possible

Superconducting Quantum Interference Device (SQUID) Microscopy

Magnetic Imaging Used to Locate Failures



Ref: Sood, Bhanu, and Michael Pecht. "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602-1615.

Site Isolation of CAF in PCBs Using SQUID[1]

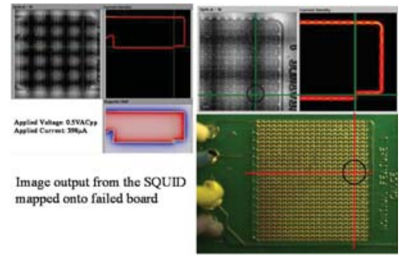
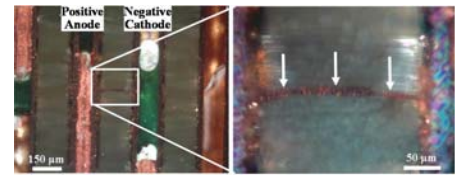


Image output from the SQUID mapped onto failed board

- Scanning quantum interference device (SQUID) microscope is a sensitive near-field magnetic imaging system.
- System can detect magnetic fields as faint as 20 picotesla. Its sensitivity is high enough to image currents as small as 600nA at a 100 mm working distance with 30 ms averaging.



- Bias is applied to the test boards suspected of CAF failures.
- Magnetic field produced by a sample can be imaged by rastering the sample in close proximity to the SQUID, magnetic field maps are generated.

[1] Sood, Bhanu, and Michael Pecht. "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602.

Spectroscopy, including Fourier Transform Infrared Spectroscopy (FTIR)

Fourier Transform Infrared Spectroscopy – Spectrum Production

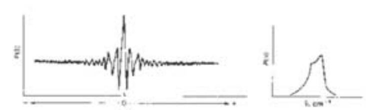
Non-absorbed Light (e.g., Reflected or Transmitted) ← Sample ← Incident Light

↓

Detector

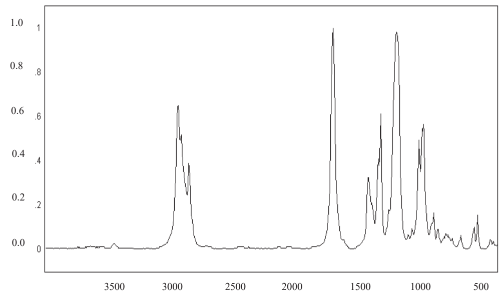
↓

Interferogram (Time Domain) → Fourier Transform → Spectrum (Frequency Domain)



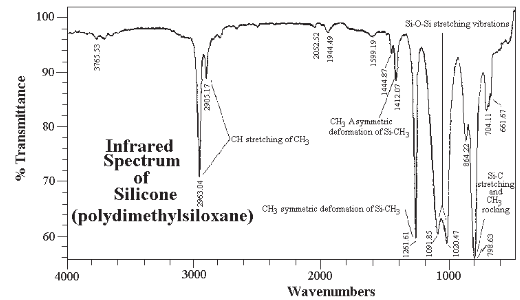
Properties of an Infrared Spectrum

- An infrared spectrum contains absorption peaks corresponding to the frequencies of vibration of the atoms of the molecules making up the sample.



Infrared Spectrum of Acetic Acid Butyl Ester

Fourier Transform Infrared Spectroscopy – Spectrum Interpretation



Correlation with charts of characteristic absorption frequencies → Identification of material

Ref: ChemAnalytical LLC: FT-IR Spectra

Engineering Applications of FTIR

- Materials identification and evaluation
  - Identification of unknown inorganic and organic materials by comparison to standards and by molecular structure determination
  - Determination of the locations of known and unknown materials
  - Determination of material homogeneity
- Failure analysis
  - Identification of contaminants
  - Identification of corrosion products
  - Identification of adhesive composition change
- Quality control screening
  - Comparison of samples to known good and known bad samples
  - Comparison of materials from different lots or vendors
  - Evaluation of cleaning procedure effectiveness
  - Identification of contaminants

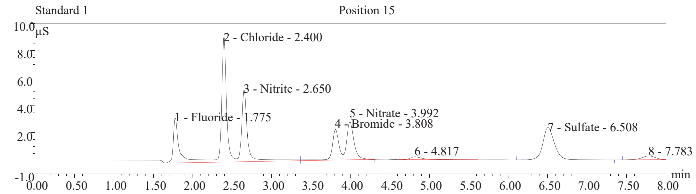
Chromatography

Ion-exchange Chromatography

- Ion exchange chromatography exploits ionic interactions and competition to realize analyte separation.
- It can be further classified into
  - cation exchange chromatography (CEC): separates positively charged ions; and
  - anion exchange chromatography (AEC): separates negatively charged ions.
- The output of an IC test is a graph of conductivity versus time.
- Calibration is with standards of known composition (elution time) and concentration (peak area).

Example of IC Results on a Mixture of Anions

- The eluent was 0.01 mol/L NaOH.
- The column used was an Dionex AS11.



- Based on the retention time, the type of ions can be determined with comparison to standard ions.
- Based on the area under the peaks, the concentration of the ions can be determined.

Ref: Dionex AS11 Carbon Eluent Anion-Exchange Column

Applications of Ion Chromatography in Electronics Reliability

1. Tests on assembled or bare printed wiring boards (PWBs) to relate cleanliness to electrochemical migration.
2. Determination of amount and type of extractable ions present in encapsulation materials to relate amount and type of ionic content to corrosion failure.
3. Electroplating chemistry analysis to relate breakdown products to plating adhesion failure.

Ref: IPC-TM-650 Test Method No. 2.3.28

Summary

Restart Criteria

- Failures with severe consequences (e.g., safety) may require processes (e.g., manufacturing, distribution) to be interrupted after discovery of the failure.
- Depending upon the identified root cause, processes interrupted may be re-started if **corrective action** (s) can be implemented that will prevent the recurrence of the failure, or sufficiently minimize its impact.

Corrective Actions

- Many of the failures having a direct impact on production require **immediate corrective actions** that will minimize downtime.
- Although many immediate actions may correct symptoms,
  - temporary solutions may not be financially justifiable over the "long haul"; and
  - there is a large risk that a temporary solution may not solve the problem.

Verification

Verification of the corrective action includes:

- verifying the approval and implementation of the corrective action;
- verifying a reduction in the incidence of failures;
- verifying the absence of new failures associated with the failure sites, modes, and mechanisms identified during the failure analysis.

Root Cause Analysis Report

The report should include the following information:

1. Incident summary
2. History and conditions at the time of failure
3. Incident description
4. Cause evaluated and rationale
5. Immediate corrective actions
6. Causes and long-term corrective actions
7. Lesson learned
8. References and attachments
9. Investigating team description
10. Review and approval team description
11. Distribution list

Failures of a Failure Analysis Program

- Shutting down the malfunctioning equipment
- Refusing to recognize that a failure can or does exist
- Assuming an apparent cause to be the root cause
- Determining the failure cause by assumption
- Collecting insufficient information and ending an analysis before it is complete
- Discarding failed parts
- No documentation

Questions?

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✷NASA GSFC SMA Mission Assurance Directorate
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