Miniaturization, Packaging, and Thermal Analysis of Power Electronics Modules

by

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EXECUTIVE SUMMARY

High power circuits, those involving high levels of voltages and currents to produce several kilowatts of power, would possess an optimized efficiency when driven at high frequencies (on the order of MHz). Such an approach would greatly reduce the size of capacitive and magnetic components, and thus ultimately reduce the cost of the power electronic circuits. The problem with this strategy in conventional packaging, however, is that at high frequencies, interconnects between the power devices on one board (such as Power MOSFETs or IGBTs) and components on another board (such as the coasting diodes) suffer from severe parasitic effects, thus affecting the overall electrical performance of the system. A conceivable solution to this problem is the design and construction of a power electronics module which would incorporate all power devices and supporting circuitry into one very simple and compact module. Such an approach would reduce interconnect inductances (thus reducing costly parasitic effects), increase system efficiency and electrical performance, produce a standardization for power electronic modules, and through this standardization, lower overall industry-wide system costs and increase power electronic system reliability. This technology would prove especially valuable for power electronics in industry, where prevalent power systems such

as half bridge or full bridge converters would benefit greatly from the large reduction of inductances which currently exist between separate bridge legs.

This thesis will discuss a novel multilayer approach towards the described issues. A power module has been designed and fabricated which contains one metallization power layer for the power devices, and a second metallization control layer for the low power signal components. The two layers are separated by a dielectric layer which serves as an electrical separation and as a physical spacer. In addition, issues have been addressed towards optimal physical layout and construction (with regards to thermal dissipation), materials comparisons have been made, and thermal simulations and experimental verifications performed.

Issues relating to standardized power electronic module design and the efforts of this researcher at the Microelectronics Laboratories at Virginia Polytechnic Institute and State University to contribute to this quickly evolving field will be discussed. Such topics as power electronic module design, control and driver circuitry design, material issues, and thermal issues will be discussed.

Acknowledgments

Trust your wings to lift you, and though at first you may feel as if you're falling, in the end it is towards the heavens that you will fly. To do this though, you must make that initial step of faith into the unknown.

I would like to first and foremost thank God for allowing me this opportunity to follow my dreams. Next I would like to thank my advisor, Dr. Elshabini, for her continued dedication and support of my research. Without her faith behind me and my work, I possibly would never even have been given this chance at graduate school. I would also like to thank my other Committee members, Dr. I. Besieris, and Dr. S. Raman for taking the time to serve on my committee.

I would like to thank my friends and family, my mother, father, sister, and grandmother for their love and support. I would like to thank Dan L. for his continued persistence in driving me on to be the best I can be (a little competitiveness is always helpful). I would like to thank Fred, Rich, and James for their assistance in my work, their helpfulness in helping me uncover problems, and of course for not laughing *too* hard when I blew things up. And if I did blow things up, Brett was always willing to go for a drink. I would like to thank Dan W., Ken, and Mary for their friendship through all of these years and their belief that I could accomplish anything I set my mind to. And finally, for all of those long days when nothing at all was going right, and when the work seemed never ending, I want to thank Rebecca for her uncanny ability to continuously lift my spirits. Thank you all.

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CHAPTER 1.

INTRODUCTION

The ultimate goal this research is leading towards is to produce an industry-wide standardized power electronics module that will form the basis for any power electronics system. Such a power module would prove to be more efficient then current power electronic systems, and it would greatly reduce engineering and system costs.[1]

Current achievements by the Microelectronics Laboratories include the design, the fabrication, and the operation of power electronic modules which have incorporated within them all of the power devices and supporting circuitry of a half bridge converter circuit. This half bridge converter has been tested and operated under a 3kW load, and has also shown the feasibility and realizabilty of the multilayer power module concept

The most significant problem with the power electronic module concept is the issue of adequate thermal management and consequent electrical performance. With high power running through dense circuitry comes the undesirable side effect of an intense heat source. This heat brings out two significant requirements that the materials within the module must meet in order for satisfactory operation to be obtained. The first requirement is that the materials must have a high thermal conductivity in order to adequately dissipate the produced heat to the heat sink. The second requirement is that the materials within the multilayer module must have matched low coefficients of thermal expansion (CTE) in order for the module to remain structurally intact. It is believed that a Metal Matrix Composite (MMC) heat spreader, with its high thermal conductivity and low CTE has the potential to solve many of these thermal management issues. An MMC is a

relatively new state of the art material in which metal is injected into a ceramic matrix composite. These combines the advantageous characteristics of both materials, resulting in a light weight, structurally strong material with a high thermal conductivity and low coefficient of thermal expansion.

The objective of this research was to address these critical issues in order to design, construct, package, and test the basic power module design within the Microelectronics Laboratories at Virginia Polytechnic Institute and State University. Three areas of investigation were undertaken.

The first task was to design the drive and control circuitry that would switch the half-bridge power converter, and to create a testbed for power electronics module measurements and evaluations. An International Rectifier Control Chip was chosen as the single phase controller to drive the pair of IGBTs (Insulated Gate Bipolar Transistors) found in the half bridge power converter. A considerable amount of effort was involved in damping gate spikes that had a tendency to destroy the transistors, and negative spikes that would incapacitate the chip controller.

The second task was to investigate fabrication procedures for a multilayer approach to power module construction. Direct Bond Copper (DBC) and polymer adhesion techniques were combined with industry standard Printed Circuit Board (PCB) technologies to create an approach that was effective as well as low cost.

The third task was to investigate the use of various thermal heat spreaders, including AlSiC MMC, AlN MMC, and comparing those with copper based heat spreaders. The task included three dimensional thermal simulation and analysis of power modules, and comparing that analysis with experimental results. It was found that by replacing the industry standard conventional copper heat spreader with more advanced MMC materials, improved CTE matching could be obtained without sacrificing thermal conductivity performance.

Through this research, the feasibility of a multilayer power electronics module has been demonstrated, and wirebond modules were designed, constructed, fabricated, operated, and tested unbder a high power load. In addition, the advantages of MMC materials as heat spreaders has been shown through the analysis of three dimensional thermal simulations of various power electronic modules.

CHAPTER 2.

THE BASIC THEORY OF POWER TRANSISTOR DEVICES

The eventual goal of this research is the realization of the power electronics module as the standard for the power electronics industry. Such a power module would prove to be more efficient then current power electronic systems, and it would greatly reduce engineering and system costs. It was therefore important to identify a simple yet applicable power electronics operation and to design a circuit to achieve that operation. The operation and power electronics circuit selected was a single phase half bridge power converter (illustrated in Figure 2.1); it is a simple circuit in configuration and yet it has a large number of industry-wide applications.

The first real design consideration involved the selection of the proper power transistor for circuit operation. Considering that the eventual application of a half bridge converter power module will be to switch high power at high frequencies, two transistor types were singled as the prime candidates for the power electronics module.[2]

The first transistor devices under consideration were the power metal oxide semiconductor field effect transistors, or power MOSFETs. These power devices were

developed in the 1970s, advancing from the MOS integrated circuit technology of the time.

The double-diffusion MOSFET, or DMOSFET (illustrated in Figure 2.2) has been the most commercially successful structure of the MOSFET family; it is more stable then the older V-groove MOSFET, and the new U-groove MOSFET has just begun to become commercialized.[3] The DMOS structure is constructed through the use of planar diffusion technology utilizing refractory gates (such as using polysilicon as a mask). The P^- region and the N^+ source regions are diffused through a common window defined by the polysilicon mask, and the difference in the lateral diffusion between the P^- and N^+ source defines the surface channel.[4]

The power MOSFET is a unipolar device in which current conduction occurs through the transport of majority carriers in the drift region without the presence of minority carrier injection (such as is required for bipolar transistor operation). It contains a high impedance input which greatly simplifies drive circuitry and allows a bias voltage with very low current (on the order of 100nA) to act as the gate control signal. The gate control signal is applied to a metal gate electrode which is separated from the semiconductor surface by an intervening insulator such as a silicon oxide. Due to the low gate current and the device switching operation, the inherent switching speed orders of magnitude greater then the older conventional bipolar transistors, making it an attractive device for circuits operating at high frequencies (where switching power losses dominate).[5]

These advantages of the power MOSFET devices, however, are somewhat diminished by their conduction characteristics which are highly dependent upon temperature and voltage rating. A solution to this problem was the advent of the insulated gate bipolar transistor or IGBT (illustrated in Figure 2.3).

IGBT devices have a virtual identical cross-section as that of the power MOSFET devices. Both types of devices share the same polysilicon gate structures, as well as the similar P wells with N^+ source contacts. However, the physical operation of the IGBT is much closer to the operation of a BJT than a MOSFET. If one inspects Figure 2.2 and Figure 2.3 closely, one will notice that the main difference between the two devices is the presence of a P^+ substrate layer in the IGBT. It is because of this layer that the IGBT device is a minority carrier transistor, and that layer is accountable for the minority carrier injection into the N-region and the consequential conductivity modulation. This device difference accounts for the power MOSFET's shortcomings, for the device does not benefit from the conductivity modulation, and consequentially a significant portion of the MOSFET's conduction losses occur in the N-region (approximately 70% in 500V devices).[6] This change in configuration does have *some* negative impact on the IGBT device, however. The reverse and blocking behaviors of the device are affected, and the result is an inferior gate switching speed performance as compared to a power MOSFET.[7] Even though there is a degradation in gate switching speed, the IGBT's advantages over the MOSFET far outweigh its disadvantages, including a massive reduction in the voltage drop, a reduction in the temperature dependence, and a virtual elimination of its dependence upon the voltage rating (as illustrated in Table I).

Table I: Dependence of Voltage Drop from Voltage Rating

Device	Voltage Rating (V)	Voltage Drop (V)
IGBT	100	1.5
	300	2.1
	600	2.4
	1200	3.1
Power MOSFET	100	2.0
	250	11.2
	500	26.7
	1000	100

Typical switching frequencies of IGBTs range from 20kHz-50kHz, while Power MOSFETs often operate at several hundred kilohertz. If the switching speed of the power circuitry is the absolute most important performance characteristic, then the MOSFET devices can be paralleled in order to alleviate some of the problems related to the voltage rating dependency and the voltage drop. As previously stated, one of the more important aspects of the power electronics module is to make it as simple and compact as possible; therefore, the number of devices involved is a very important issue to consider. For this reason, the minor loss in switching speed is far outweighed by the advantages of using only two IGBT devices.

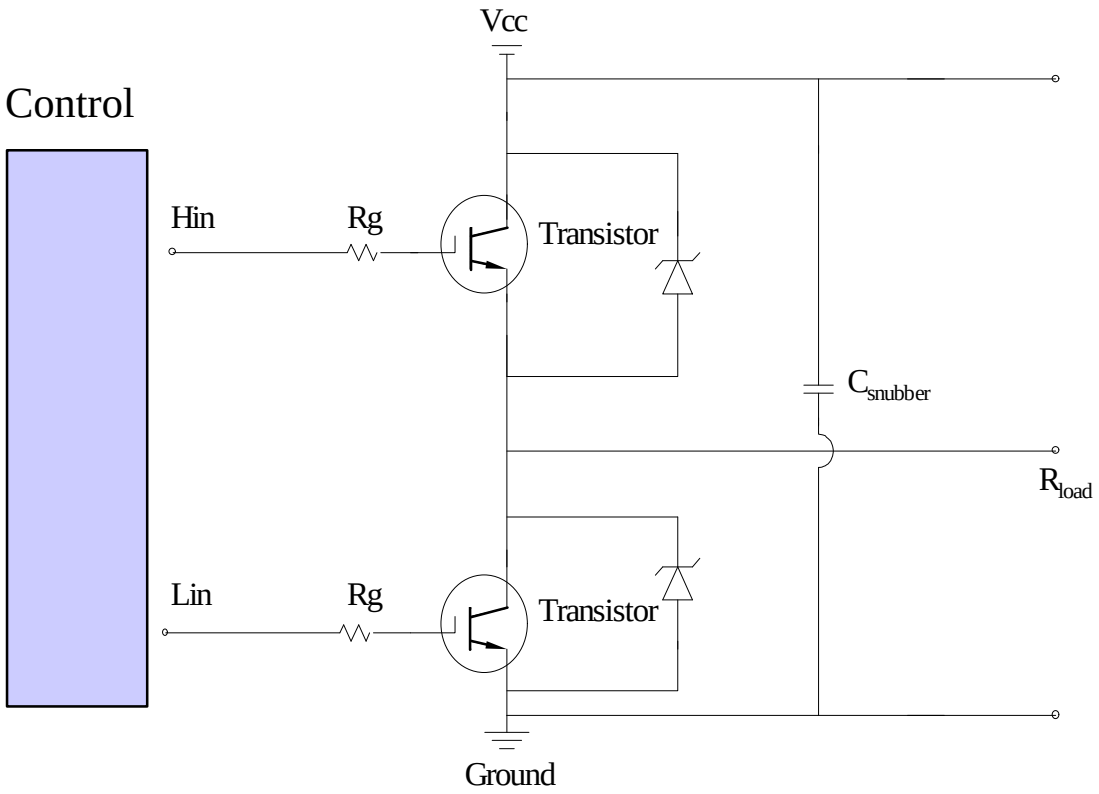


Figure 2.1: Typical Half Bridge Power Converter

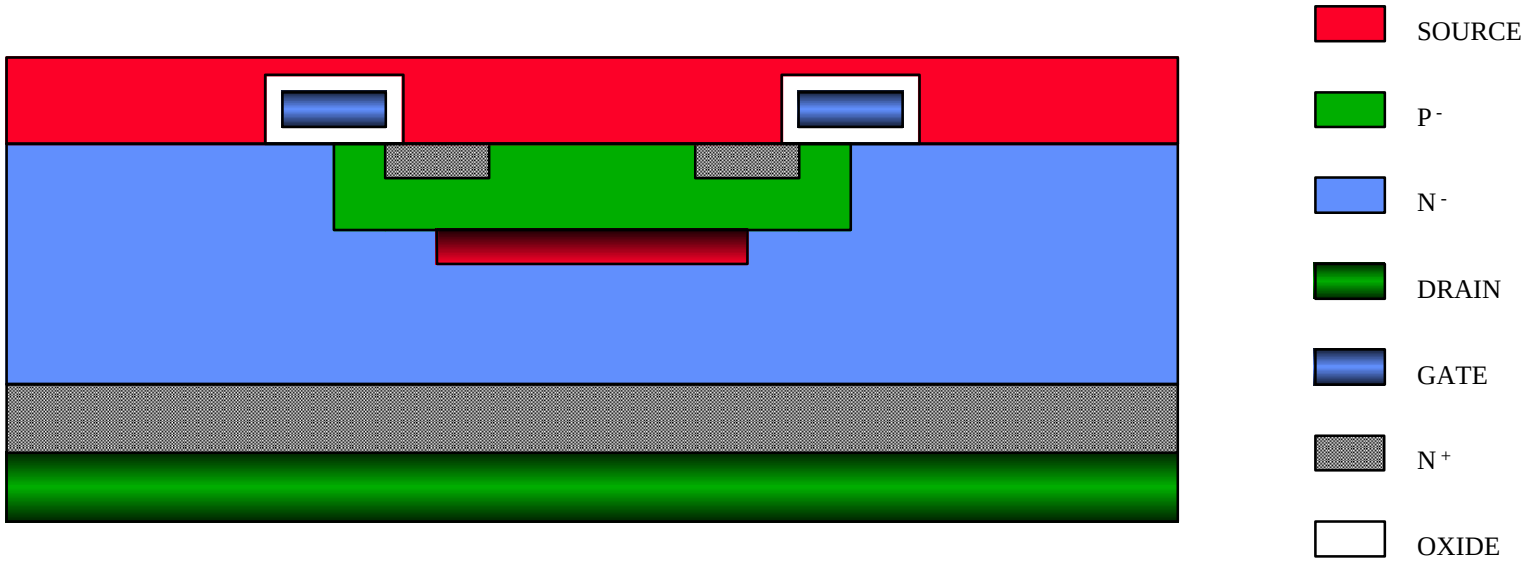


Figure 2.2: Cross-section of Power DMOSFET Device

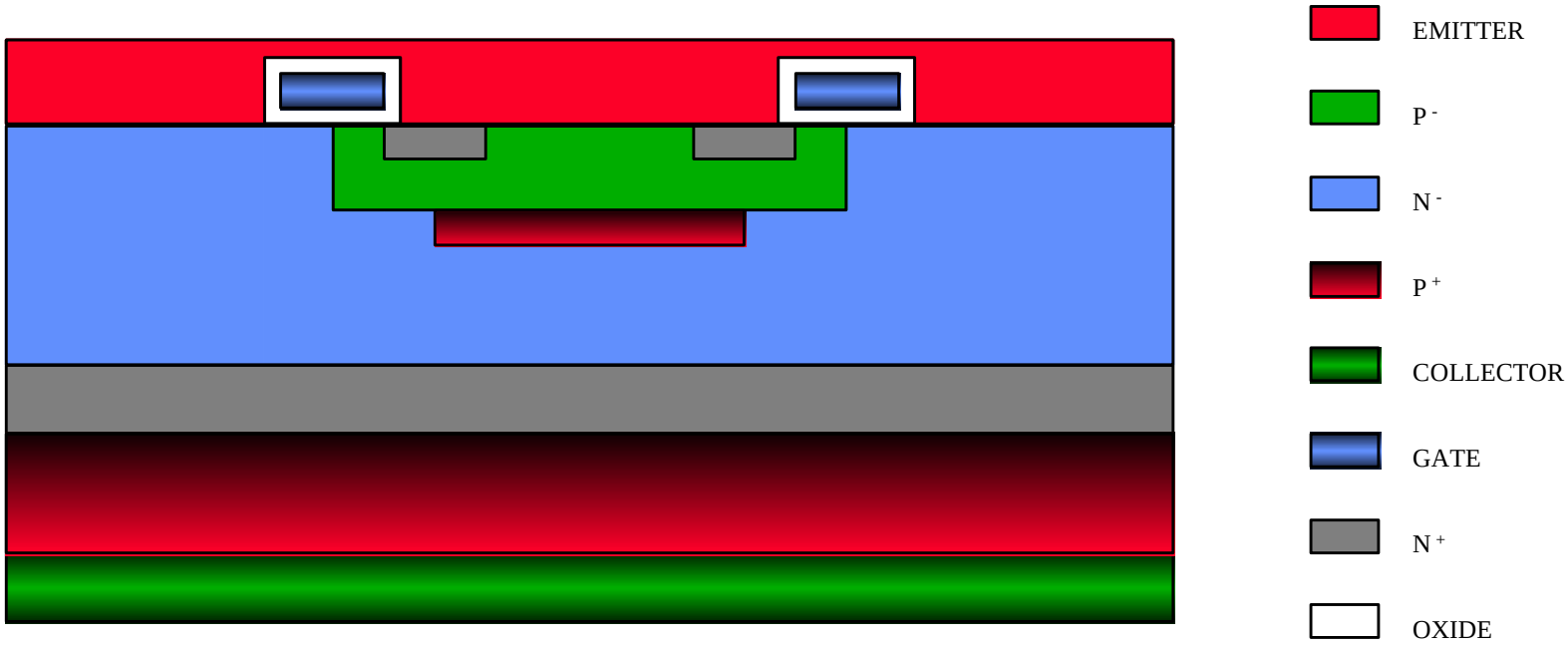


Figure 2.3: Cross-section of IGBT Device

CHAPTER 3.

POWER ELECTRONICS CIRCUIT DESIGN THEORY

3.1 Introduction to Power Circuit Design

Power electronic circuits are those circuits which alter the characteristics of the electrical energy provided by a source to those characteristics which are required by the load. Power circuits can be divided into three basic categories; DC/AC converters, DC/DC converters, and AC/AC converters, each with a number of topologies and design approaches. One design topology applicable to both DC/AC converters and DC/DC converters is the use of a half-bridge configuration. As one of the goals of this research is the standardization of power modules, it was therefore decided to focus on the half-bridge layout utilizing PWM (pulsewidth modulated) switching. The overall circuit design process of a power converter can be divided into a number of steps including; circuit fundamentals, transformer and magnetics design, output filter design, power switch design, controller and drive design, feedback design, circuit start-up design, and protection design.[8, 9] The emphasis of this research is on the packaging design, so all of the mentioned basic design steps will not necessarily be utilized.

3.2 Pulsewidth Modulated Switching Basics

Efficient operation of PWM switching supplies is achieved by chopping the DC input voltage into rectangular pulses which have an amplitude magnitude equal to the voltage level of the DC source. That waveform can then be stepped up or down to the desired level through the utilization of a magnetic component (transformer) and then properly filtered to acquire the desired AC or DC output. The frequency and duty cycle of the rectangular waveform are defined as the pulsewidth modulation functions.

3.3 Circuit Fundamentals and Topology [10]

The first required step in designing the power converter circuit is deciding upon the circuit's required power capabilities, input and output maximum voltage and current levels, and the conversion requirement (DC/AC or DC/DC). From this information, the proper circuit topology can be chosen.

3.3.1 Buck Topology

The buck converter, also known as a down converter, simply takes a DC voltage source and converts it to a DC output at a lower level. Figure 3.1 illustrates a direct down converter. When the series transistor closes, the shunt diode is forced into a reversed biasing condition, and when the series transistor opens, the continuity of the inductor current forces the diode into conduction. In this topology, the inductor and capacitor components are of sufficient values to eliminate switching frequency components.

3.3.2 Boost Topology

The boost converter illustrated in Figure 3.2, also known as an up converter, works exactly opposite of the buck converter. In this configuration, the transistor and diode switches are exchanged as are the voltage inputs and outputs.

3.3.3 Buck/Boost Topology

The buck/boost converter illustrated in Figure 3.3 combines the buck and boost topologies so that the DC voltage output level can be either higher or lower then the DC input voltage level (depending on the selected switching duty cycle). The inductor and capacitors are chosen so as to remove any undesirable ac ripple components which may be present in the waveforms.

3.3.4 Flyback Topology

The flyback converter illustrated in Figure 3.4 is an indirect DC/DC converter utilizing a filter inductor for isolation purposes, and a transformer for energy storage purposes. During the first part of the switching cycle, the primary winding of the transformer takes energy from the input and stores it in the magnetizing inductance. During the second part of the cycle, the secondary winding removes the energy and delivers it to the load. The transformer in this case steps the input voltage up or down to the desired output voltage level. Thus the circuit has the functionality of a buck/boost converter, except that the power switch is isolated from the load.

3.3.5 Half-Bridge Topology

The half-bridge topology illustrated in Figure 3.5 utilizes two power transistors to "chop" the DC source voltage into a rectangular waveform. This AC waveform can then be stepped up or down (through a transformer), and filtered as desired if filter is placed on the output.

3.3.6 Push-Pull Topology

The push-pull converter illustrated in Figure 3.6, also known as the transformer coupled half-bridge, operates similar to the half-bridge converter. The switch outputs are centertapped to the transformer's primary winding.

3.3.7 Full-Bridge Topology

The full-bridge converter illustrated in Figure 3.7, again works similar to the half-bridge topology, except that the switching duties are shared by two transistors performing the same function (thus two switches are on while the other two are off). This topology is used to relieve stresses from the devices, however a problem arises; if an imbalance occurs, the power will not be shared equally between the two performing switches. A catastrophic failure of one of the switches could result from this imbalance.

3.4 Transformer and Magnetics Design

The transformer of the power electronic circuit performs one or more of several possible functions, depending upon the operational mode of the switching devices and the overall circuit topology. In a forward mode operational circuit, the transformer serves as an isolation barrier between the input and output, and it serves to step up or down the pulsewidth modulated input voltage signal. The function of the transformer in the flyback mode is different. Energy in this transformer is stored within the core material by the primary winding and transferred to the secondary when the primary turns off.

The primary function of the circuit inductors is to provide energy storage for filtering purposes. The inductor acting as a storage element converts a rectangular waveform into a DC output, with additional filters reducing the observed ripple to acceptable levels.

Since magnetics were not used in this research, further detail as to the steps involved in the actual design of inductors and transformers will not be discussed.

3.5 Output Filter Design

The output filter of a power circuit is responsible for rectifying and filtering the switching ac waveform into the desired voltage output waveform. The output filter's physical layout and circuit design is very important in regards to efficiency and circuit reliability. As stated, inductors and capacitors play a large role in diminishing ac ripples and producing the desired output signals. For purposes of this research, capacitors were

used to remove parasitic spikes at the source and load, but otherwise no filtering was performed to change the output waveform from its rectangular shape.

3.6 Power Switch and Driver Design

The main purpose of this stage is to convert a DC input waveform to a rectangular AC output waveform, and central to that function is the power switch. This is the foundation and central idea upon which most power converters are based. The AC waveform can then be stepped up or down to the desired voltage level, and then that waveform can be filtered to produce an AC or DC output. Much detail has already been given on the advantages and disadvantages of both Power MOSFETs and IGBTs, along with the proper utilization of these devices within the circuit topology. Voltage and current maximum levels, as well as the switching frequency of operation are important factors that need to be taken into consideration here.

3.7 Controller and Driver Design

The control and drive circuitry of the power electronics circuit centers around an IC chip that typically performs the PWM functions of switching frequency and duty cycle control, feedback control through a voltage error amplifier, and supplying the proper drive to the power devices. The more complicated circuits replace voltage controlled feedback with current controlled feedback and variable frequency control. All of the functions stated here are typically performed by a PWM IC. The PWM's drive outputs are then sometimes used to drive a Driver IC. This is especially the case in higher power

applications where additional current levels may be required to overcome the capacitave effects of the power devices in order to turn them on.

3.8 Feedback Design

The feedback of a circuit can be divided into three basic categories, voltage controlled feedback, current controlled feedback, and variable frequency control (which is based upon voltage controlled feedback).

Voltage controlled feedback, as illustrated in Figure 3.8, can be achieved by a comparator following a voltage error amplifier. The amplifier's output is compared to the ramp voltage across a timing capacitor. The disadvantage of this method is that it can not protect against instantaneous overcurrent conditions in the power switch due to core saturation, and it exhibits a fairly slow response time.[11, 12]

Current controlled feedback includes an ac current feedback loop in addition to the previously mentioned voltage feedback. This method can be achieved by running the output of the error amplifier into the input of a comparator that compares the error voltage against the instantaneous switching current. The controller, through this method, is able to detect a voltage surge or an impending core saturation condition. This thus makes the current controlled feedback more robust, though more costly.[13, 14]

Feedback control is highly dependent upon circuit application and desired load levels, so again feedback is not a high priority within this research. Control and drive chips utilizing a fixed frequency and duty cycle control were used instead for sake of simplicity.

3.9 Circuit Start-up Design

The start-up and supply circuitry provides the IC supply voltage from the main DC rail or from a feedback. Typically, there are two portions of the supply circuitry. The first powers the ICs under initial start-up conditions as the power circuit turns on from a totally unpowered state. After start-up, this portion of the circuit becomes disabled as a second circuit kicks in. The first circuit is less efficient as it draws power from the main DC rail. The second supply circuit is tapped into the inductor or transformer of the power stage and draws the necessary power from its own output. When this second circuit turns on, the first turns off.

These designs were eliminated in this research by simply supplying the power module with two separate DC bias levels, a 15V DC for the control and driver chip, and a high power DC voltage for the power stage.

3.10 Protection Design

Protection from catastrophic failure is an important design consideration when engineering a power electronics circuit. All of the protection mechanisms trace back to protecting the supply and loads first, and then the power circuit. Typically, upon failure detection, the power electronics will shutdown, either until manually reset, or until conditions allow it to restart (depending upon the design).

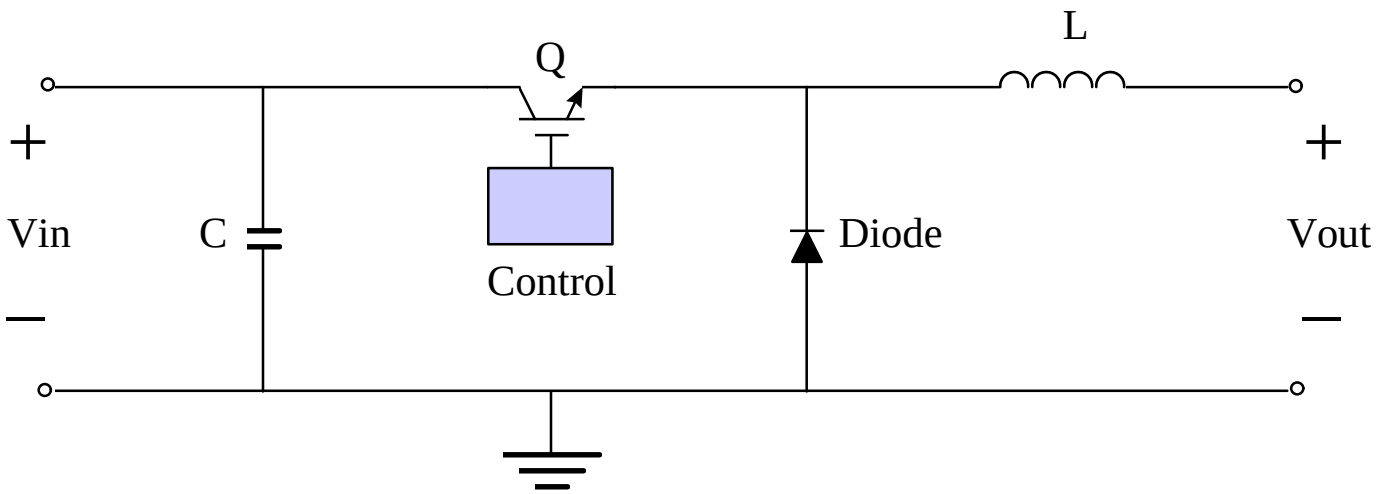


Figure 3.1: Buck Converter Topology

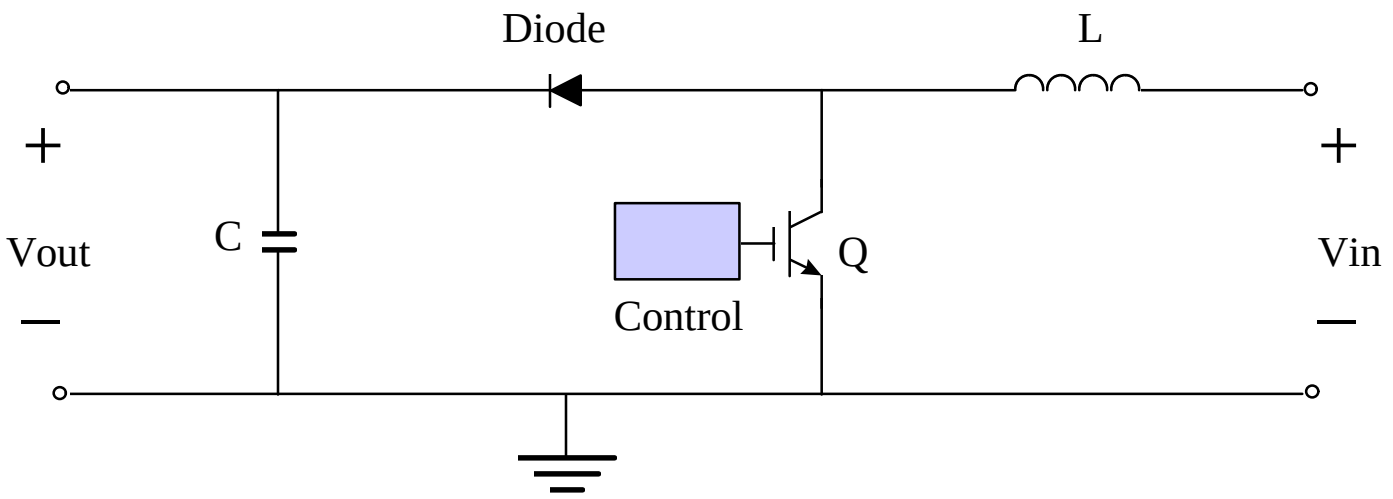


Figure 3.2: Boost Converter Topology

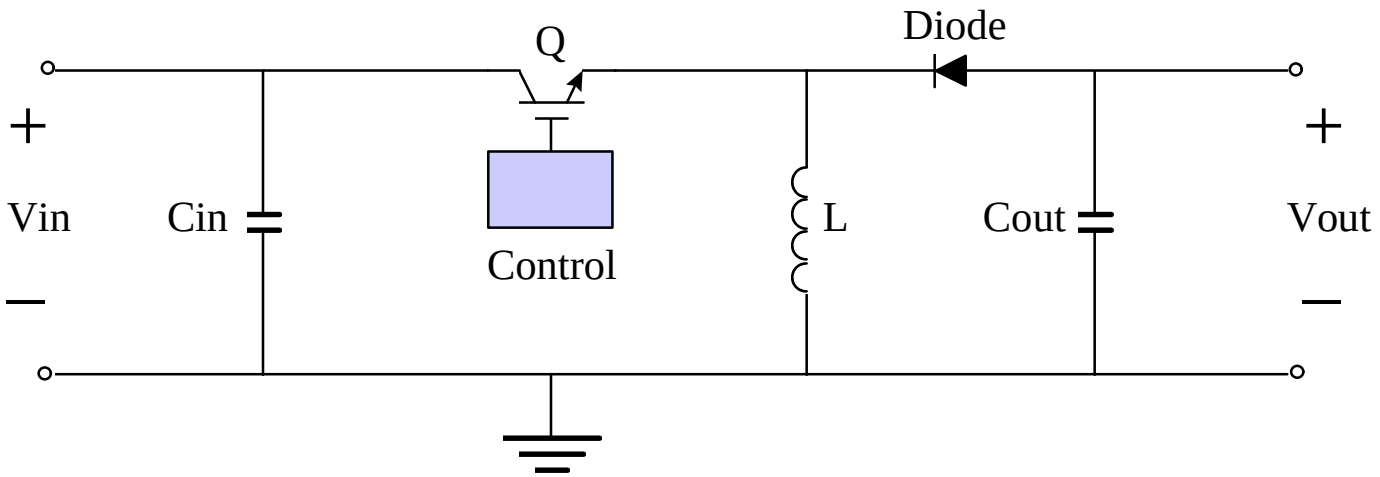


Figure 3.3: Buck/Boost Converter Topology

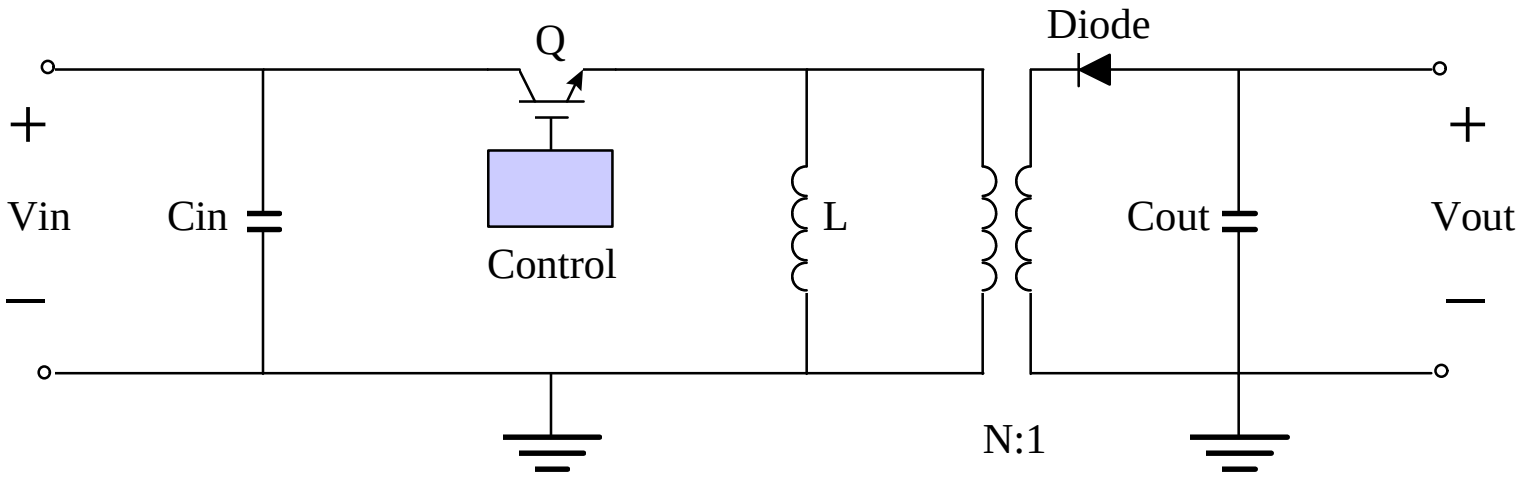


Figure 3.4: Flyback Topology

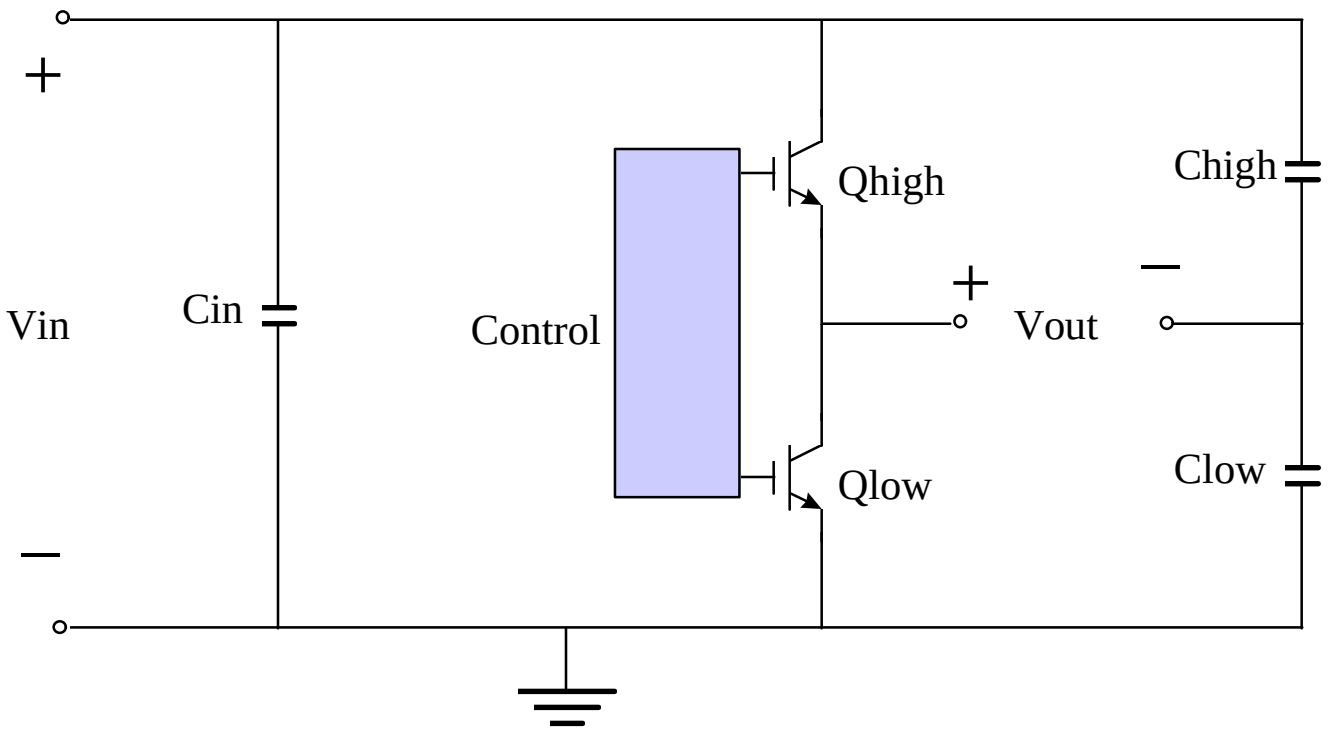


Figure 3.5: Half-Bridge Topology

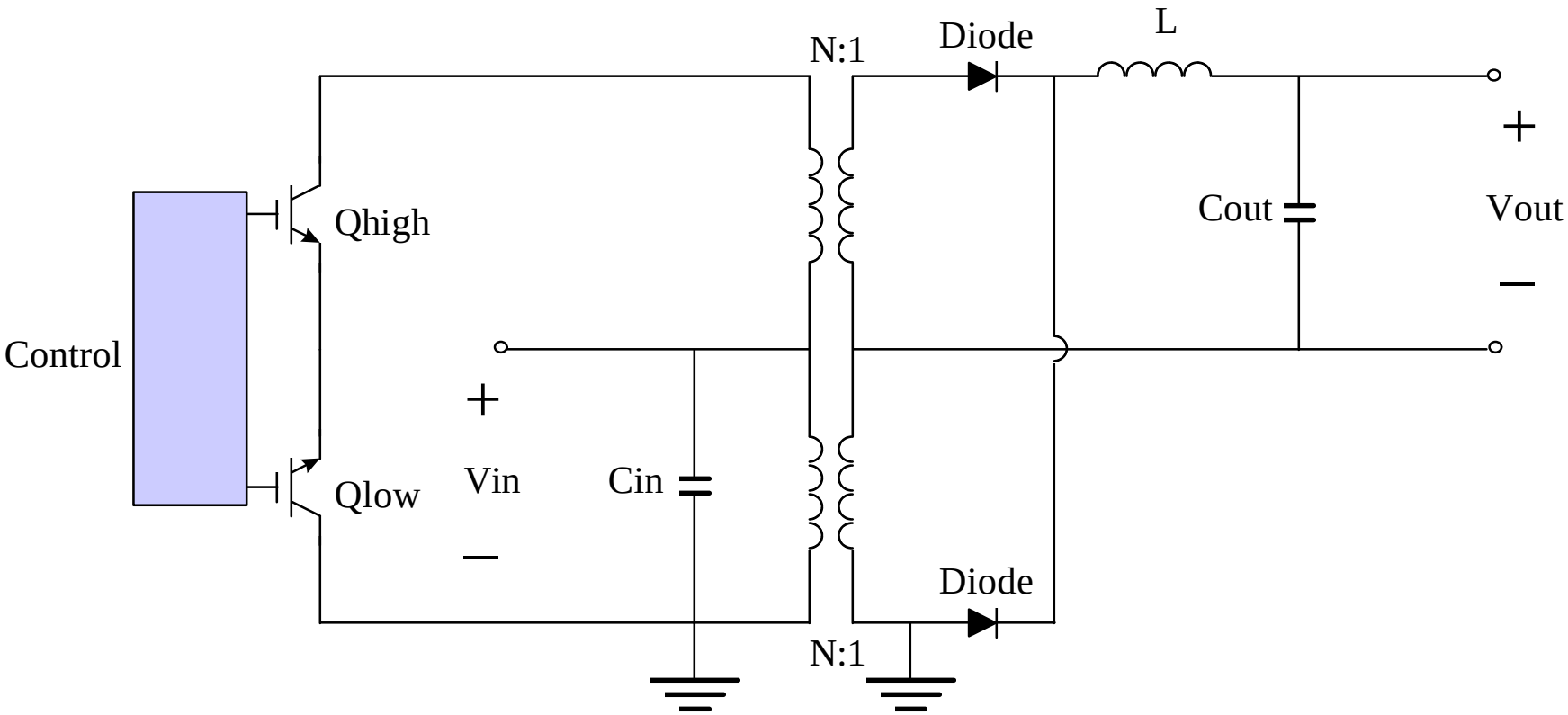


Figure 3.6: Push-Pull Converter Topology

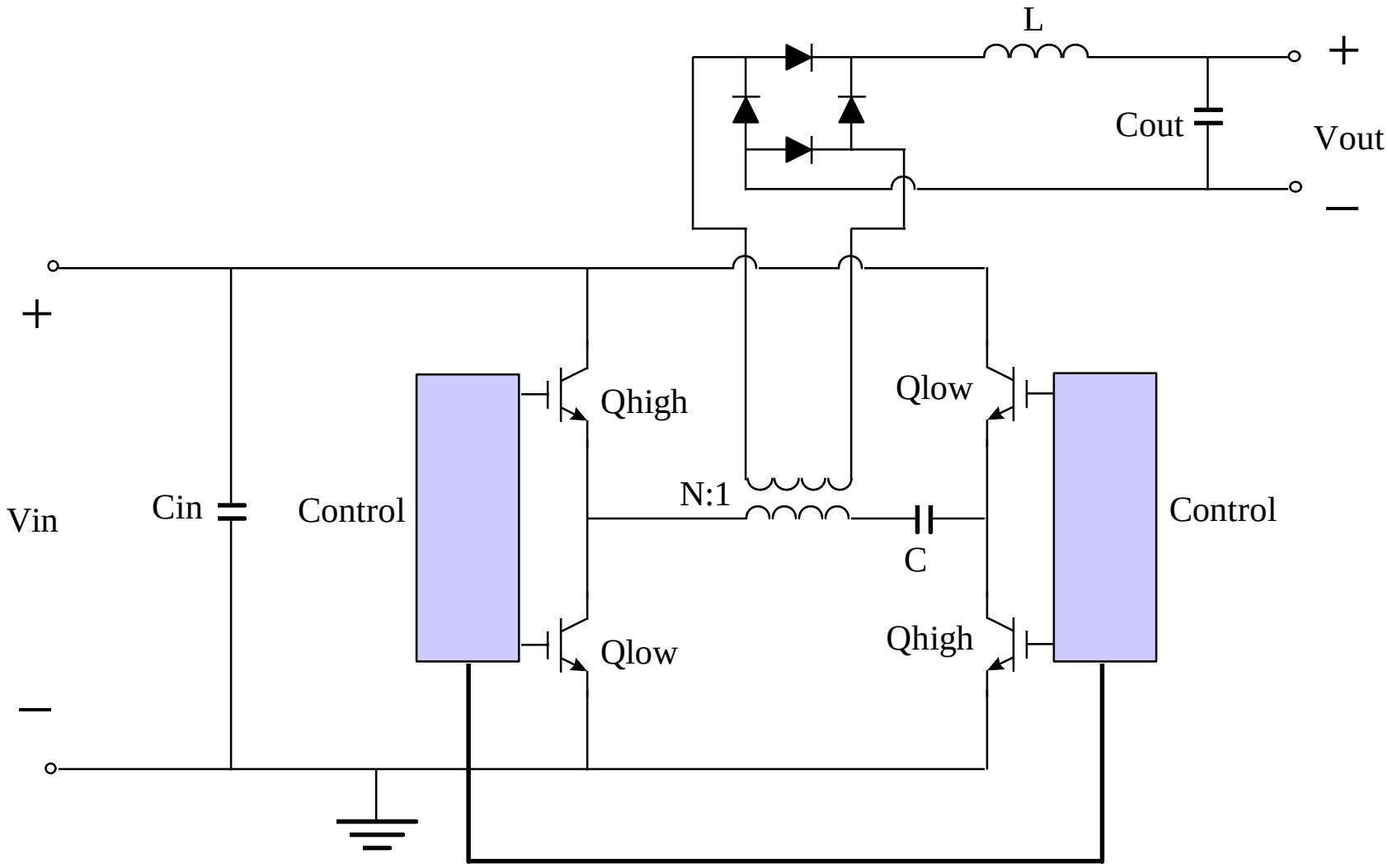


Figure 3.7: Full-Bridge Converter Topology

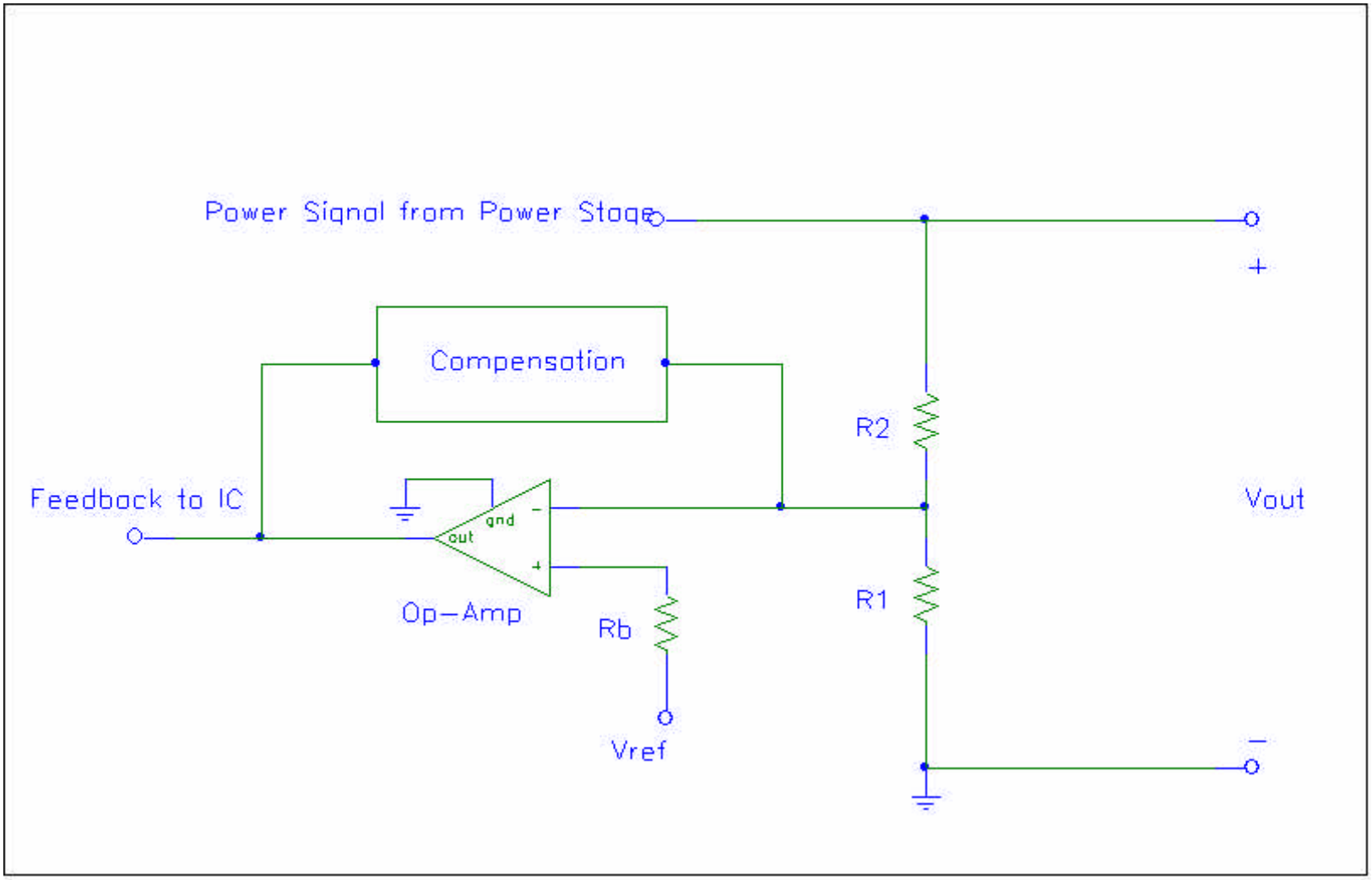


Figure 3.8: Voltage Controlled Feedback

CHAPTER 4.

HALF BRIDGE POWER CONVERTER, CONTROL, DRIVER, AND LOAD CIRCUITRY DESIGN

4.1 Half Bridge Power Converter Design

As stated, the first design choice was to decide what would be the application of the test power electronics module. The operation and power electronics circuit selected was a single phase half bridge power converter; it is a simple circuit in configuration and yet it has a large number of industry wide applications.

The second design choice was to decide upon which power transistors would be chosen to function in the power module. Insulated gate bipolar transistors were chosen for this task because of their quick switching speeds, high voltage and current operational capabilities, and low voltage rating dependency. After examining a wide variety of options and possible selections, the IXGH40N60A IGBT device (manufactured by IXYS, refer to Appendix A) was finally settled upon as the device of choice.[15] This selection was made upon a variety of attractive and required features, as well as upon supply availability. The IXGH40N60A is a bare die chip and capable of functioning under a

load of 600 volts and 75 amps, both of these being essential design criteria requirements for the high power and compact nature of the electronics module.

The switching of the devices in a half-bridge power converter is abrupt, and when an IGBT is turned off in this manner, trapped energy in the circuit stray inductance is dissipated in the transistor, causing a voltage overshoot (illustrated in Figure 4.1).[16]

These switching transients could prove detrimental to a device operating under high current and high voltage, and thus it is imperative to protect the power transistors. This was accomplished by employing three techniques. The first was to introduce a resistor to be placed before the device gate. This configuration protects the IGBT by limiting the turn-on speed of the device, thus allowing the energy time to dissipate from the device. The second technique used was to apply a snubber capacitor across the pair of devices in order to cancel stray inductances caused by the load and voltage source connections. The third technique was to utilize freewheeling diodes placed in parallel with the IGBT devices. This technique provides residual currents with a nondestructive path to ground.

The driver control chip is also susceptible to damage when high power transistors are being switched at high speeds.[17] The turn off of the transistor can produce a negative spike which filters back to the control. This negative spike could be dangerous to the control circuitry, and if large enough, could destroy it. This negative voltage spike can also be controlled by slowing down the switching speed of the device through the use of a gate resistor. Figure 4.2 illustrates a graph of the negative spike voltage amplitude versus the series gate resistance. It can be seen that with no gate resistance, a negative spike of

over 90 volts is returned to the control chip; the result would obviously be the destruction of the control chip. A gate resistance of 120 Ω (found experimentally to be the most effective value) was chosen according to this negative voltage spike criteria and what the control chip could handle. This is discussed in further detail in the **Control and Driver Circuitry Design** (4.2).

There are a number of other procedures that can be followed in order to minimize stray inductances and ensure reliable circuit operation. These procedures include: minimizing inductances through circuit layout considerations (such as keeping leads as short as possible or using copper strips instead of wires whenever possible); using decoupling capacitors as physically close as possible to the power stage; minimizing the area of high current loops; and using coupled twisted wires whenever possible.

4.2 Control and Driver Circuitry Design

The next step was to design a half bridge driver and control circuit. International Rectifier's IR21XX series ICs proved to be the most logical choice to fulfill the requirements of this application. The IR21XX series control chips range from simple single phase drivers to complex three phase signal feedback drivers, each chip easily upgradable to its more complicated successor. It was for the ease of increasing driver complexity and functionality that the IR21XX series chips were selected.[18] One of the basic chips is the IR2155 single phase driver with frequency control capability. The IR2155 is a self-oscillating, high voltage, high speed IGBT driver with high and low side referenced output channels, high pulse current buffer, internal deadtime (to eliminate

driver cross-conduction), and fixed 50% duty cycle. Figure 4.3 illustrates the IR2155 control chip and its supporting circuitry.

4.2.1 Programmable Oscillator Frequency

$$f = \frac{1}{1.4 \bullet (R_T + 150\Omega) \bullet C_T}$$

By picking C_T = 1nF (recommended by manufacturer), the required R_T can be solved for by choosing a desired frequency. In this case, it was desired that the frequency be variable, so a potentiometer was used instead of a fixed resistance value. The variable resistor has a range varying from approximately 500Ω to 3MΩ.

$$f = \frac{1}{1.4 \bullet (R_T + 150\Omega) \bullet C_T} \quad \Rightarrow \quad 250\ \text{Hz} \le f \le 10\ \text{MHz}$$

4.2.2 Dropping Resistor

The logic supply voltage of the IR2155 driver control chip is rated at approximately 15 V with 25 mA supply current. The power electronics module was desired to operate from a 300 volt power supply (the maximum rated power supply available), and so a proper dropping resistor had to be designed in order for the control circuit to be powered by the same power supply.[19]

$$V_{DC} - V_{CC} = I_{CC} \bullet R_1$$

$$I_{CC} = 5 \text{ mA} \qquad V_{DC} = 300 \text{ V} \qquad V_{CC} = 15 \text{ V}$$

$$\Rightarrow \quad R_1 = \frac{V_{DC} - V_{CC}}{I_{CC}} = \frac{300V - 15V}{5mA} \cong 57k\Omega$$

It also must be kept in mind that with such a large voltage drop through this resistor that it must be capable of handling the power dissipation.

$$P = I_{CC} \bullet (V_{DC} - V_{CC}) = 5mA \bullet 285V \cong 1.5 \text{ Watts}$$

4.2.3 Clamping Capacitors

$C_1 = C_2 = 1\mu F$

Both of these devices are simply common clamping capacitors.

4.2.4 Blocking Diode

D = Fast Recovery Rectifier Diode rated to 300 V

This diode blocks any current feedback that may attempt to run from the output stage back to the chip logic supply input.

4.3 Load Circuitry Design

One application of the power electronics module half bridge converter would be to convert DC power to AC in order to drive an AC motor. If only a single phase half bridge converter were used, such as was designed for the power module, then a single phase AC motor would be driven. As stated earlier, this single phase could easily be improved upon for a three phase design; however, single phase will be focused upon within this study.

Figure 4.4 displays an H-Bridge (full-bridge) configuration of switches which would be suitable for running a single phase motor with a single power supply. Figure

4.5 displays a half bridge converter that would switch a single phase motor using a ± power supply.

Both of these configurations have problems, though. In order to run the H-Bridge configuration, a pair of power modules couple with a more complicated driver control circuit would be required. This was undesirable, as stated, because the overall electrical design was to be kept as simple as possible. With the half bridge configuration, a ± power supply would be needed to run a single phase motor. The Microelectronics Laboratories were not equipped with such a power supply, so again, that was not a plausible solution.

It was decided that for test purposes, it was not necessary to run a single phase motor. The IGBT devices simply had to be stressed to their limits in order to insure proper operation. Figure 4.6 illustrates a purely resistive load configured with the half bridge power converter that results in stressing both devices equally. This is a cost effective solution that remains simple to configure and cheap to implement, while at the same time performing all of the required tests.

The values of R_{L1} and R_{L2} had to be designed using multiple high power resistors already in stock in the Microelectronics Laboratories, and this design had to be configured to the high rated power supply.

Power Source	Load Resistors
V_{DC} = 300 V	$R_{Resistor}$ = 5 Ω
I_{DC} = 10 A	$P_{Resistor}$ = 300 Watts
$R_{L1} = R_{L2}$	

$$V_{DC} = I_{DC} \bullet R_{L1} \qquad \Rightarrow \qquad R_{L1} = \frac{V_{DC}}{I_{DC}} = 30\ \Omega = R_{L2}$$

Connecting six 5 Ω resistors in series will result in the desired load resistances of 30 Ω.

$$R_{L1} = R_{L2} = 6 \bullet 5\Omega = 30\ \Omega$$

The average power dissipated over each load resistance is

$$P_{RL1} = P_{RL2} = \frac{1}{2} \bullet V_{DC} \bullet I_{DC} = \frac{1}{2} \bullet 300V \bullet 10A = 1.5\ \text{kW}$$

The total power dissipated by the total load is then

$$P_{Total} = P_{RL1} + P_{RL2} = 1.5\text{kW} + 1.5\text{kW} = 3.0\ \text{kW}$$

And the required dissipation per resistor is

$$P_{Each} = \frac{P_{Total}}{12} = \frac{3.0kW}{12} = 250\ W \qquad \text{(which is within the 300 watt limit)}$$

4.4 Electrical Testbed for Power Electronics Module

The combination of the driver and control circuitry, the power module, and the load circuitry constitutes the power module electrical testbed. The testbed circuit layout is illustrated in Figure 4.7, the testbed physical setup is illustrated in Figure 4.8, and the driver control PCB layout is illustrated in Figure 4.9.

4.5 Testing of the Electrical Testbed

The electrical testbed configuration of Figure 4.10 was setup using a discrete half bridge power converter with standard low cost 730 Power MOSFETs bolted to a heat sink (refer to Appendix A), and 680kΩ load resistors operating at high voltage and low current (and thus low power). The purpose here was to ensure proper operation of the power module testbed. The testbed tests the proper switching of the control and driver circuitry. Since this was an initial phase, MOSFETs were used instead of IGBTs due to their much lower cost.

The discrete 730 Power MOSFETs were then replaced by the more costly International Rectifier IRGBC30FD2 (refer to Appendix A) IGBT devices (discrete devices of similar operation and characteristic to the bare die devices to be used in the

power module). This setup was then tested with the low power load in order to ensure proper operation of the electrical testbed.

The load was then reconfigured to the high power design and the test was run again, ensuring proper circuit functionality of the electrical testbed at 300 V and 10 A. With the testbed successfully tested, the discrete version of the half bridge converter was removed, and the power module simply needed to be plugged into its place for module testing to begin.

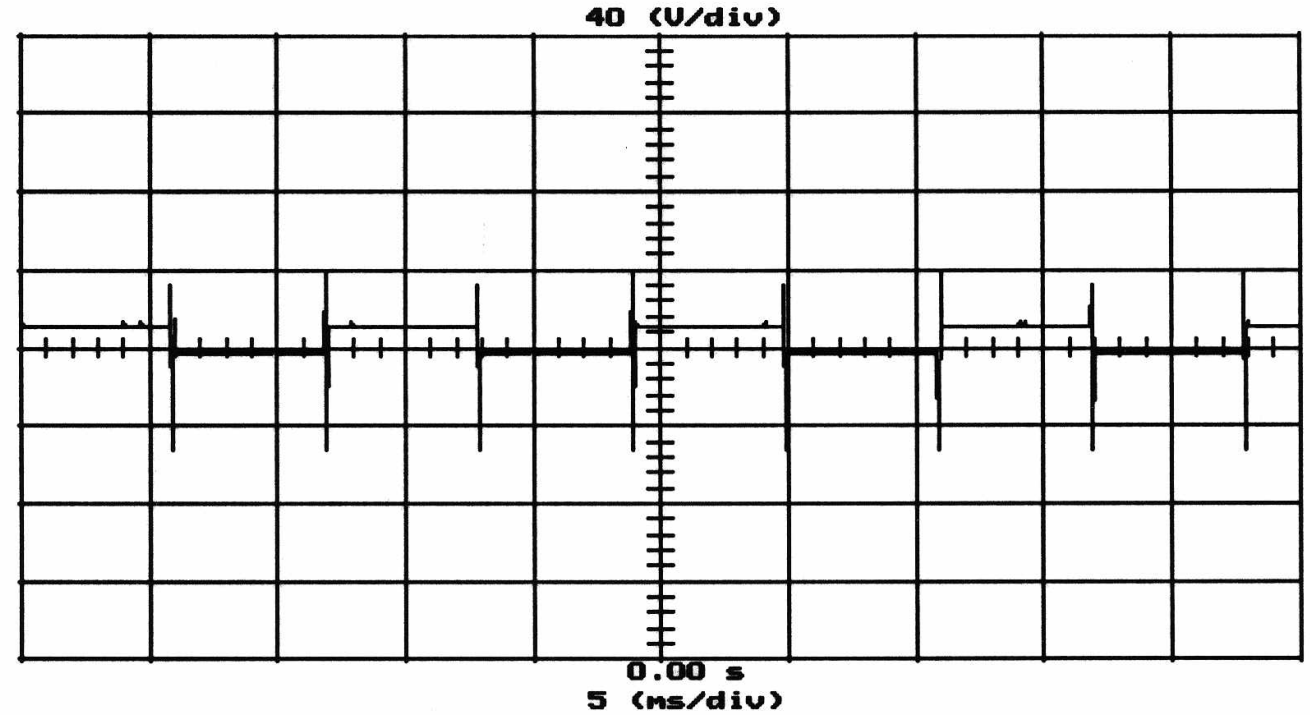


Figure 4.1: Experimentally Measured Voltage Overshoot and Negative Return Spikes

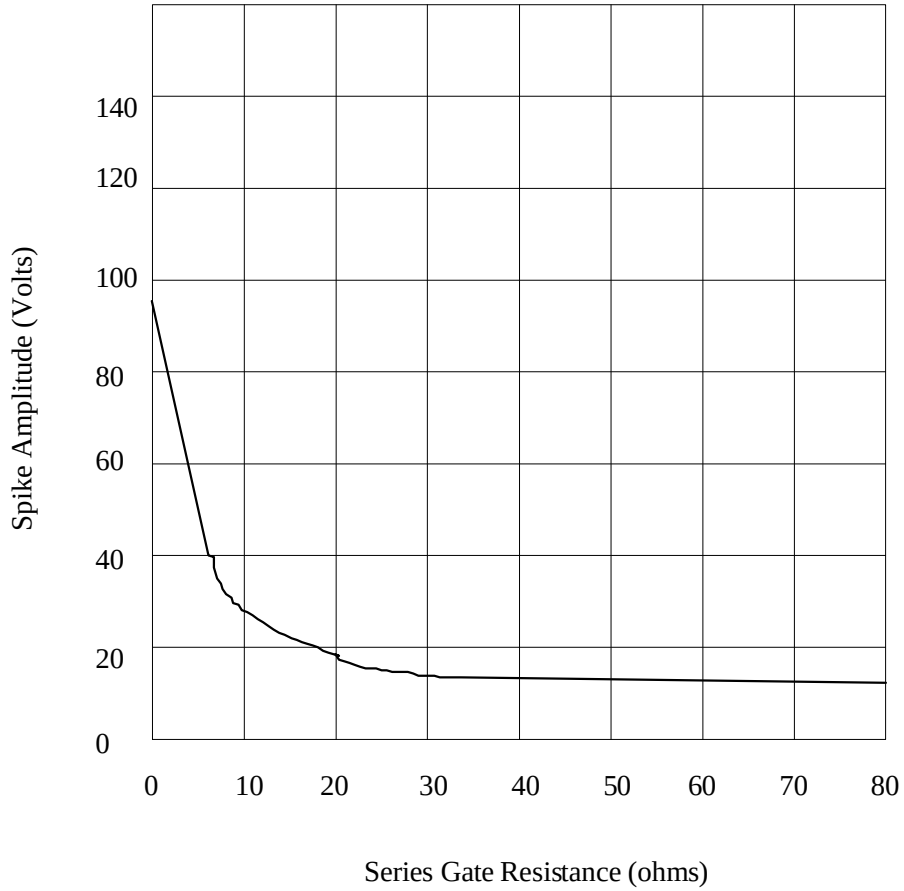


Figure 4.2: Series Gate Resistance vs. Negative Voltage Spike Amplitude at Turn Off

V_{CC} = Logic Supply Voltage

V_B = High Side Floating Supply Voltage

R_T = Oscillator Timing Resistor Input

HO = High Side Gate Drive Output

C_T = Oscillator Timing Capacitor Input

RL = High Side Floating Supply Return

COM = Low Side Return

LO = High Side Gate Drive Output

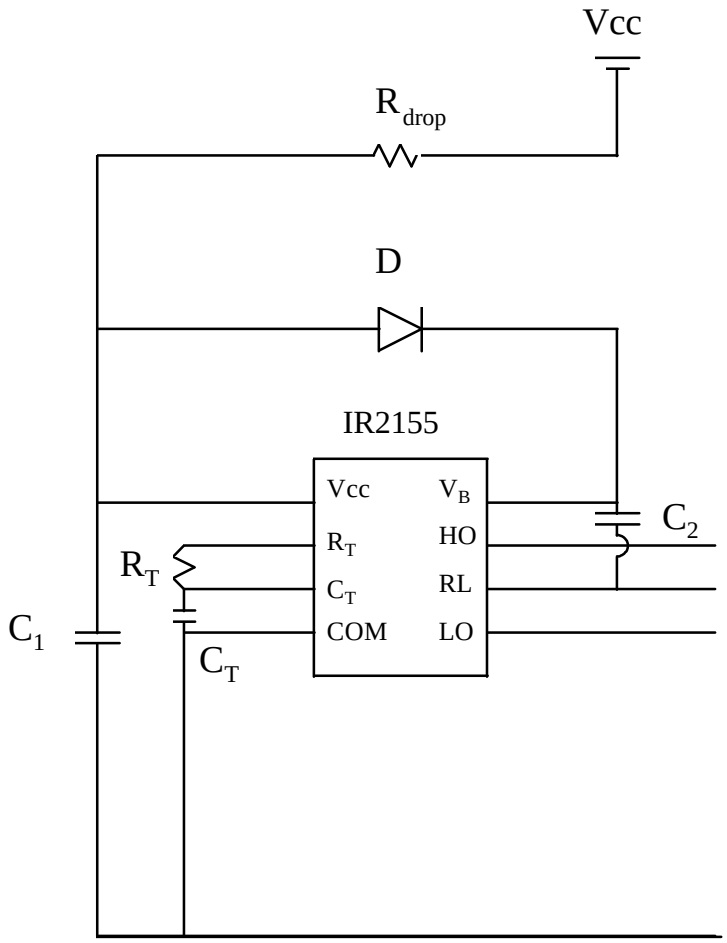


Figure 4.3: Driver and Control Circuitry

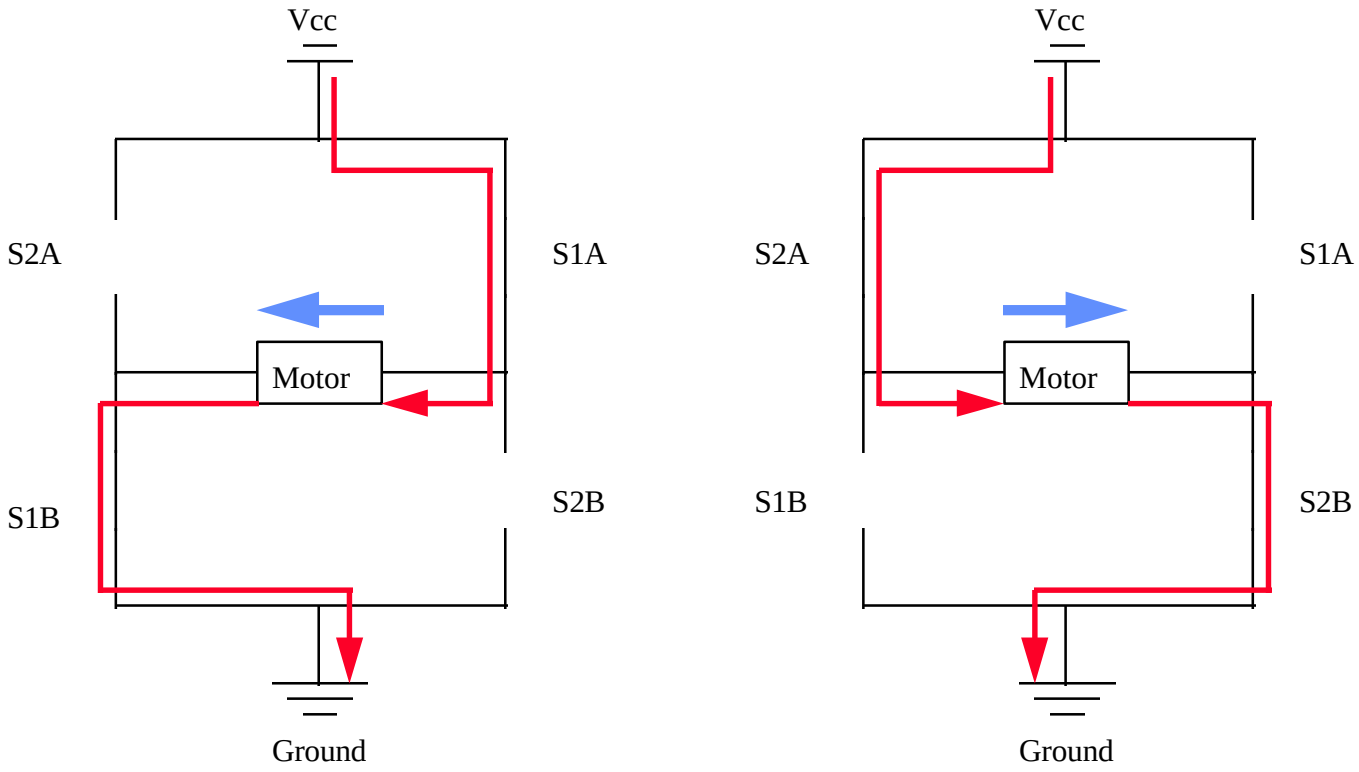


Figure 4.4: H-Bridge Configuration

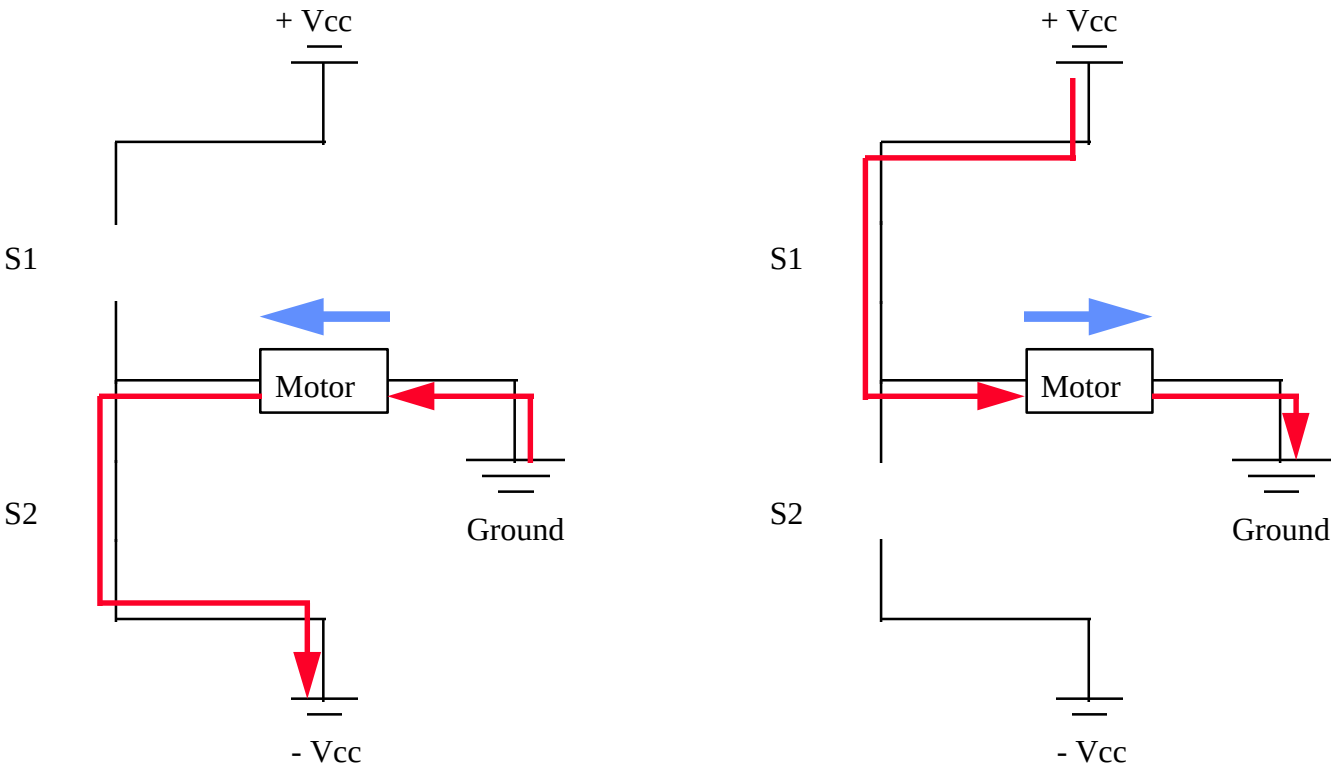


Figure 4.5: Half Bridge Power Converter Configuration

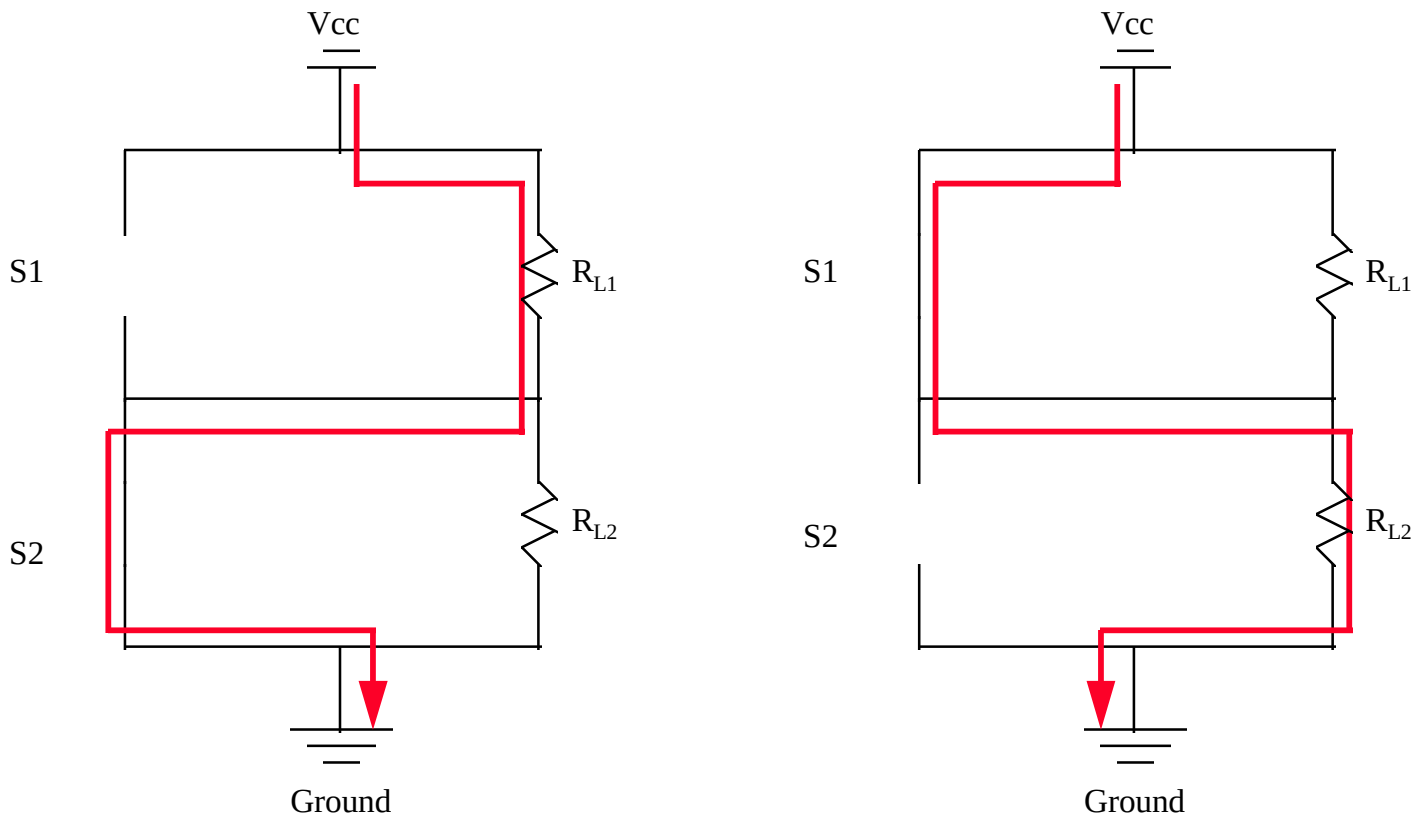


Figure 4.6: Resistive Test Load Configuration

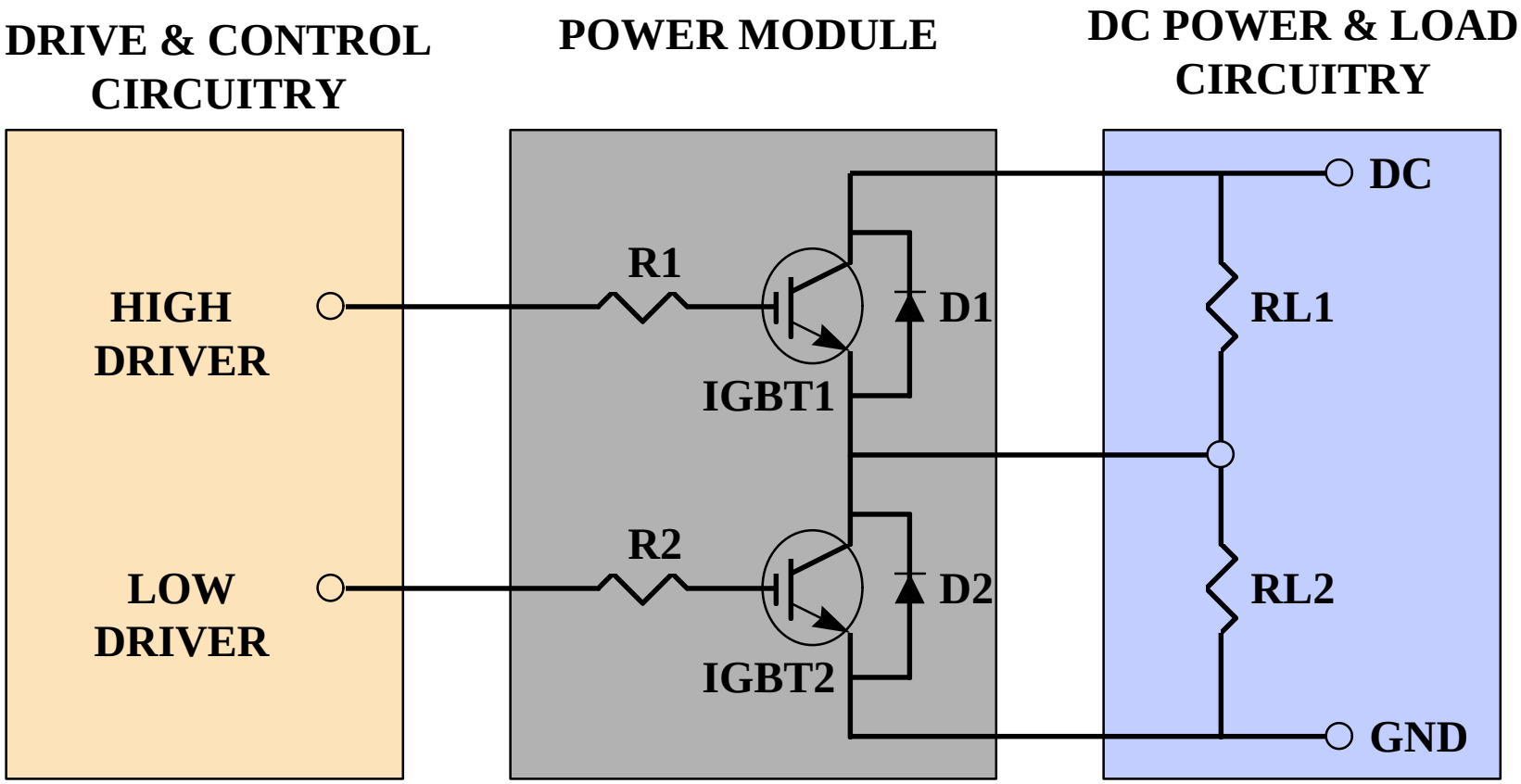


Figure 4.7: Testbed Circuit Layout

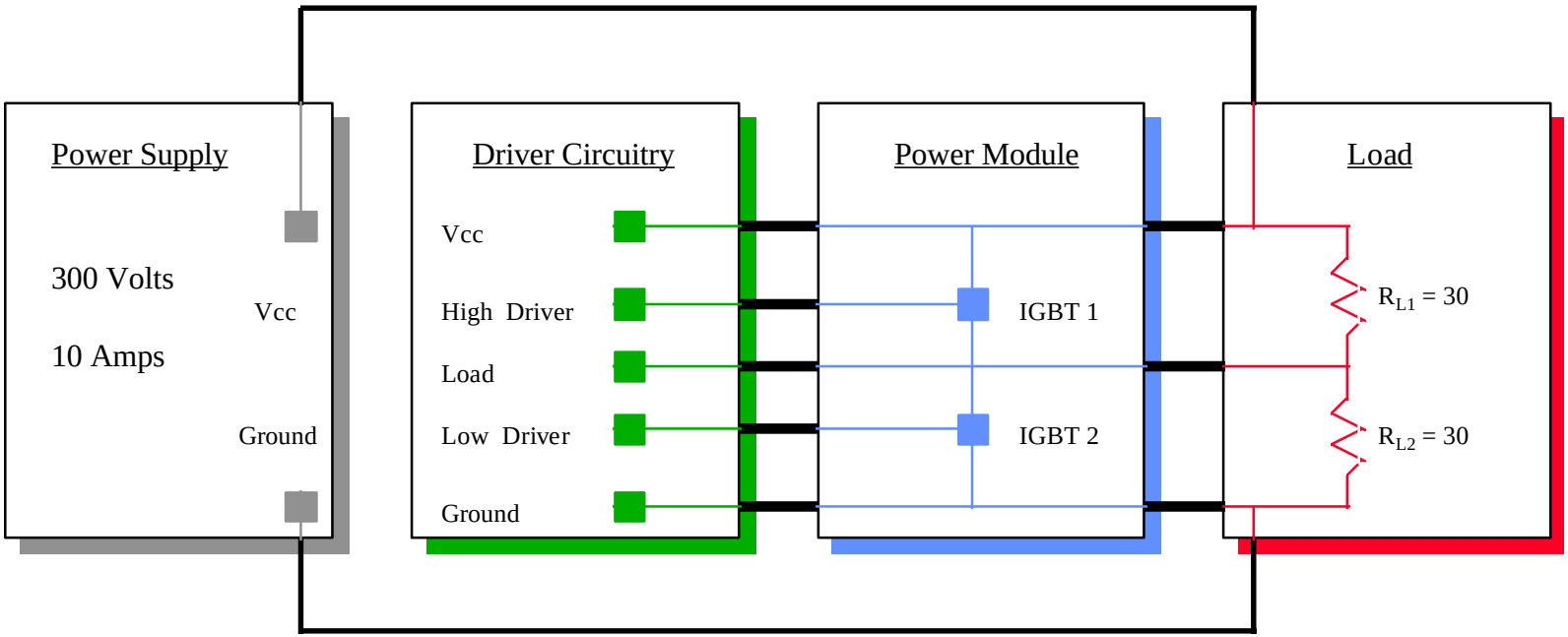


Figure 4.8: Testbed Physical Setup

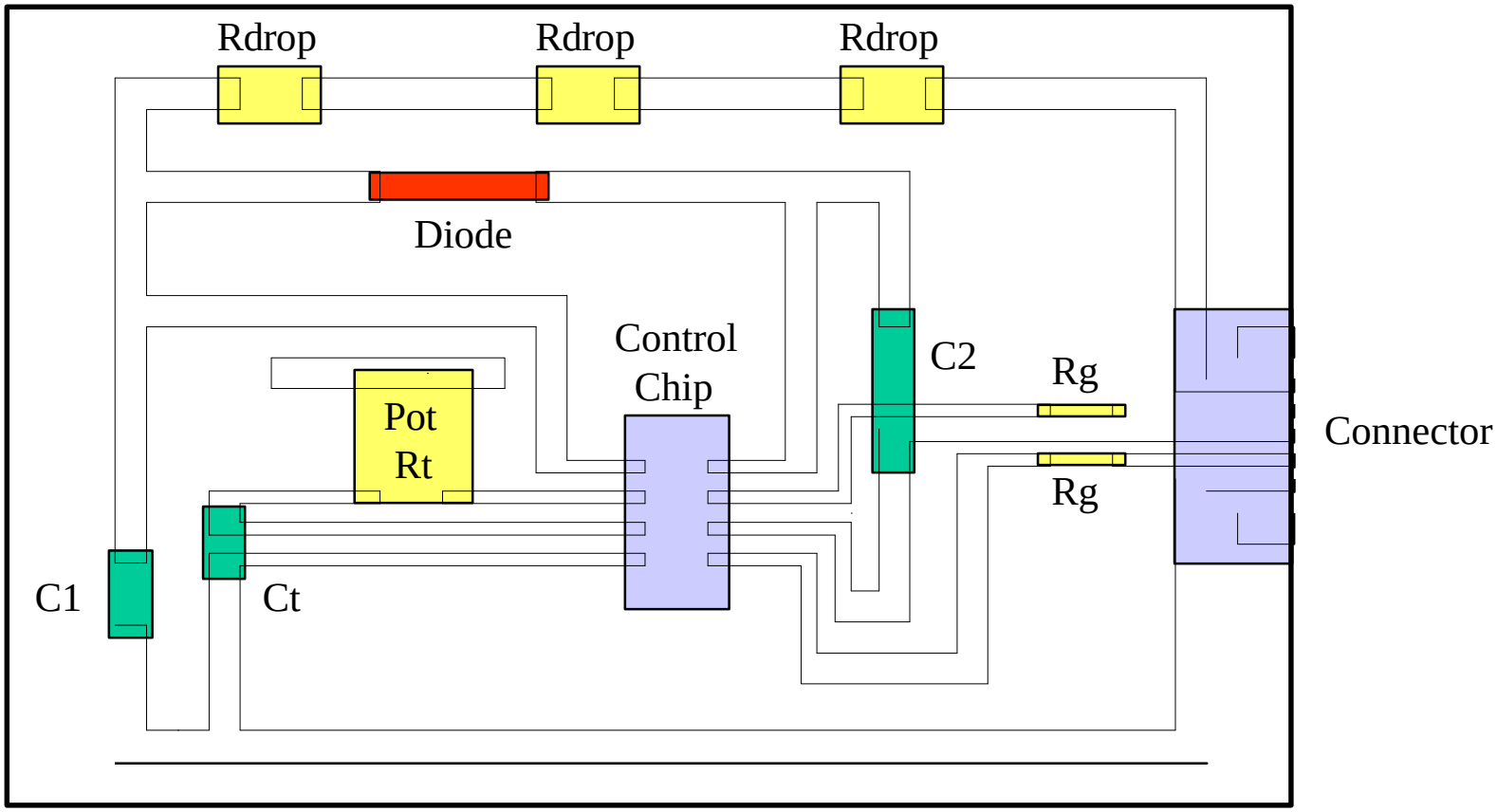


Figure 4.9: Driver Control PCB Layout (Through-hole)

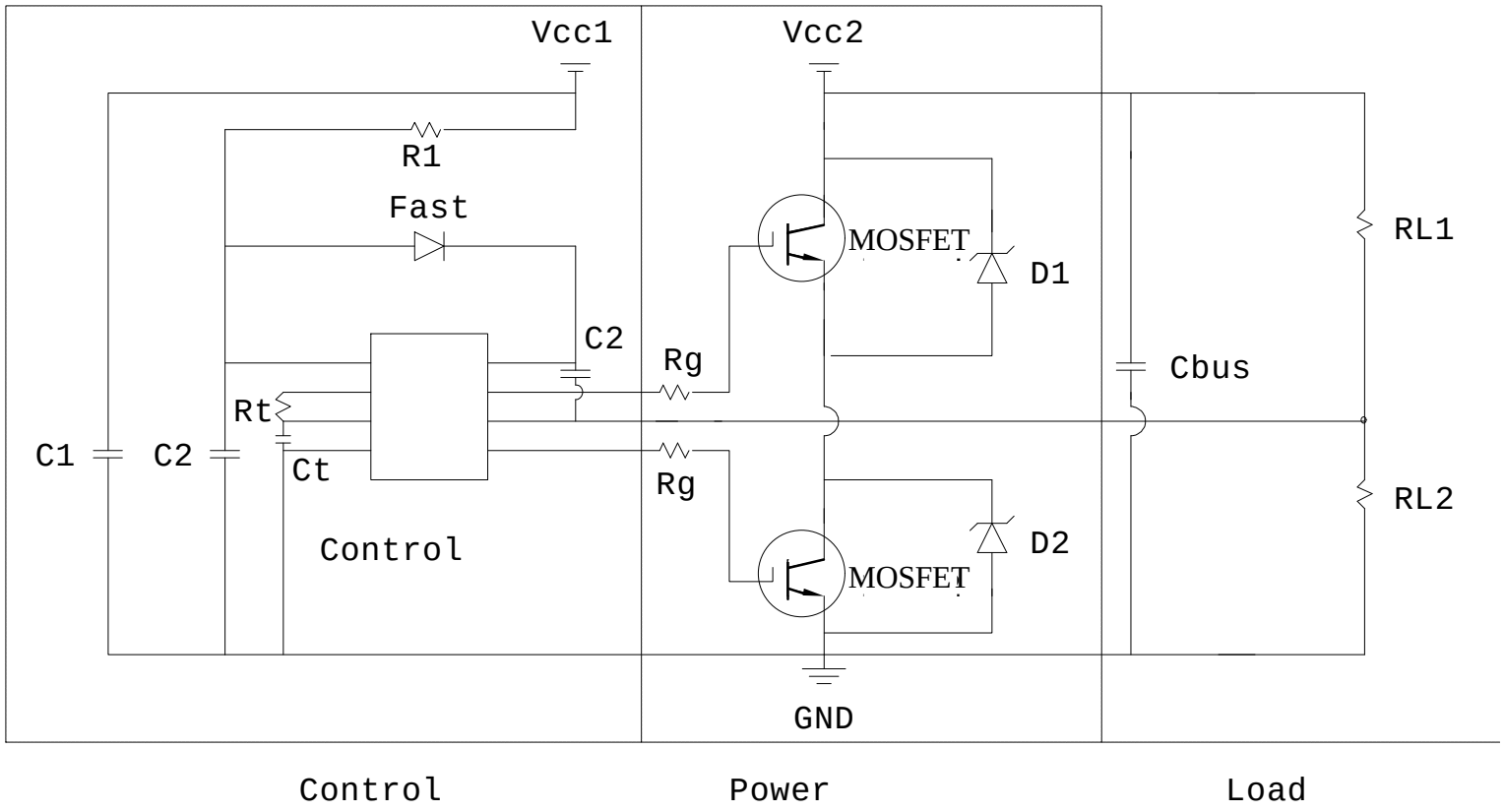


Figure 4.10: Testing of the Electrical Testbed

CHAPTER 5.

DESIGN AND FABRICATION

OF POWER ELECTRONICS MODULES

5.1 Single Metallization Layer Wirebond Module Design

The next step was to design, fabricate, and test a basic wirebond module (to serve as a reference module) in which all of the necessary power devices and supporting circuitry were placed on a single surface metallization layer. Constructing this wirebond module confirmed various fabrication ideas for a multilayer construction, as well as provided the researcher with an excellent starting position for improved module performance.[20] This wirebond module proved the bare die soldering techniques to be feasible options, confirmed the reliability of an AlN direct bond copper substrate to be used as the base metallization layer for the power devices, and confirmed that all of the half bridge converter circuitry could be mounted on a single module. This initial wirebond module cross-sectional layout is illustrated in Figure 5.1, the circuit metallization layout is illustrated in Figure 5.2, and the IXGH40N60A bare die IGBT and C-DWEP 55-06A bare die Diode layouts are illustrated in Figure 5.3.

5.2 Single Layer Wirebond Module Fabrication

The wirebond module consists of an AlN substrate bonded directly on either side to copper (DBC).[21] The copper is nickel plated through an electrolysis nickel plating procedure (to enhance bondability through removal of oxidation), and then the desired circuit paths are etched from the metallization. The surface mounted components and bare die devices are then reflow soldered to the module. The bare die wirebonds are performed and then the entire module is bonded to a heat sink.

The DBC is approximately a 20 mil thick AlN layer with a 12 mil copper layer on either side. The nickel plating setup is illustrated in Figure 5.4. The current is set to approximately 0.75 amps with a voltage of approximately 1.5 volts. The voltage may vary, depending upon the distance of the anode and cathode, but it was found that a current of 0.75 amps produced the best plating results. The nickel solution should have a pH=5, and the solution should be heated to a temperature of approximately 50 °C. The AlN substrate is connected as the cathode and a nickel plate is connected as the anode. Each side of the DBC should be plated for approximately fifteen minutes for an even plating of approximately one mil.[22]

A mask is generated using the metallization layout of Figure 5.2, dry photoresist is applied to the DBC, and then the circuit is etched using a Ferric Chloride etchant solution. The components are then soldered down utilizing the Sacomma open air belt drive reflow unit. Indalloy #209 ribbon solder (refer to Appendix A for solder properties) is used to bond the devices to the metallization. The 209 is dipped in #5RA flux, the excess flux is wiped free, and then the solder is placed onto the circuit trace. This process

is repeated for each component, and then each of those components is placed down in their respective positions (refer to Appendix A for temperature profile).

The source and gate of each IGBT, and the anode of each diode is wire bonded to the proper metallization traces of the module using 15 mil diameter aluminum wire. The heat spreader is then reflow soldered to the module using Indalloy ribbon solder #1E, flux #5R (refer to Appendix A for temperature profile).

5.3 Multi Metallization Layer Power Module Design

A number of various techniques and methods were explored and tested in the development of the multilayer power electronics building module, providing the researcher with valuable experience and knowledge. Procedures such as thin film deposition through sputtering, metal plating through electrolysis (nickel and gold plating), Ferric Chloride etching of direct bond copper, substrate and polymer cutting through laser trimming, high temperature / high pressure polymer to copper plate bonding, and reflow solder and wirebond techniques to surface mounted and bare die components were explored.[23]

In this design, a direct bond copper AlN substrate makes up the bottom metallization layer, and copper bonded to polymer (with cut out vias) makes up the top metallization layer. AlN was chosen because of its inherent thermal advantages (which are discussed in Chapter 6), and polymers were chosen for the multilayer control construction due to their low cost and processability. The two layers are then bonded together, the devices placed into the recessed areas or vias and soldered down, and

molytabs soldered to the top of the devices. Copper metallization straps are then soldered to the molytabs and connected to the top copper metallization layer, and then the surface mount devices are soldered down to complete the circuit. The final step is to bond the entire module to an MMC or copper heat spreader. The final multilayer power electronics module cross-sectional layout is illustrated in Figure 5.5.

There are a number of purposes for creating a multilayer power module. The first purpose is to eliminate wirebonds. By replacing the wirebonds with a molytab, it is expected that the parasitics of the module will be greatly decreased, and thus performance will improve.[24] The second purpose for using the multilayer concept is to increase metallization space. The power devices are placed on the bottom metallization layer and the control devices are placed on the surface metallization layer. This design increases the amount of metallization that is connected to the power devices and thus increases thermal dissipation and module efficiency.[25, 26, 27] The third reason for a multilayer approach is compactness and removal of board to board noise. In standard power module constructions, the control circuitry and power circuitry exist on separate boards. This is because the noise, power, and thermal requirements for the two stages are greatly differing, thus requiring the boards to have different properties. By combining the two stages into a single module which is multilayer, the power stage retains its high power substrate (AlN DBC) with thick copper traces, while the control stage retains its thin lines and high density.

The designed power electronic module circuit layout is illustrated in Figure 5.6 and a conceptual three dimensional multilayer power module is illustrated in Figure 5.7.

5.4 Multi Metallization Layer Power Module Fabrication

The multilayer power module fabrication is similar to that of the wirebond module, although several new processes had to be explored.

The first processing steps are the same as in the wirebond module. The bottom metallization layer is a DBC AlN substrate, the top metallization is a 5 mil thick layer of copper cladded polymer, and the metal straps are 5 mil thick pieces of copper. All of these layers are nickel plated through the same process as explained in the previous section.

The first problem that had to be overcome was the bonding of the top metallization layer to the bottom metallization layer, while at the same time, preserving the insulation characteristics. The solution to this is the bonding of multiple layers of polymer to the sheet of nickel plated copper under high temperature and high pressure. Vias in the polymer and adhesive first have to be trimmed out (illustrated in Figure 5.6) using the laser trimmer. The polymer, adhesive, and top metallization layer are then pressed under a temperature of 370-390 °F and a pressure of 200 psi for approximately 1/2 hour. The press is then allowed to cool for four to six hours before the layer is removed.

The top metallization layer (now bonded with the polymer), the bottom metallization layer, and the metal straps are etched through the processes described in the previous section. The top and bottom layers are then bonded together under high temperature and high pressure. The power transistor and diode devices are then placed

into the recessed vias and soldered down using the #209 solder ribbon and 5RA flux (see Appendix A for temperature settings). The molytabs are soldered to the top of the devices using the same process, except they are run through the Infrared Reflow Solder Unit (see Appendix A for temperature settings). The surface devices are then soldered down using #104 solder paste and the IR unit (see Appendix A for temperature settings). The last step is to solder down the metal straps and the heat spreader using #1E solder ribbon (see Appendix A for temperature settings).

5.5 Module Testing

Once the modules are fabricated, they must be tested. The first step in testing is to make sure the devices are not shorted. This is a simple matter to check by using a multimeter and checking for shorts between the gate, emitter, and collector. Connections throughout the entire module are then checked in order to ensure metallization trace continuation through vias and strap connections. After this is completed, the module is plugged into the electronic testbed for operational verification.

Figure 5.8 illustrates test waveforms for the wirebond module operating under a three kilowatt load, verifying the full functionality of the power modules. The DC input power was approximately 214V. The gate drive was a 15V pulse waveform opperating at approximately 60Hz with a pulse width of about 50%. The low side load output is therefore a pulse waveform with a maximum magnitude of approximately 214V at 60Hz cycle and 50% duty cycle. One key factor for proper operation of the power devices is the inclusion of deadtime so that both IGBTs are not on at the same time. Figure 5.9 illustrates the deadtime waveform measurements of the power module operating under 3kW load conditions. The deadtime measured to be approximately 1μs.

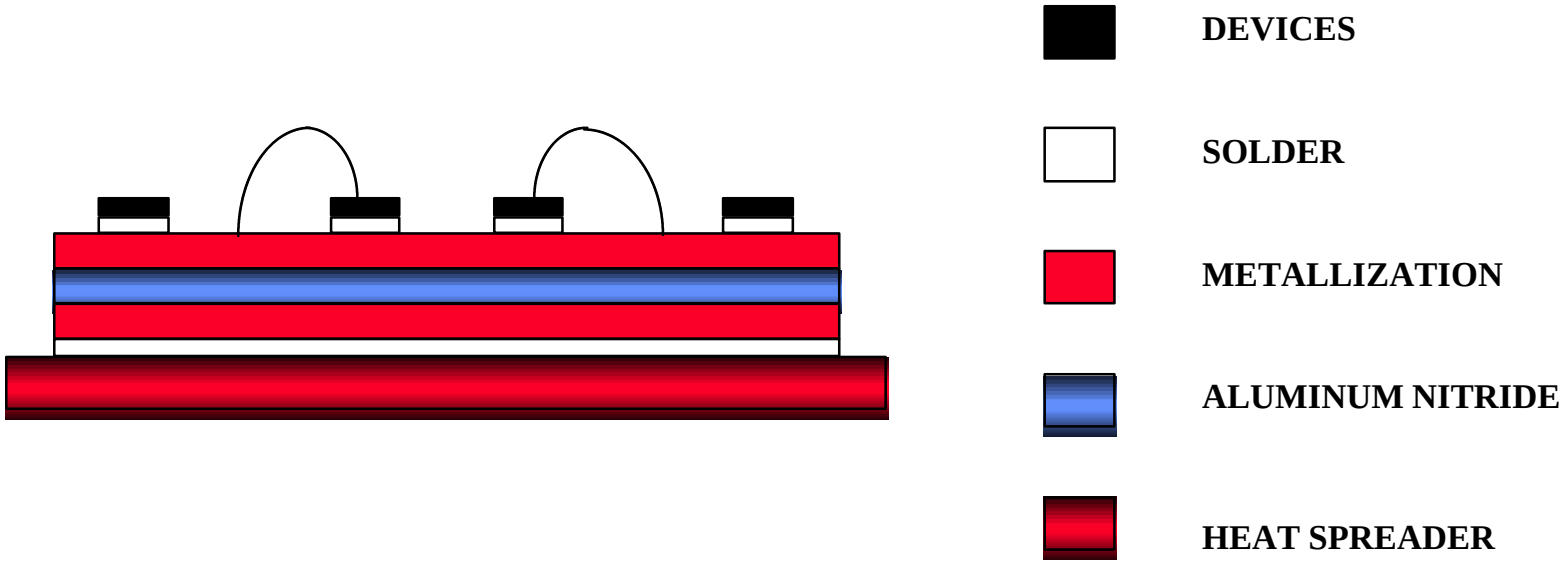


Figure 5.1: Wirebond Module Cross-sectional Layout

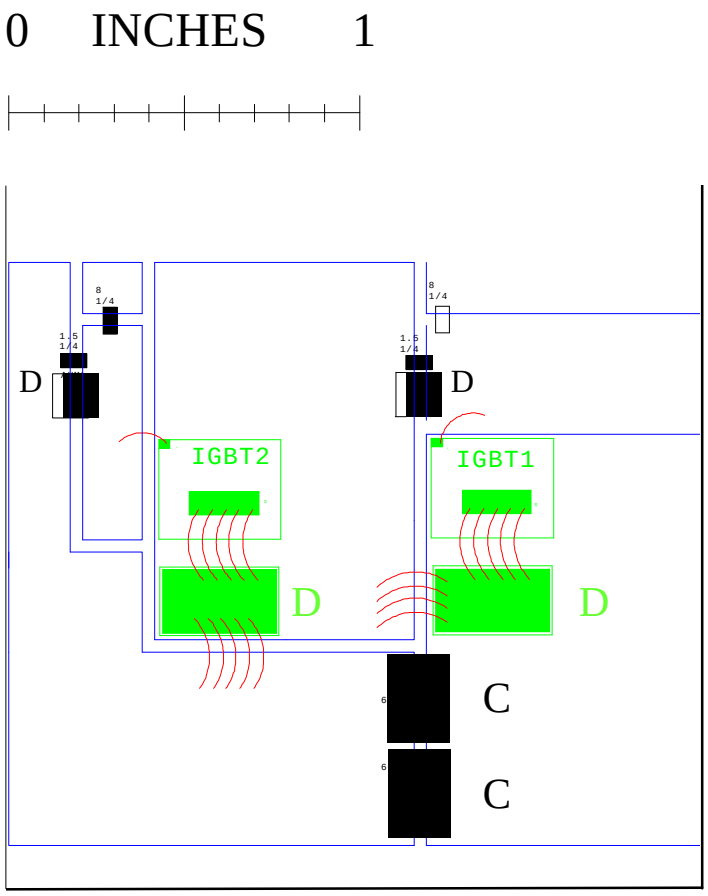


Figure 5.2: Wirebond Module Circuit Layout

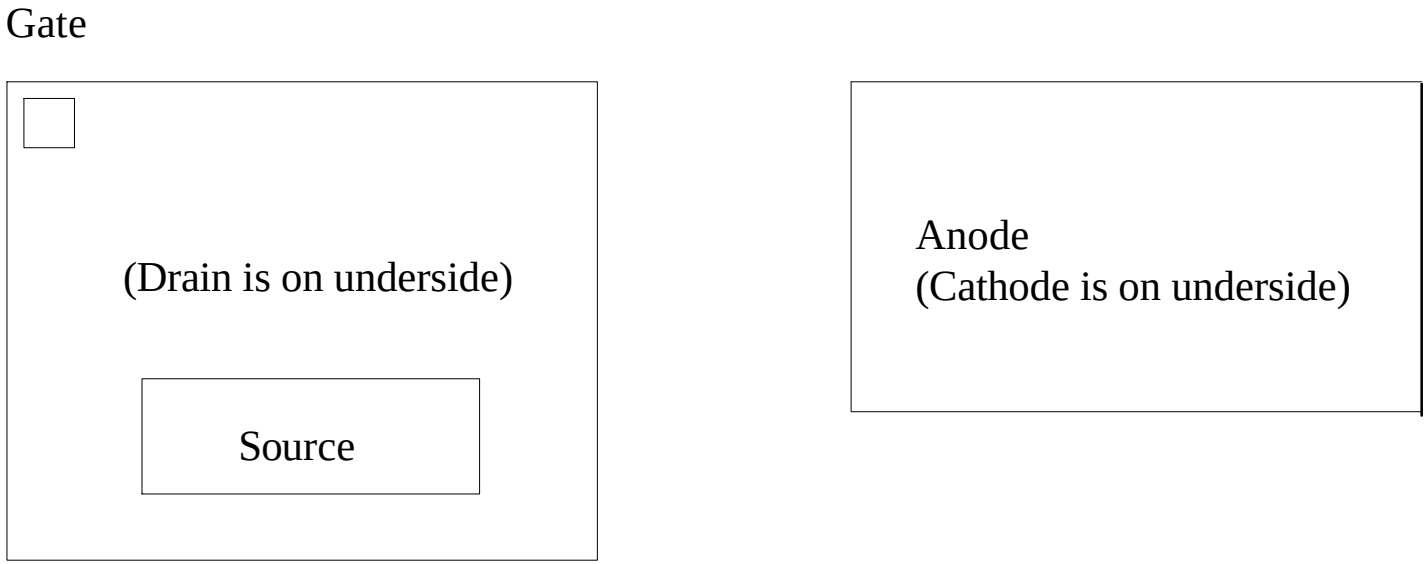


Figure 5.3: Bare Die Layouts

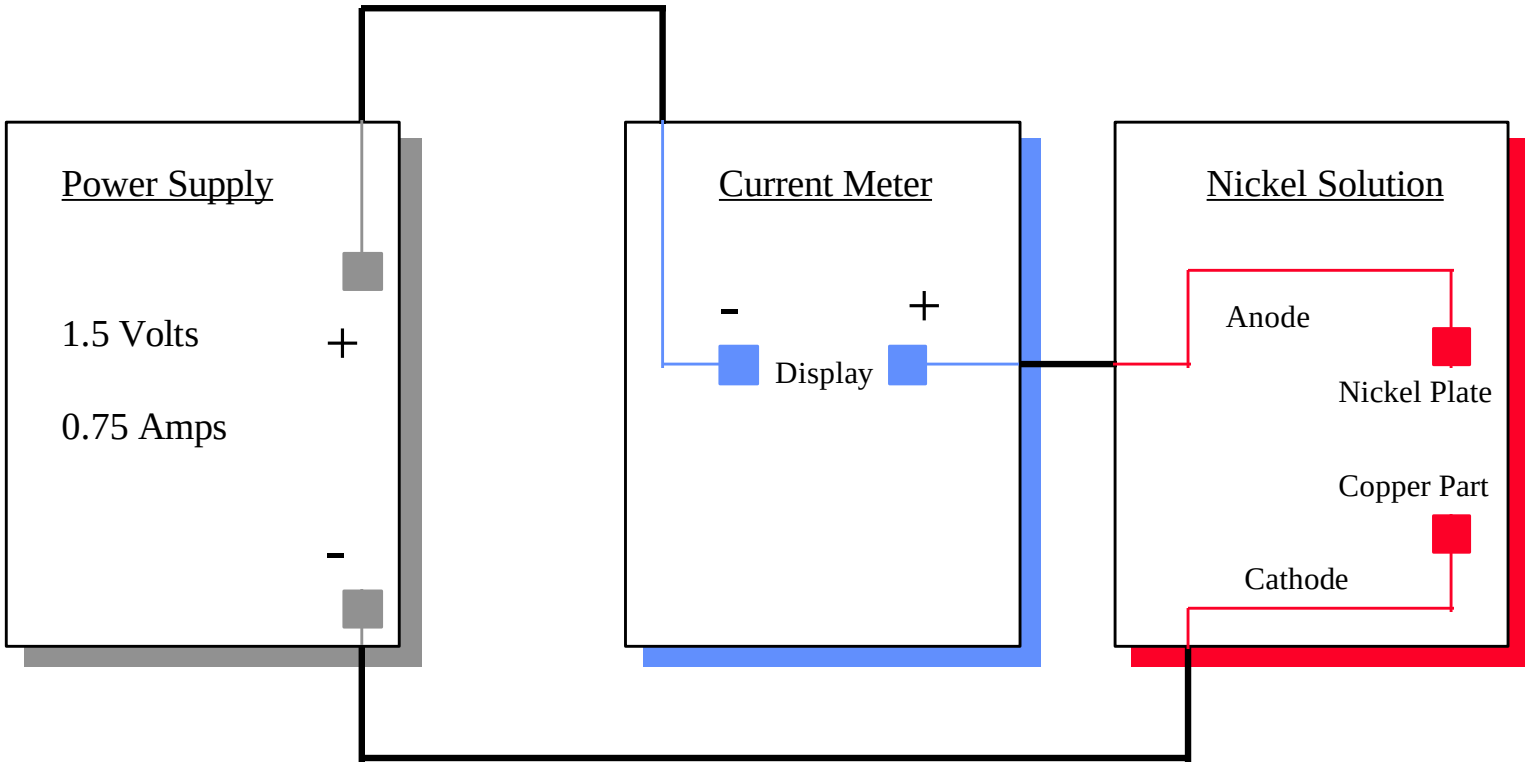


Figure 5.4: Electrolytic Nickel Plating Setup

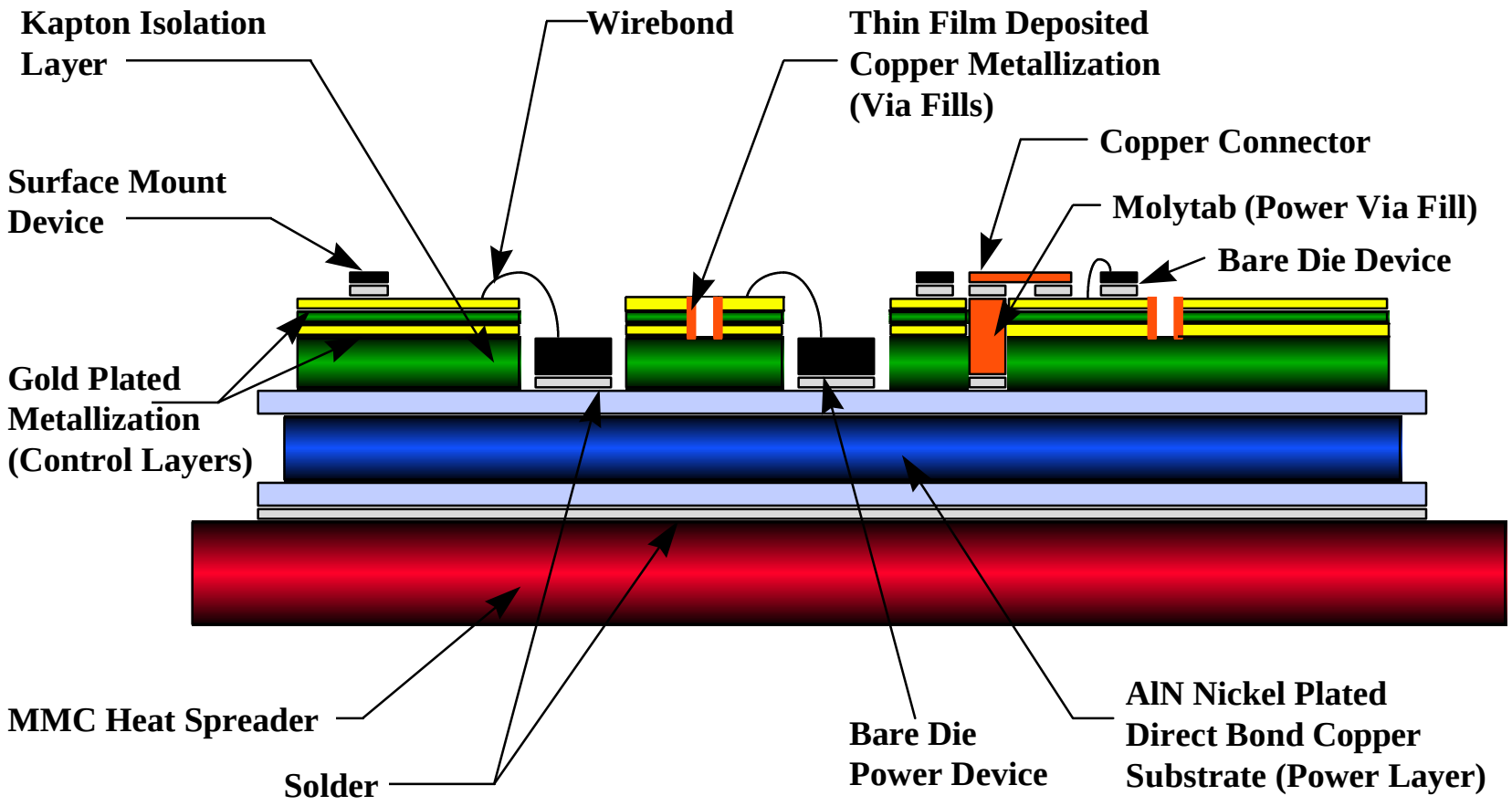
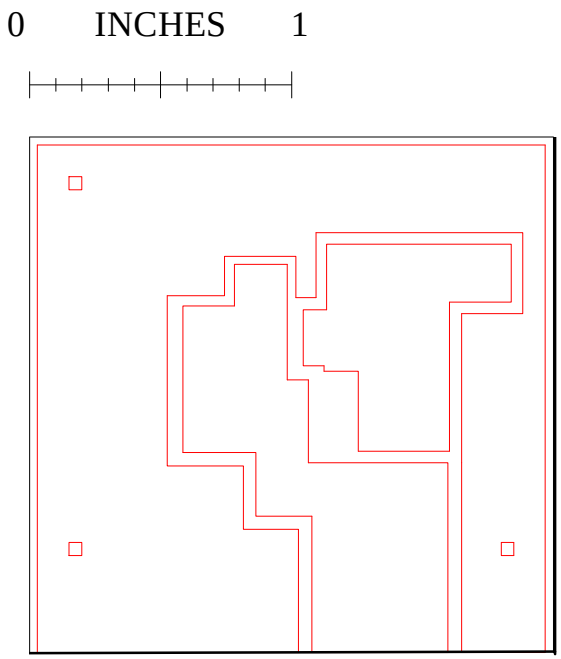
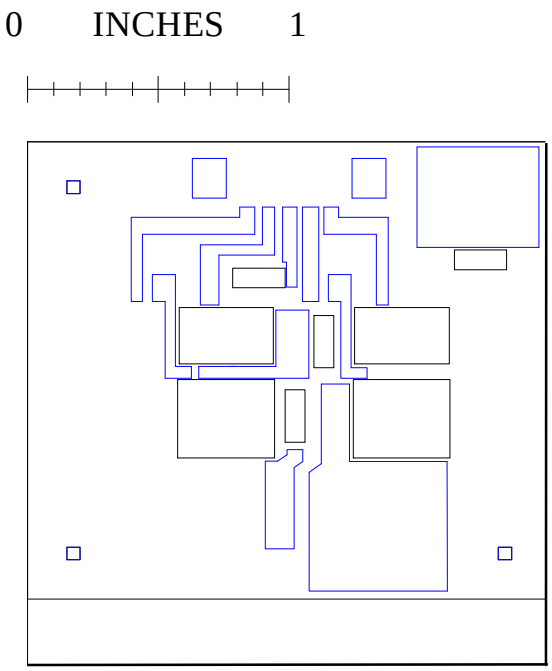


Figure 5.5: Multilayer Power Electronics Module Cross-sectional Layout



Bottom Metallization



Top Metallization

Figure 5.6: Multilayer Power Module Circuit Layout

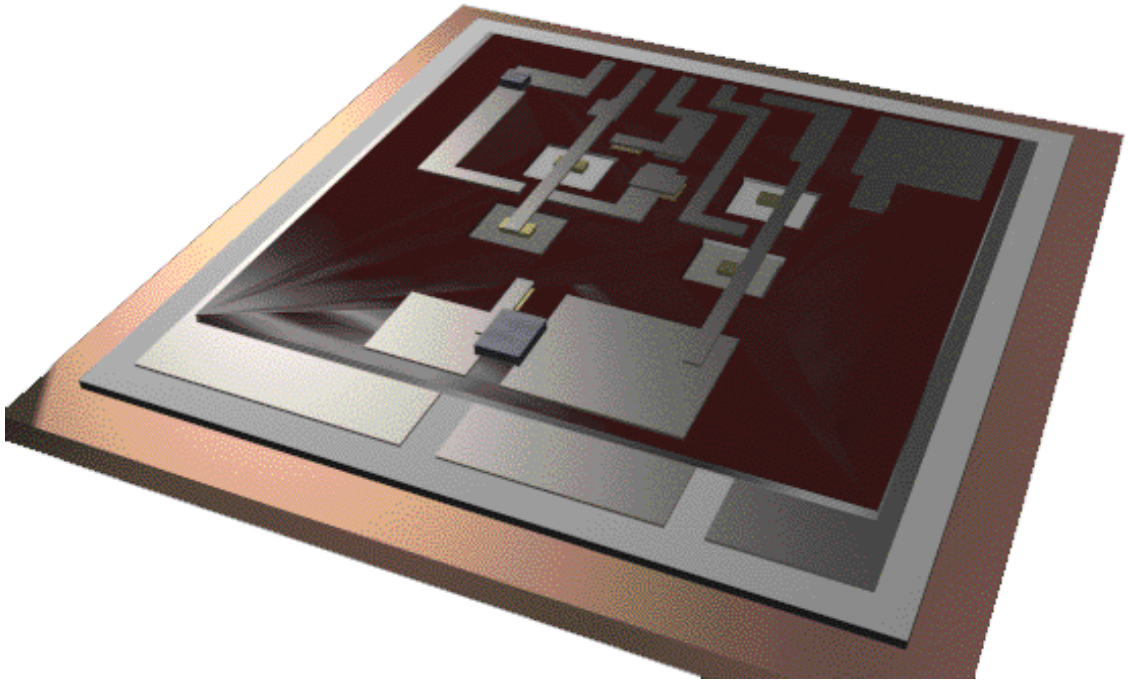


Figure 5.7: Conceptual 3D Power Module Illustration

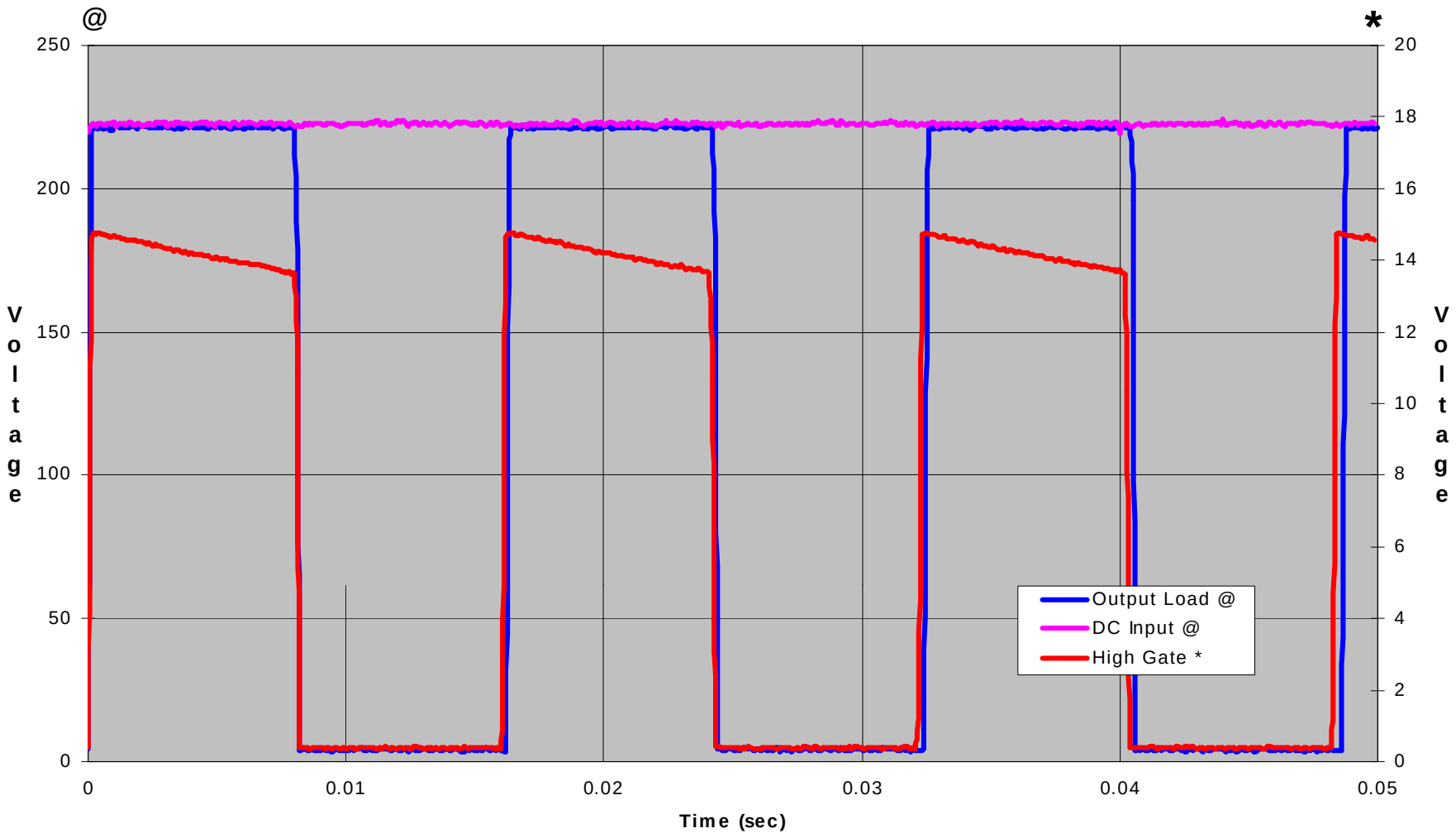


Figure 5.8: Measured Wirebond Module Waveforms

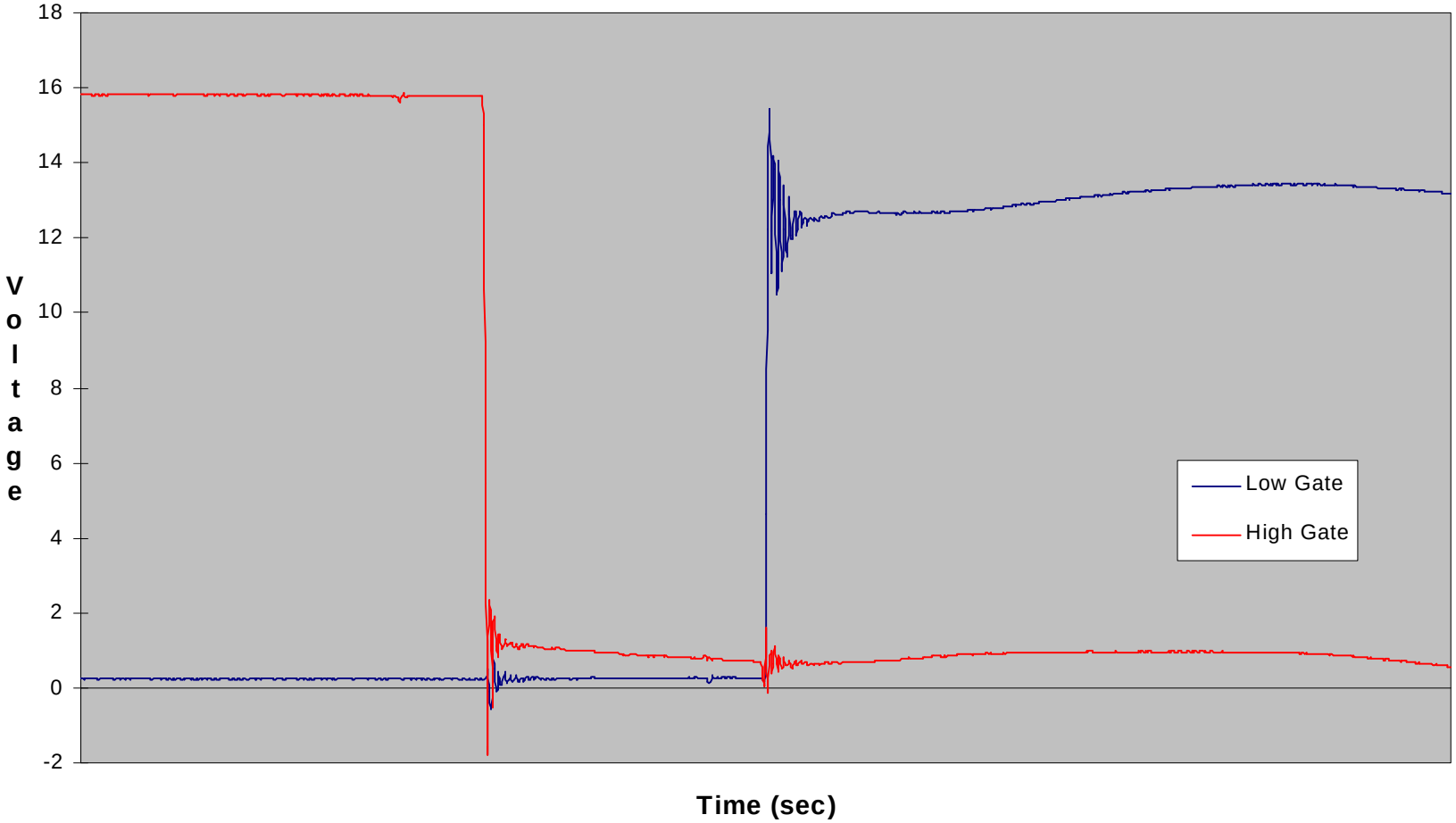


Figure 5.9: Measured High Side and Low Side Deadtime

CHAPTER 6.

POWER MODULE THERMAL ANALYSIS

6.1 Thermal Issues with Power Electronic Modules

One of the more important concerns of the power electronics module, is its thermal performance. As large amounts of power are run through the module, the devices' energy losses due to imperfect efficiency will be released as thermal energy. There are two major factors that effect the thermal performance of the power module. The first performance factor that needs to be considered is the coefficient of thermal expansion (CTE) of different materials. As the materials attempt to spread this thermal energy, they too will begin to heat up, and as they do so, they will expand. Different materials expand and contract at different rates, and this produces stress at the material interfaces. As a result, these material interfaces are the first probable areas to experience failure. In order to reduce this failure rate, it is therefore desirable to attempt to fabricate the module using layers that have closely matching CTE material characteristics.[28] The second performance factor that needs to be considered is the thermal conductivity. As the power devices release their thermal energy, that energy must then be conducted out of the power module. If this does not occur, the power module will heat up, and the devices

will quickly exceed their maximum operational temperature of 120 °C and fail. It is therefore critical that the thermal energy be dissipated as quickly and efficiently as possible.[29]

The real problem comes in attempting to solve the two performance factors at the same time. The industry-wide standard heat spreader is copper, due to its high thermal conductivity (Table II illustrates comparative material properties).[30, 31, 32, 33, 34, 35]

Table II: Material Property Comparisons

Material	**CTE (ppm/K)**	**Thermal Conductivity (W/mK)**
AlN	3.0 - 4.1	100-170
Al_20^3 (96%)	6.4	35
AlSiC (60% Al)	12.6	240
AlSiC (63% SiC)	7.9	175 (Minimum)
Aluminum	24	226
Be-BeO MMC	6.8	240
Copper	17	393
Cu-Mo	7.2	197
Cu-W (20% Cu)	7.0	248
Diamond	0.8 - 2.0	1000 – 2000
Graphite-Cu MMC	0 - 2.0 (Directional)	356 (Minimum)
Gold		317
Invar	3.1	11
Kovar	5.3	17
Molybdenum	4.9	143
Silicon	4.1	136
Silver		429
Solder		50

Copper presents problems for power electronics modules though. The most fragile part of the module is the power device, and thus it is the device interface that is the first failure to likely occur. In order to minimize this, it is therefore further desirable to attempt to match the CTEs of all of the materials to the CTE of the silicon device. If one inspects Table II, one will notice that the CTE of silicon is about 4, while that of copper is 17. This is an enormous difference, and one likely to cause great problems. The solution is to replace the copper heat spreader with another material that has high thermal conductivity but also a low CTE in order to closer match silicon.

The solution to test is to replace the copper heatspreader with a metal matrix composite (MMC) heatspreader. The MMCs do not have as high of a thermal conductivity as copper, but they have a much closer CTE match to silicon. The question is, does the gain in CTE matching outweigh the loss in thermal dissipation?

This answer was to be obtained through a combination of strategies. The main goal was to explore heat spreaders, so the wirebond module was the module of choice for testing. It is simpler in design over the multilayer module, problems are easier to diagnose, and failures are more likely to be due to thermal issues. The heatspreaders tested were AlSiC MMC, Be/Beo MMC, and copper. The MMCs are of different sizes, so each were compared with their industry standard copper equivalent in order to perform thermal analysis (Figure 6.1 illustrates heat spreader sizes). Using the wirebond module and the described heatspreaders as the test basis for thermal analysis, three major courses of action were identified, two of which were pursued in the course of this work.

The first course of action was to produce a thermal model and analyze the different cases using 3D thermal analysis software simulations (FLOTHERM).[36, 37, 38] These cases were analyzed under different thermal conditions (natural convection, forced air, and liquid cooled) and in all three dimensions in order to obtain maximum operating temperatures at steady state. These comparisons can describe the importance of thermal conductivity, and give an idea of the difference between maximum temperatures of the modules utilizing the different materials.[39]

The second course of action was to operate the wirebond modules under the identical conditions as the simulations in order to confirm the thermal models and obtain experimental verification. The third course of action was not performed in this work, and includes a series of thermal stress cycling tests upon the modules in order to analyze the projected failure reduction rate and life extension of the modules containing MMC heatspreaders.

6.2 Three Dimensional Thermal Computer Simulations

The thermal models of the power module design were based off of a physical inverter design (using IGBTs as the switching devices) that was devised here at the Microelectronics Laboratories. These thermal models are illustrated in Figure 6.2.

There are three separate model configurations which were simulated through computer analysis. The first two configurations were identical modules using only different sized heat spreaders. These heat spreaders were of equivalent dimensions to those MMCs which were donated to the Microelectronics Laboratories. By performing the simulations in this manner, the results could be verified through experimental techniques. The third configuration is that of a module that is directly integrated to a heat spreader. This layout has a significant number of advantages, most importantly the removal of entire layers. With the elimination of a copper and solder layer, significant thermal improvements were expected.

The following conditions were assumed and calculations performed:[40]

Ambient Temperature $\Rightarrow$ $T_A = 27°C = 300K$

Theramal Resistances $\Rightarrow$ $R_{Thermal\ Grease} = 0.01\ K/W$

$R_{Total} = R_{Heat\ Sink} + R_{Thermal\ Grease}$

Natural Convection (Air) $\Rightarrow$ $R_{Heat\ Sink} = 0.41\ K/W$

Forced Convection (Air) $\Rightarrow$ $R_{Heat\ Sink} = 0.10$ K/W

Forced Convection (Liquid) $\Rightarrow$ $R_{Heat\ Sink} = 0.05$ K/W

Heat Transfer from Module $\Rightarrow$ $h = \frac{1}{R_T \bullet A}$ (Illustrated in Table III).

Maximum Device

Operational Temperature $\Rightarrow$ $T_{max} = 120°C$

Table III : Configuration Dependent Variables

Variable	Configuration (1)	Configuration (2)	Configuration (3)
Heat Spreader Area	$A = (3.57 \times 10^{-3})\ m^2$	$A = (2.7 \times 10^{-3})\ m^2$	$A = (2.7 \times 10^{-3})\ m^2$
Heat Transfer			
Natural Convection (Air)	$H = 668\ W/m^2K$	$h = 882\ W/m^2K$	$h = 882\ W/m^2K$
Forced Convection (Air)	$H = 2551\ W/m^2K$	$h = 3367\ W/m^2K$	$H = 3367\ W/m^2K$
Forced Convection (Liquid)	$H = 4676\ W/m^2K$	$h = 6173\ W/m^2K$	$H = 6173\ W/m^2K$

Perfect thermal interfaces between module layers were assumed. For example, it was assumed that there were no void fractions (air bubbles) in the solder that was used to bond the power devices to the metallization traces. The power module (including heat spreader) is attached to a common predetermined heat sink, with a thermal grease

interface. Power bare die device efficiency of approximately 96.6% was assumed (see Table IV).

Table IV: Estimated Thermal Energy Dissipation per Bare Die Device

Load Power (Watts)	IGBT Thermal Energy Dissipation (Watts)	Diode Thermal Energy Dissipation (Watts)
1kW	16.66	0.66
3kW	50	2
6kW	100	4
9kW	150	6
10kW	166.66	6.66
11kW	183.25	7.25
12kW	200	8
13kW	216.66	8.66

The thermal models were run through various simulations at various power levels under various conditions in order to obtain comparison graphs. The first series of simulations illustrates the impact of heatspreader design and conditions upon the maximum module temperature (at 3kW load).

The next series of tests were performed upon configuration (2) in an attempt to determine the most effective substrate thicknesses for various materials.[41] The simulations were run with a load power of 6kW, copper and AlSiC (60% Al) heat spreaders, and AlN and diamond (k=2000) substrates, as illustrated in Figure 6.3. As expected, if the thermal conductivity of the substrate is less then that of the heat spreader, as is the case for the AlN substrate modules, the substrate acts as a thermal chokepoint.

As the substrate thickness increases, so does the maximum temperature of the module. Conversely, if the substrate thermal conductivity is greater then that of the heat spreader, then the maximum module temperature decreases as the substrate thickness increases. The interesting observation arises in that in all cases, the temperature seems to level off at a substrate thickness of about 2.5 mm, indicating that the geometrical properties of the substrate outweigh the thermal properties at that point.

The next series of simulations were performed in an attempt to determine the effect of the heat spreader thickness upon the maximum temperature of the module. Again, the computer tests were performed upon configuration (2). Figure 6.4 illustrates the effect of AlSiC (60% Al) heat spreader thickness upon the maximum module temperature under various load powers. Figure 6.5 illustrates a comparison of copper and AlSiC (60% Al) heat spreader materials under various thicknesses with a 6kW load power. The interesting conclusion that can be drawn, is that for all cases, the temperature performance levels off with a heat spreader thickness of approximately 6mm, regardless of load power or heat spreader material (once again indicating a high dependence upon geometry).

The next tests were performed in an attempt to compare the effects of different materials upon the module temperature. By changing one material type at a time in the 3D thermal power module model, the effects of those material changes upon the maximum module temperature could be observed. Assuming 120°C as the maximum operational temperature of the bare die devices, the maximum operational power of the module using a specific material could then be identified. The ultimate goal is to achieve

CTE matching (and thus improving expected lifetime) with as little thermal conductivity loss as possible. This conductivity loss will be observable in the reduction of the module's maximum operational power.

The base power module simulated was that illustrated in Figure 2, using the industry standard materials of an AlN DBC substrate and copper heat spreader. Two series of simulations were performed. The first series replaced the copper heat spreader with various experimental material heat spreaders of the same dimensions, which were then compared, as illustrated in Figure 6.6. The second series replaced the AlN ceramic substrate of the DBC with various materials, which were also then compared, as illustrated in Figure 6.7.

It can be seen from Figure 6.6 that an industry standard power module utilizing a copper material heat spreader (which is also industry standard) reaches its maximum operational temperature of 120°C when it is operating at a load power level of approximately 9.5 kW. The same value can be seen in Figure 6.7. In that series, the industry standard copper heat spreader is used in all cases, and the substrate material of the DBC is changed and compared. It can be seen that for the industry standard AlN ceramic substrate, the maximum operational temperature of 120°C is reached when the module is operating at a load power of approximately 9.5kW. Therefore, for the thermal model layout of Figure 2, 9.5kW is the maximum operational power level of a module utilizing the industry standard copper heat spreader with an AlN DBC. All other comparisons can be made to that single value in order to observe their impact.

As can be seen from Figure 6.6, the graphite-copper material presents itself as an extremely promising candidate as a heat spreader material. It has a thermal conductivity of 356 W/mK, almost equaling that of copper, while at the same time having a CTE of approximately 2.0 ppm/K which is much closer to silicon than copper's CTE of 17 ppm/K to matching silicon's CTE of about 4.1 ppm/K. It can be seen that MMC materials such AlSiC and Be-BeO offer enormous potential advantages in CTE matching while paying a small price in maximum power degradation. While copper-graphite is still in its experimental phases, AlSiC and Be-BeO MMCs are now becoming readily available on the commercial market.

Figure 6.7 illustrates the enormous advantage of diamond materials over today's industry standard AlN or even Be-BeO ceramic substrates. Diamond offers an approximate 25% maximum power output increase over the AlN and Be-BeO substrates, not to mention its outstanding thermal spreading characteristics.[42, 43] This is of extreme importance, even though diamond substrates are still currently a costly expenditure. It can be seen that the lower grade diamond (carbon graphite) also has a great impact upon the module's thermal performance, and this material is much more cost effective then the pure diamond material. Figure 6.8 illustrates the actual FLOTHERM graphical outputs for comparisons between substrate materials. These test cases were performed with a forced air convection heat sink and a 10kW load in order to graphically illustrate the excellent thermal dissipation capabilities of the diamond substrates.

A module cross-sectional layout alteration could also greatly increase thermal management performance, as is the case for a directly integrated heat spreader. Figure

6.1 illustrates a module in which a copper-ladded substrate has been directly bonded to an MMC material heat spreader. The advantage of such a configuration is the elimination of an entire material layer as well as the layer of solder which bonds it to the heat spreader. The materials used in the thermal simulations of this module were identical to those used in the DBC power module layout, the results of which are illustrated in Figures 6.9 and 6.10.

The results here indicate that the module's power performance actually increases slightly for most materials over the DBC module using those same materials (which is an added bonus). The real advantage of such a configuration, however, comes into play due to the elimination of entire material layers. With the elimination of layers comes a reduction in the number of bonded interfaces, and thus a reduction in likely stresses and failure points. All of this results in an overall increases in the module's life expectancy. In addition, the thermal conductivity would likely improve more than is indicated in the simulations. For thermal analysis purposes, it was assumed that soldering bonds were 100% perfect bonds, which definitely is not the case in real life production where void fractions are the norm. Soldering layers are areas which greatly degrade thermal conductivity potentials. The integrated heat spreader module eliminates an entire solder layer, the result of which will greatly enhance performance from a thermal conductive standpoint.

One of the purposes for using these thermal model configurations was so the simulations could be experimentally verified through measured thermal imaging. The four wirebond modules that were physically built for testing were two of configuration

(1), one with a copper heat spreader and one with an Be-BeO heat spreader, and two of configuration (2), one with a copper heat spreader and one with an AlSiC heat spreader. These specific cases are therfore singled out for further investigation.

Figure 6.11 illustrates a particular test case of configuration (1) in which copper heat spreader and Be-BeO heat spreader modules were placed under a 3kW load using AlN DBC substrates, and forced air convection heatsinks. Figure 6.12 illustrates a test case of similar conditions with configuration (2) modules using a copper heat spreader and AlSiC heat spreader. Both of these figures are the actual FLOTHERM three dimensional graphical outputs for those particular cases, and through these figures, it is easier to get an idea of how the heat flows through the module and how well the material spreads the dissipated thermal energy.

As shown in these, it can be seen that when replacing the copper heat spreader with an MMC of equivalent size, the maximum module temperature rises by only about 5%. This is a result indicating that the loss in thermal conductivity when switching to MMC heat spreaders from copper is small. Figures 6.13 and 6.14 illustrates the load power versus temperature for both of these comparisons. As can be seen, the maximum operational power of the copper and MMC modules differs by only about 0.5 kW, or about 5%, thus again verifying the before mentioned conclusion.

It must also be pointed out that since these are comparisons between identical models, with a specific material being the only variable, any errors made in calculated assumptions will cary over to all of the configuration models, and thus will have no effect on the *comparitive* results. It can be concluded from these results that if the lifetime of

the module is indeed increased and failure rate decreased by changing to an MMC heat spreader, then the gain will be well worth the small loss in thermal energy dissipation capabilties.

6.3 Experimental Thermal Testing

In order for the computer thermal simulations to be valid, they had to be based off of power module designs from which the thermal data could be experimentally verified. To this end, the Microelectronics Laboratories at Virginia Tech designed, built, and tested a standard inverter power module, taking experimental thermal data from modules attached to AlSiC MMC heat spreaders, Be-BeO MMC heat spreaders, and the industry standard copper heat spreaders.

The power modules were run with a 3kW resistive load and thermal heat maps were obtained of the bare die devices. Figure 6.15: Bare Die Thermal Heat Map illustrates an example, with the maximum operating temperature of the power module (with Be-BeO heat spreader) as approximately 55°C with a 3kW load, thus verifying within 5% error the validity of the computer thermal simulations.

This experimental result can compared to the graphical thermal simulation of Figure 6.12 for testing verification. Figure 6.12 illustrates the computer simulation that was performed with an identical model module and with as closely matching environmental conditions as possible in order to match those of the experimental test. As stated, the error of the die temperature was within 5%.

Though experimentally acceptable, the error in the verification of thermal measurements can be attributed to the error in the predicted efficiency of the IGBTs and thus their thermal energy dissipation. It was predicted that the module would dissipate approximately 104 watts of thermal energy. By measuring the input power and output power, the power lost to thermal dissipation in the module could be obtained, and it was

determined to be 86 watts. This difference accounts for a large portion of the small difference between the simulated maximum of 60 ^{o}C and the actual temperature observed of 55 ^{o}C. Another factor that contributed to the error of thermal model was that of ambient temperature. The thermal simulations were performed under conditions with the T_A = 27 ^{o}C, while the actual experimental testing was performed under the condition of the T_A = 22 ^{o}C. This also accounts for a large portion of the thermal error.

Other factors that could contribute to simulation error are bonded interfaces. The assumption made was that all material interfaces formed perfect bonds, which is hardly the case in reality. Solder is a prime example of such a nuisance, where void fractions often reach up to 50%. Material thermal conductivity could also account for error in the simulations. The computer models used material thermal conductivity values which are on the average. MMCs especially have a high degree of thermal conductivity variation from one component to the next, due to their high sensitivity to exact composition percentages.

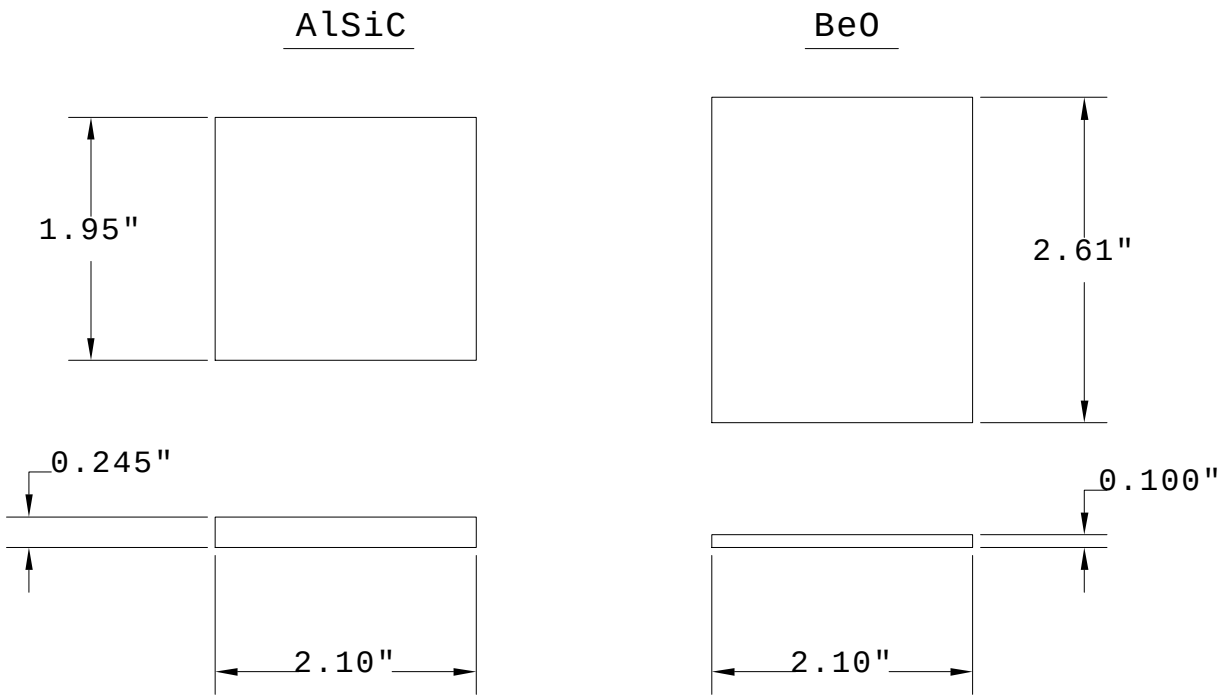


Figure 6.1: Heat Spreader Sizes

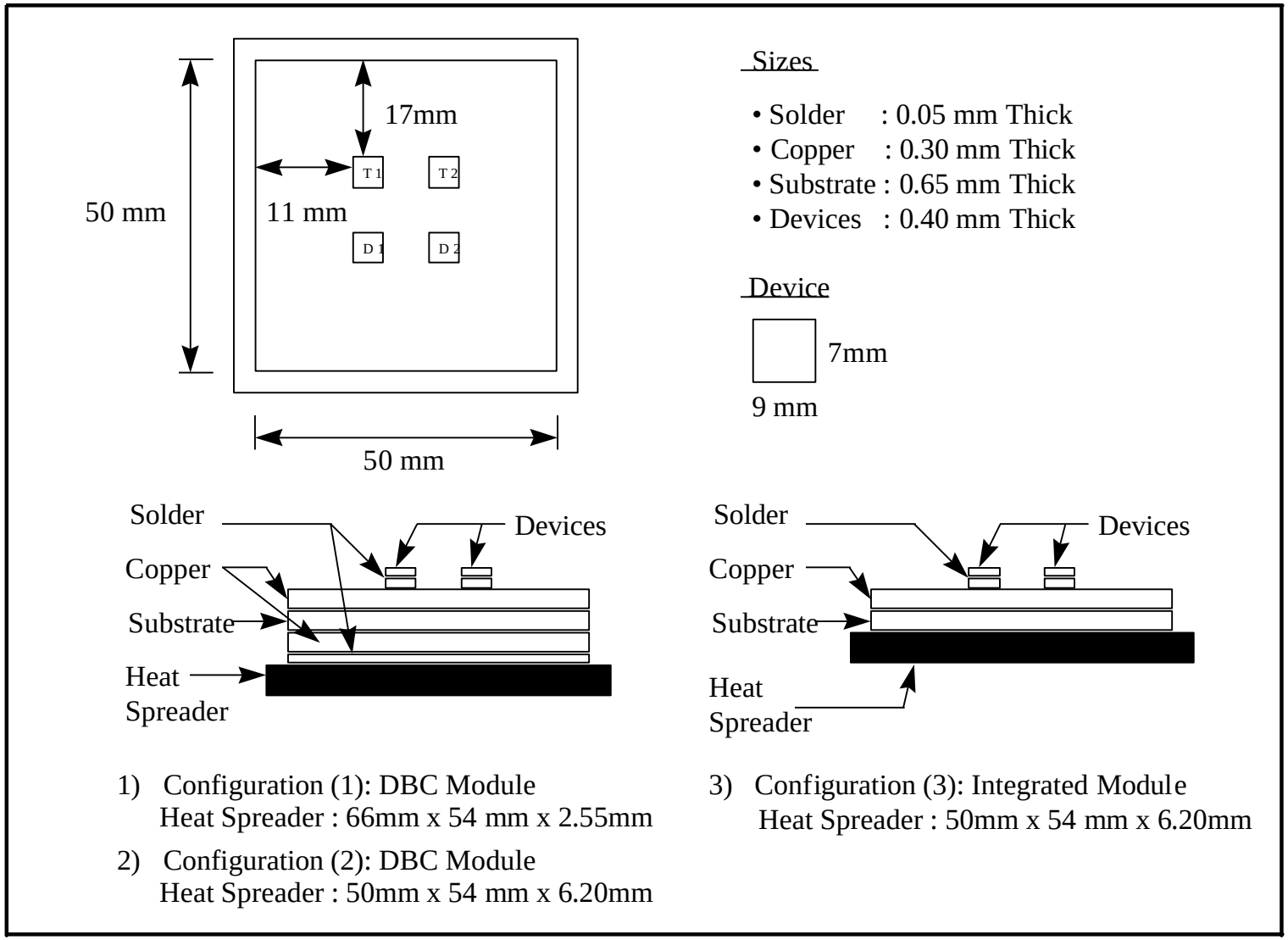


Figure 6.2: Thermal Model Layouts

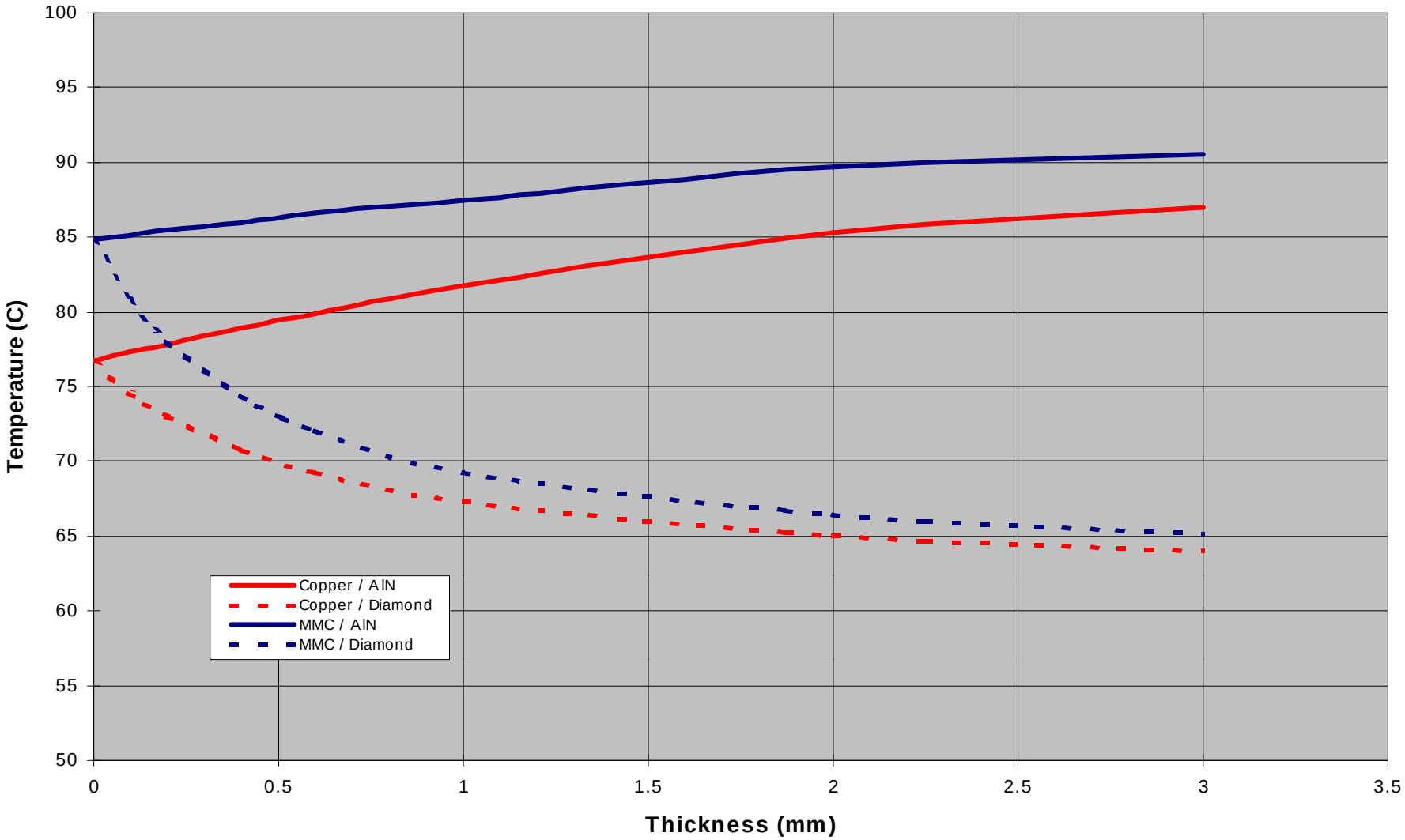


Figure 6.3: Substrate Thickness Comparison

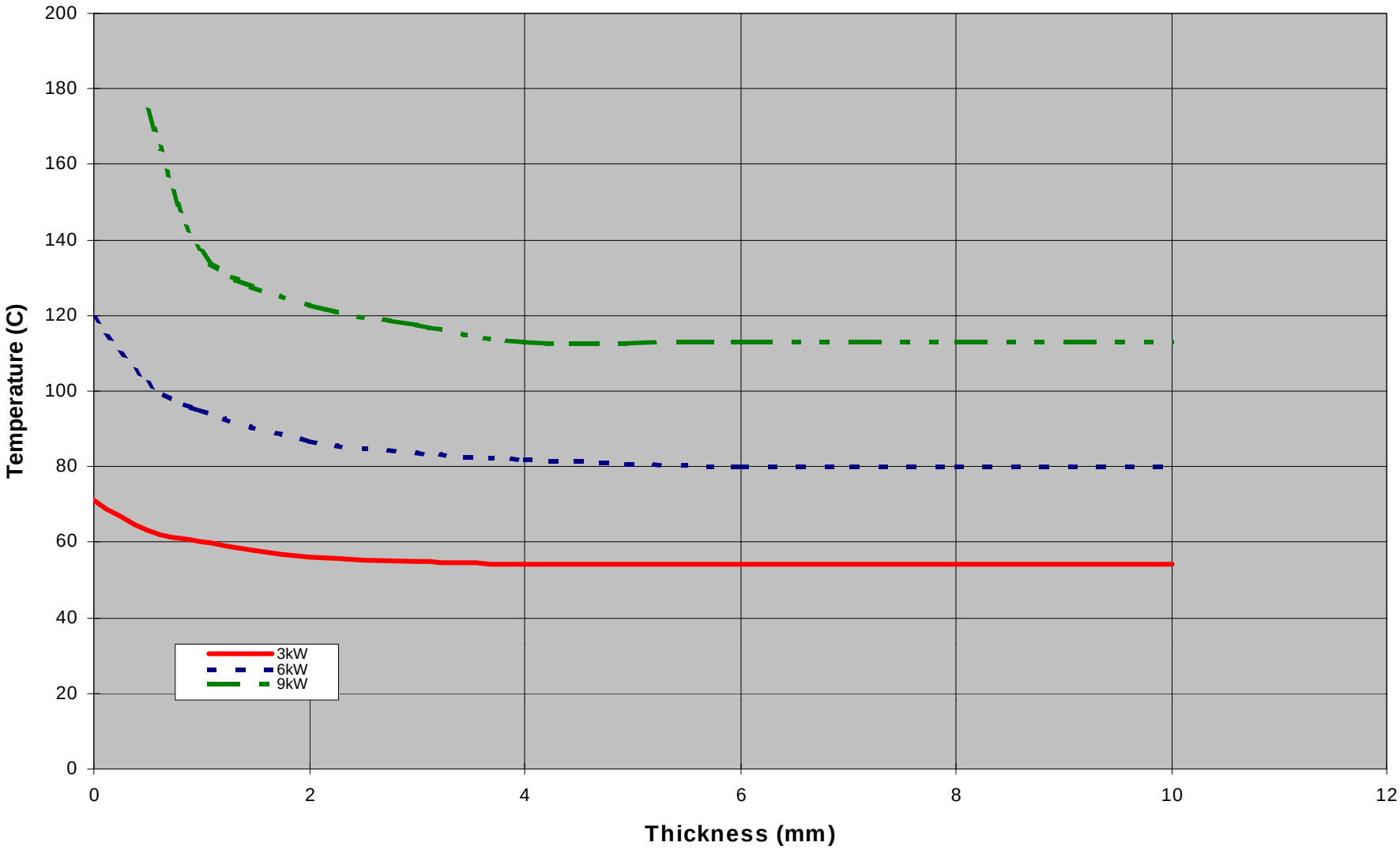


Figure 6.4: Heat Spreader Thickness Comparison

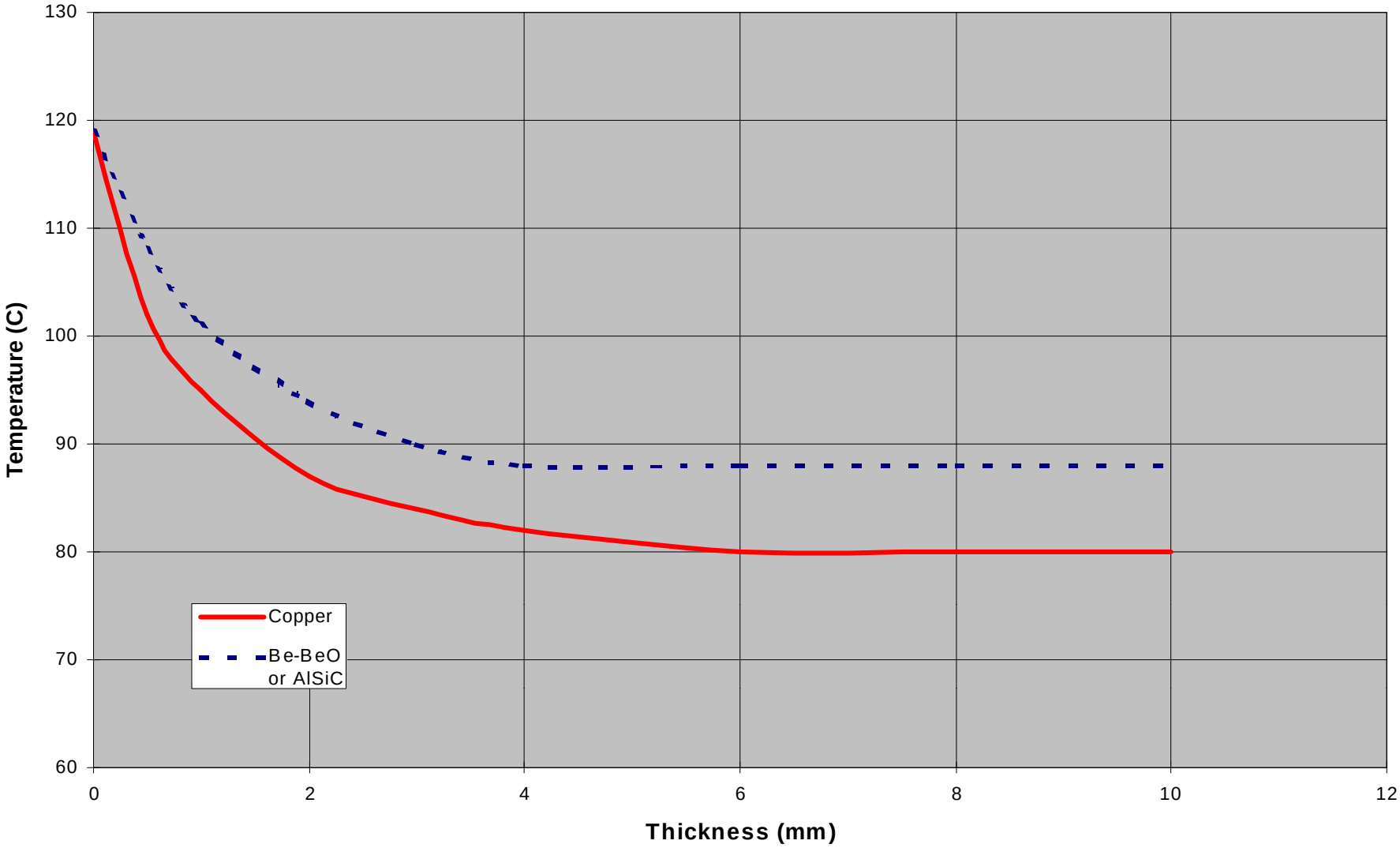


Figure 6.5: Heat Spreader Thickness Comparison

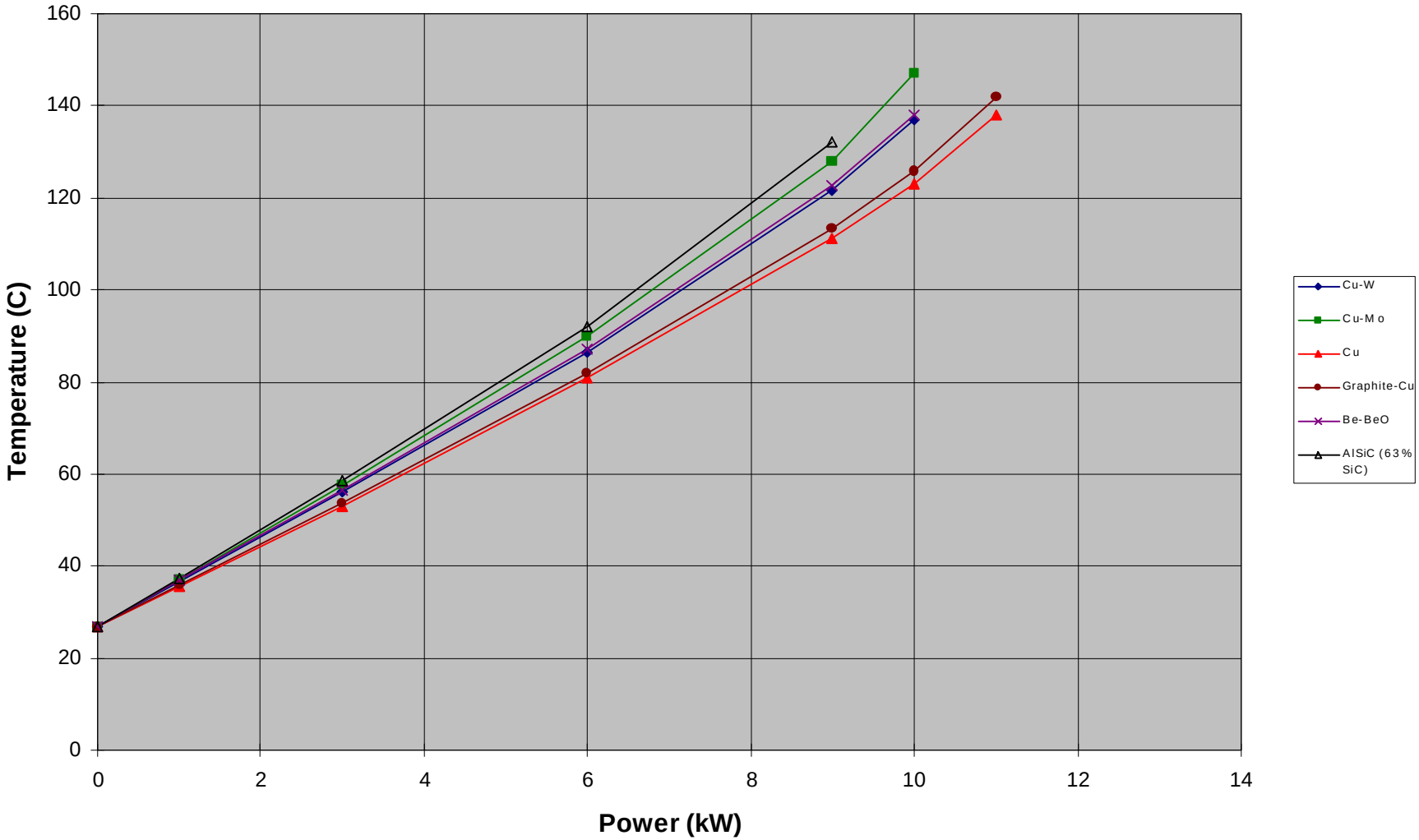


Figure 6.6: Heat Spreader Material Comparisons

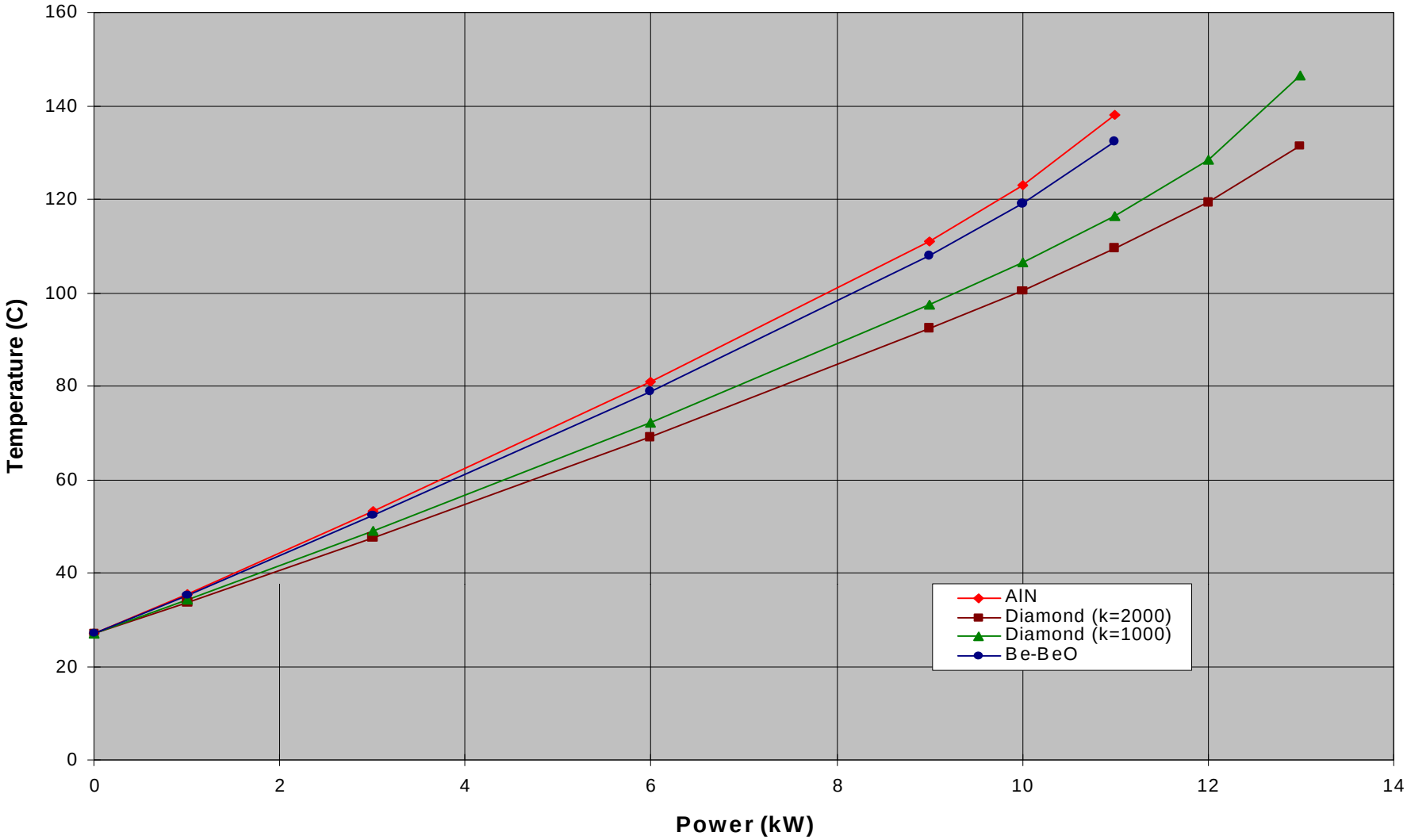


Figure 6.7: Substrate Material Comparisons

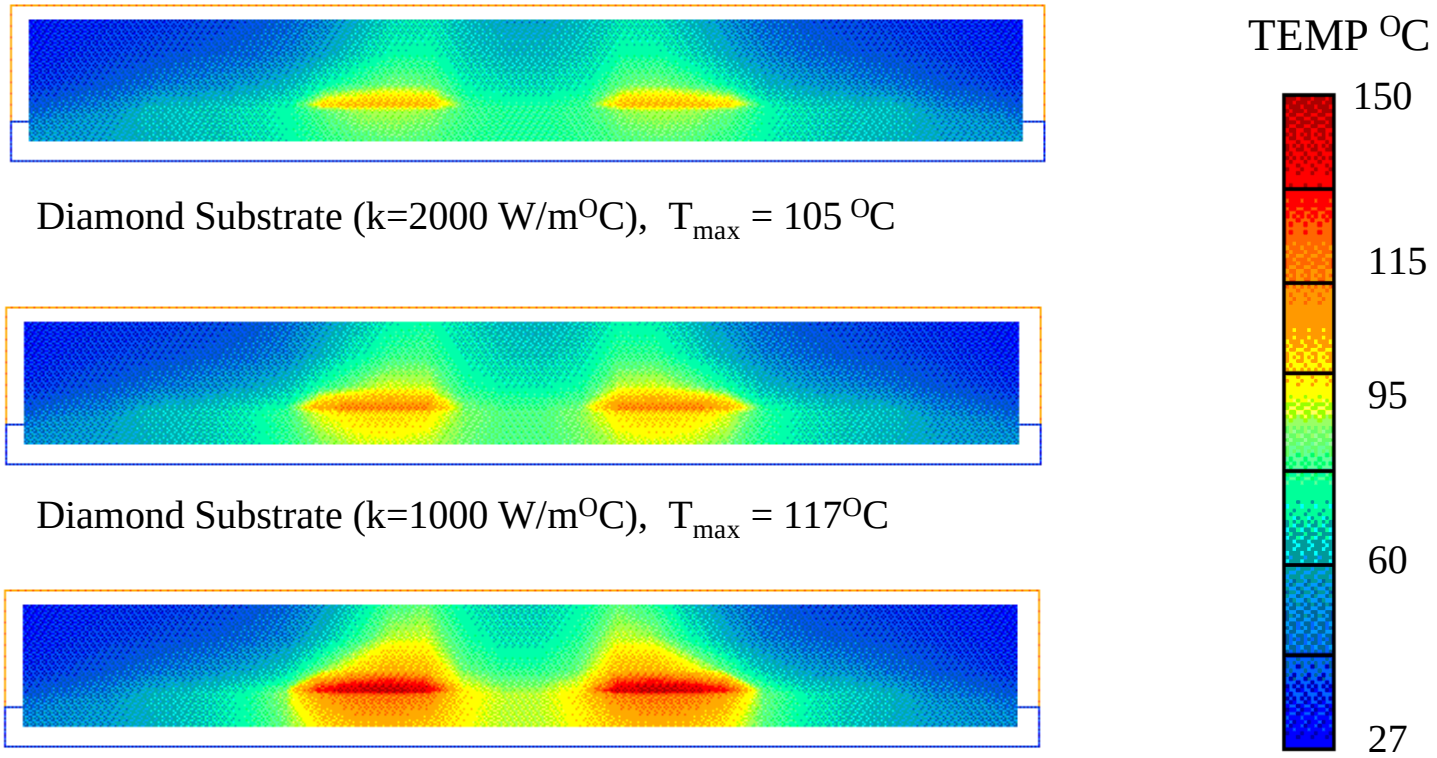


Figure 6.8: Diamond and AlN Substrate Graphical Comparisons

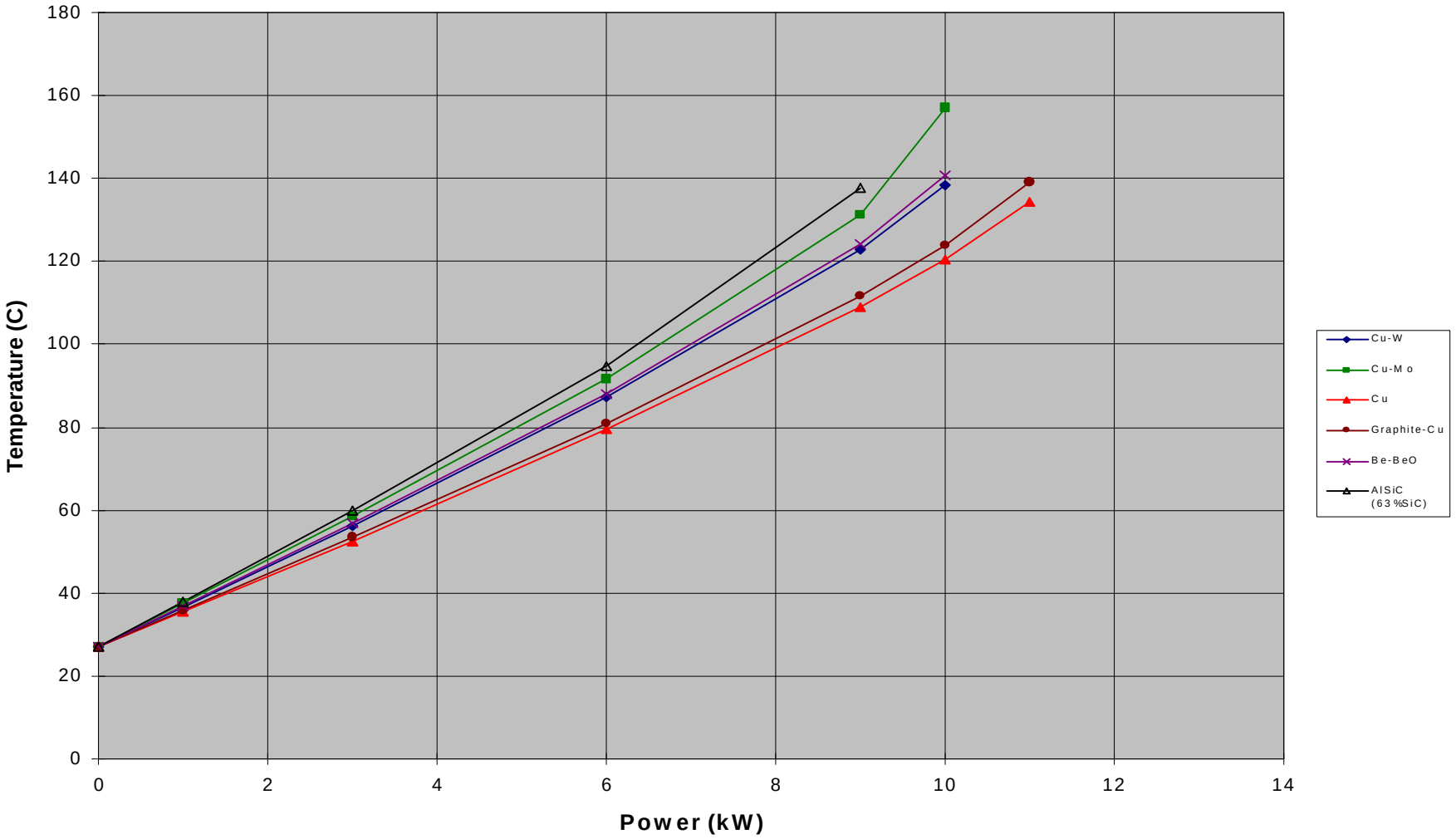


Figure 6.9: Heat Spreader Material Comparisons of Integrated Power Module

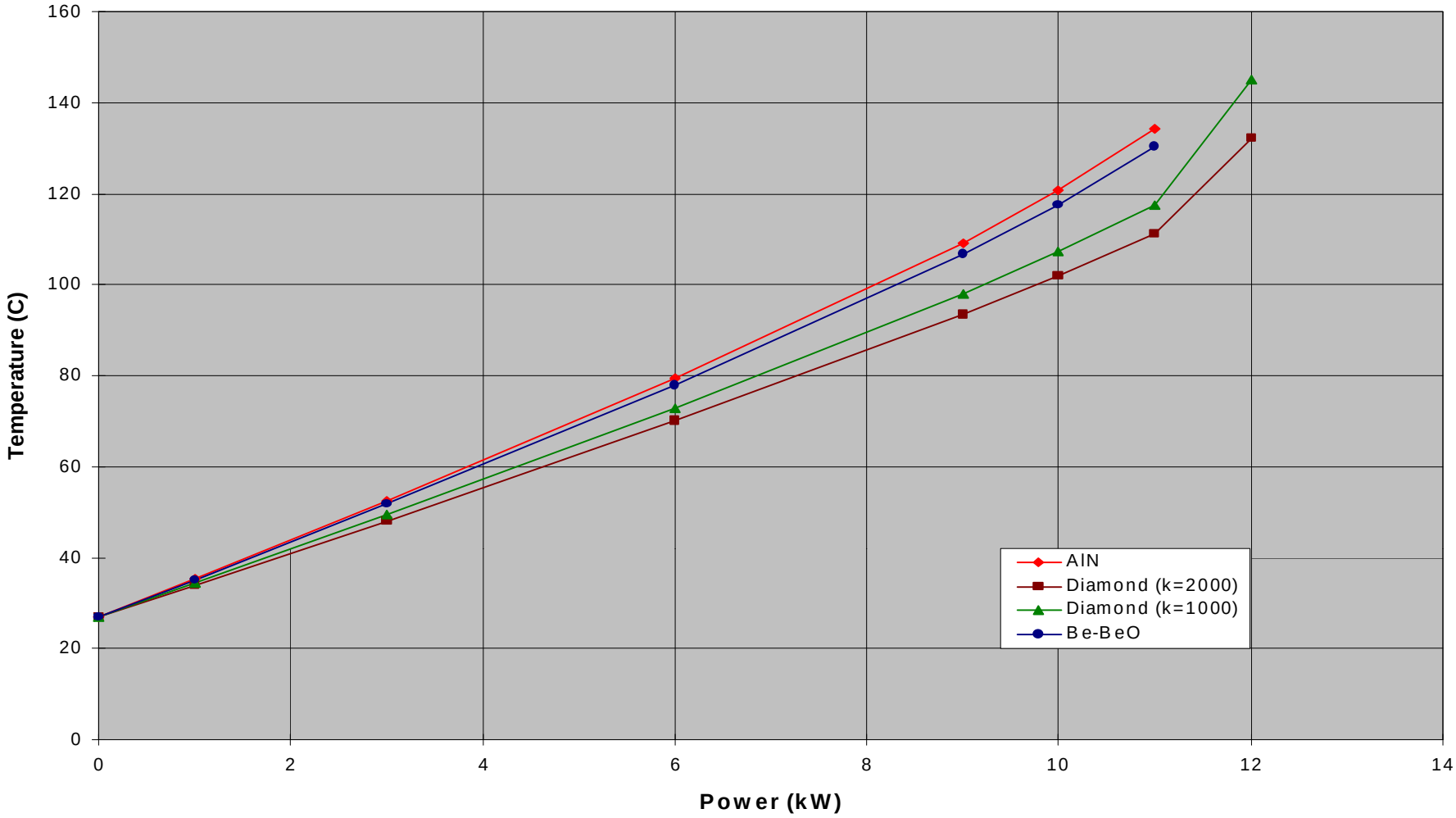
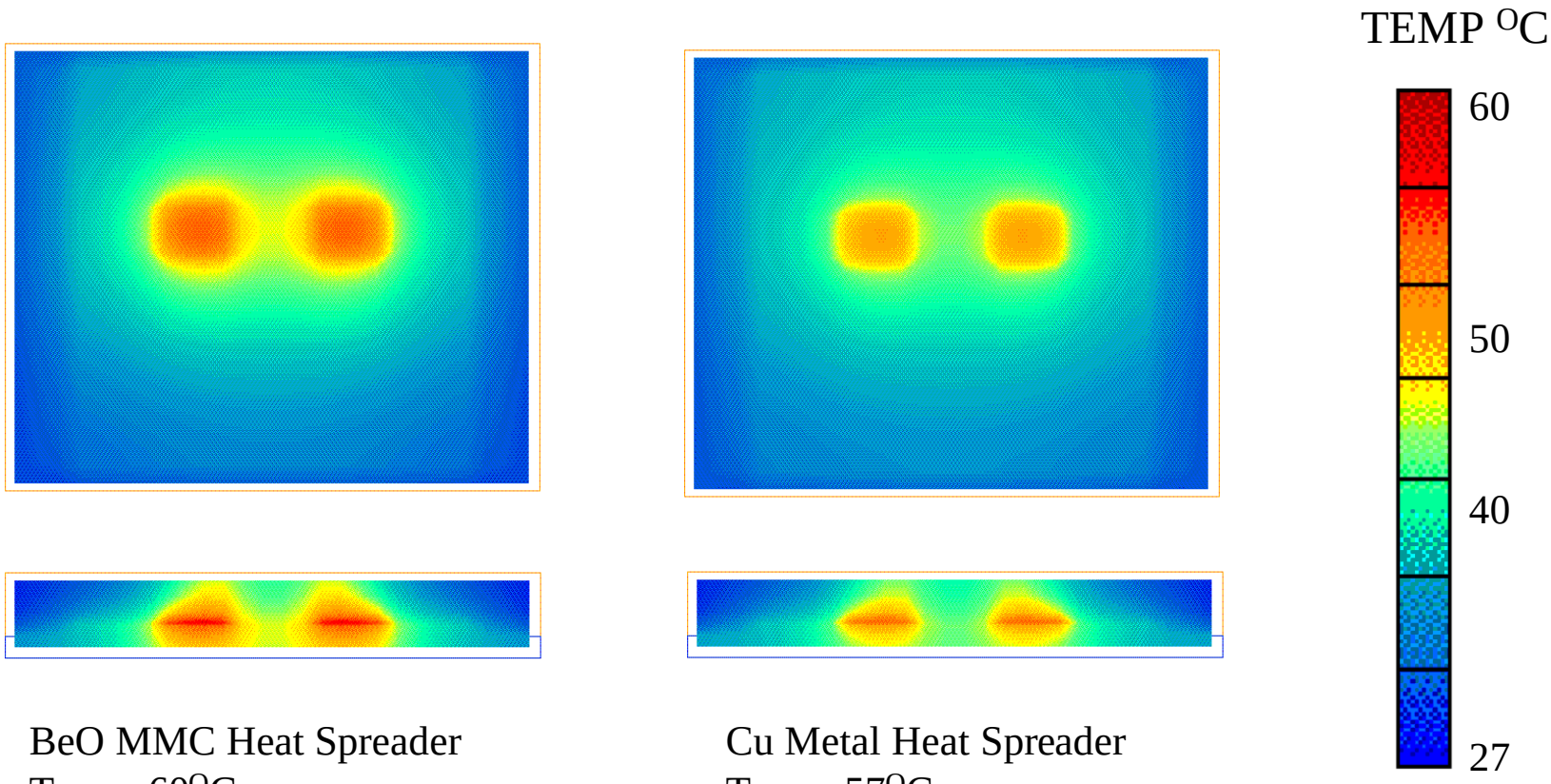


Figure 6.10: Substrate Material Comparisons of Integrated Power Module

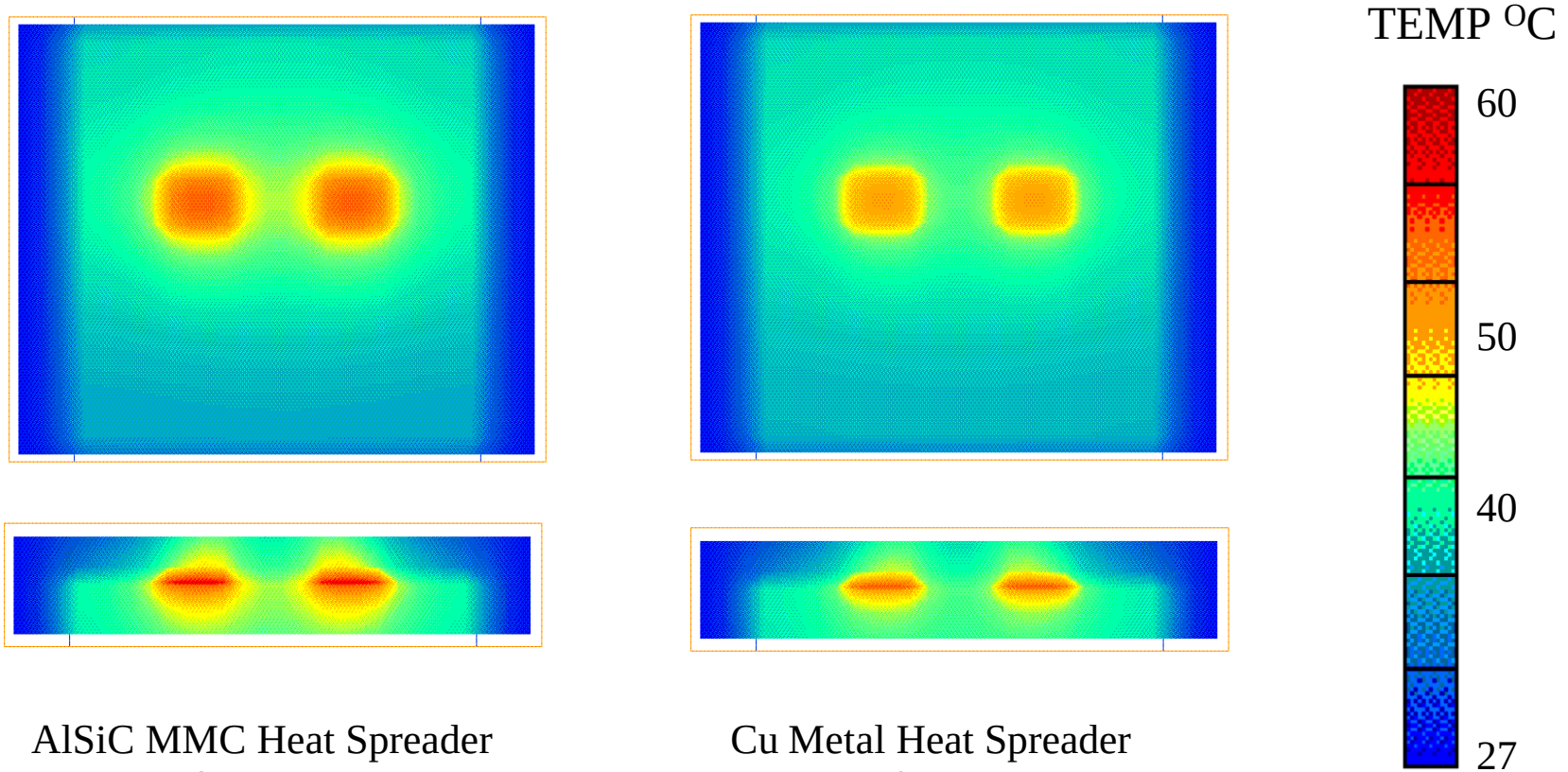


BeO MMC Heat Spreader
T_{max} = 60^{O}C

Cu Metal Heat Spreader
T_{max} = 57^{O}C

ΔT=5.0%

Figure 6.11: Be-BeO MMC and Copper Graphical Comparison



AlSiC MMC Heat Spreader
T_{max} = 56^{O}C

Cu Metal Heat Spreader
T_{max} = 53^{O}C

ΔT=5.4%

Figure 6.12: AlSiC MMC and Copper Graphical Comparison

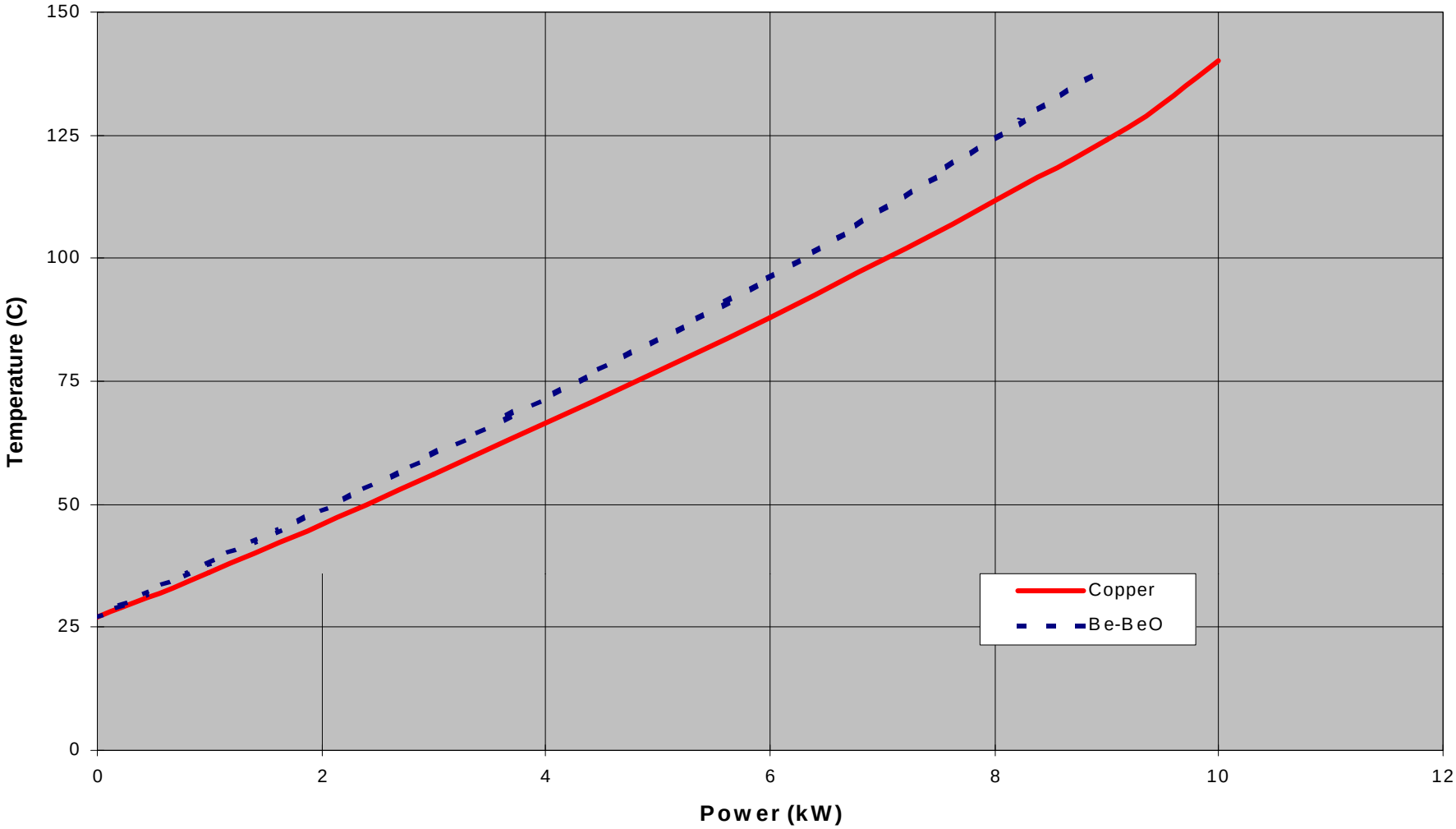


Figure 6.13: Be-BeO MMC and Copper Heat Spreader Comparisons

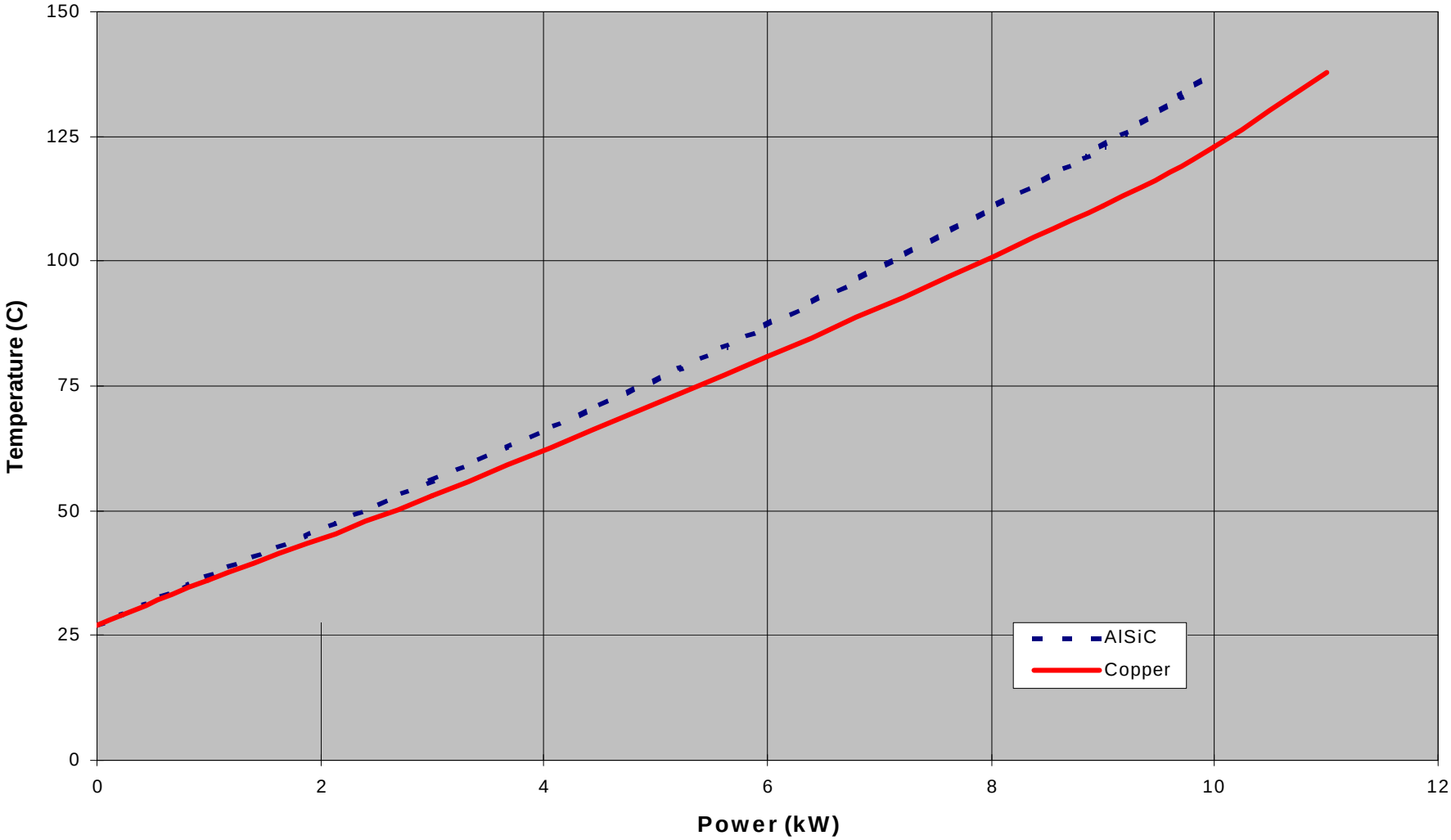


Figure 6.14: AlSiC MMC and Copper Heat Spreader Comparisons

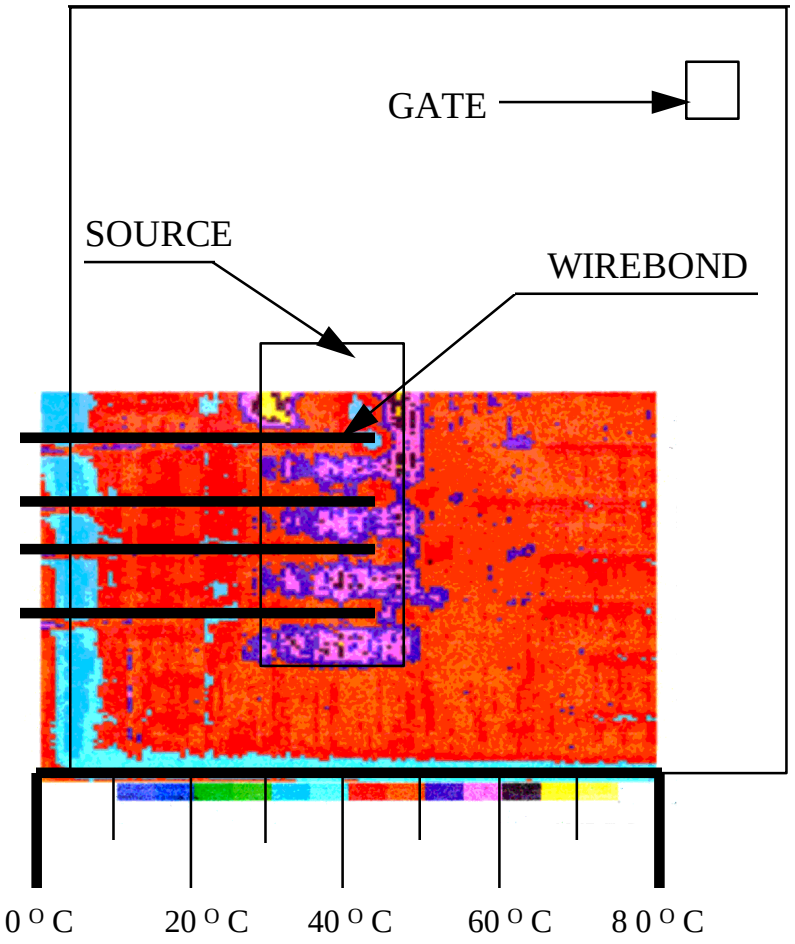


Figure 6.15: Bare Die Thermal Heat Map

CHAPTER 7.

CONCLUSIONS

The research of the Microelectronics Laboratory has produced working power electronic modules of single layer and multilayer configurations. The work has covered material and thermal issues of module construction as well as the electronic issues of circuit drive and module testing.

The half-bridge power converter circuit was chosen as the basic module for this research due to the overwhelming industry-wide use of the half-bridge. Driver controls and switching devices were explored, power converter circuits tested, and an electronic testbed devised for use with the power module.

Multilayer fabrication techniques have been explored, including the bonding of Direct Bond Copper, AlN substrates, polymers, and copper through the use of adhesives under high temperature and pressure. Soldering techniques with multiple temperature solders has been investigated and the bonding of bare die performed. Thin film and electroplating techniques were used to reduce oxidation problems and increase surface bondability.

Thermal issues were investigated, including a multitude of computer simulations under various environmental and load conditions (using FLOTHERM software). Materials were tested, experimentally and theoretically, including high performance heat spreaders and substrates such as Metal Matrix Composites and diamond based materials. Finally, the thermal simulations were experimentally validated through the thermal mapping of wirebond modules under conditions matching those of the simulations.

The advantage of the multilayer power electronics approach is that this strategy will reduce interconnect inductances, increase system efficiency and performance, produce a standard for power electronic building modules, lower power system costs, and increase power system reliability. The concept of power electronic modules would prove especially valuable for systems using half bridge and full bridge converters; these systems currently contain large amounts of inductances between separate bridge legs, which when removed through the use of power electronic modules, would greatly increase industry wide performance and reduce overall costs.

The researcher will continue these investigations in the pursuit of his P.h. D. Now that the multilayer concept has been proven as a viable process, the work will progress to integrate the control circuitry and power circuitry into a single module as planned. Investigations will continue in the area of thermal design, and stress and reliability concerns will also be addressed. Finally, high performance, low loss converter topology will be explored with the emphasis of the research placed on computer or microprocessor control.

APPENDIX A

Solder Temperature Profiles

Browning Open Air Belt Drive Reflow Soldering Unit

Solder	Temperature Profile °C					Speed
#209	50	170	268	170	50	8
#104	50	155	214	155	50	8
#1E	50	140	153	140	50	8

Infrared Reflow Soldering Unit

Solder	UP (V)	LP (V)	US (V)	LS (V)	Speed
#209	100	100	230	110	0.2
#104	100	100	190	110	0.18

Indalloy #	Composition (%)	Liquidus (°C/°F)	Solidus (°C/°F)	Density (g/cm^3)	Electrical Conductivity (% of Cu)	Thermal Conductivity (W/cm°C) @ 85°C	Thermal Coefficient of Expansion (µm/m°C)	Tensile Strength (PSI)	Bond (Shear) Strength (PSI)	% Elong-ation* (1 in.)	Young's Modulus (PSI x 10^6)	Brinell Hardness	
117	44.7Bi 22.6Pb 19.1In 8.3Sn 5.3Cd	47/117	47/117	9.16	3.3 - 4.5	0.15	25	5400		37.5 (1.5 in.)		16.5'	
136	49Bi 21In 18Pb 12Sn	58/136	58/136	9.01	2.43	0.10	23	6300				16.5'	
140	47.5Bi 25.4Pb 12.6Sn 9.5Cd 5In	65/149	57/134	9.47	2.0	0.15		3725		77.5		14.0	
158	50Bi 26.7Pb 13.3Sn 10Cd	70/158	70/158	9.58	3.8 - 4.2	0.18	22	5990	300	120		14.5	
23	50Bi 25Pb 12.5Sn 12.5Cd	73/163	70/158	9.50	3.1			4550		30		25*	
160-190	42.5Bi 37.7Pb 11.3Sn 8.5Cd	88/190	71/160	9.43	4.3			5400	300	22		9	
8	44In 42Sn 14Cd	93/199	93/199	7.46		0.36	24	2632					
39	52Bi 30Pb 18Sn	96/205	96/205	9.85	3.0	0.13		5178		100		15.5'	
IE	52In 48Sn	118/244	118/244	7.30	11.7	0.34	20	1720	1630	83		4.3 - 4.9	R
255	55.5Bi 44.5Pb	124/255	124/255	10.44	4.0	0.04		6400		37.5		15'	
1	50In 50Sn	125/257	118/244	7.30	11.7	0.34	20	1720	1630	83		4.3 - 4.9	
13	70In 15Sn 9.6Pb 5.4Cd	125/257		7.63		0.39	27	1476	2000			4	
281	58Bi 42Sn	138/281	138/281	8.57	4.5 - 5.0	0.19	15	8000	500	55		23'	
△ 290	97In 3Ag	143/290	143/290	7.38	23.0	0.73	22	800				2	P R
181	51.2Sn 30.6Pb 18.2Cd	145/293	145/293	8.45		0.35	24.4	6263					
2	80In 15Pb 5Ag	154/300	149/288	7.85	13.0	0.43	28	2550	2150	58		5.2	R
4	100In	157/315		7.31	24.0	0.86	29	273	890	22 - 41	1.57	0.9	R
9	70Sn 18Pb 12In	167/333	154/309	8.04	12.2	0.45	24	5320	4190	135.5		12	
281-338	60Sn 40Bi	170/338	138/280	8.21	1.4*	0.30		8478		35		23.5'	
101	50Pb 30Sn 20Bi	173/343	130/266	9.85	0.8*			4400	2900	42			
△ 204	70In 30Pb	171/347	162/329	8.19	8.8	0.38	28	3450					P
104	62.5Sn 36.1Pb 1.4Ag	179/354	179/354	8.41	11.6	0.31	25.2	7000				14.6	R
- ✳ 62-36-2	62Sn 36Pb 2Ag	179/354	179/354	8.41	11.9	0.50	27	6380	7540				
5	37.5Pb 37.5Sn 25In	181/358	134/274	8.84	7.8	0.23	23	5260	4300	101		10.2	
205	60In 40Pb	187/358	173/343	8.52	7.0	0.29	27	4150					R
106	63Sn Pb37	183/361	183/361	8.40	11.5	0.50	25.0	7500	6200	37	4.35	17	R
108	70Sn 30Pb	186/367	183/361	8.17	12.5		22	7500	5200	30	5.08	17	
226	83.6Sn 8.8In 7.6Zn (patented)	187/369	181/358	7.27				6600		85.5	4.0		

R: RIBBON (MUST ADD FLUX)

P: PASTE (INCLUDES FLUX)

Indalloy #	Composition (%)	Liquidus (°C/°F)	Solidus (°C/°F)	Density (g/cm^3)	Electrical Conductivity (% of Cu)	Thermal Conductivity (W/cm°C) @ 85°C	Thermal Coefficient of Expansion (µm/m°C)	Tensile Strength (PSI)	Bond (Shear) Strength (PSI)	% Elong-ation* (1 in.)	Young's Modulus (PSI x 10^6)	Brinell Hardness
227	77.2Sn 20In 2.8Ag (patented)	187/369	175/347	7.25	9.8	0.54	28	6800	4800	47	5.6	17
109	60Sn 40Pb	191/376	183/361	8.5	11.5	0.49	25.2	7600	5600	40	4.35	16
201	91Sn 9Zn	199/390	199/390	7.27		0.61		7940		32.5		21.5
7	50In 50Pb	205/410	183/363	8.86	6.0	0.22	27	4670	2680	55		9.6
116	50Sn 50Pb	212/414	183/361	8.90	10.9	0.48	23.4	6000	5200	35		14
121	96.5Sn 3.5Ag	221/430	221/430	7.36	16.0	0.33	30.2	5620		73		40
206	60Pb 40In	226/448	205/387	9.3	5.2	0.19	26	5000				
128	100Sn	232/450	MP	7.28	15.6	0.73	23.5	1900			6.1	
209	65Sn 25Ag 10Sb	233/451	MP	7.80			36	17000				
3	90In 10Ag	237/459	143/289	7.54	22.1	0.67	15	1650	1600	61	6.1	2.7**
130	60Pb 40Sn	238/460	183/361	9.28	10.1	0.44	24.7	5400	4600	25	3.34	12
132	95Sn 5Ag	240/464	221/430	7.39	12.6		23.2	4780	3540	49 (2 in.)		13.7
133	95Sn 5Sb	240/464	235/455	7.25	11.9	0.28	31.1	5900	6000*	38		13.3
10	75Pb 25In	260/502	240/464	9.97	4.6	0.18	26	5450	3520	47.5		10.2
150	81Pb 19In	275/527	260/500	10.27	4.5	0.17	27	5550				
149	80Pb 20Sn	280/536	183/361	10.04	8.7	0.37	26.6	4800	3000	20	2.9	11
182	80Au 20Sn	280/536	280/536	14.51		0.57	15.93	40000	40000	2	8.57	
155	90Pb 5Ag 5Sn	292/558	292/558	11.15		0.25						
151	92.5Pb 5Sn 2.5Ag	296/565	287/549	11.02			28.7	4210	2240		2.0	
228	88Pb 10Sn 2Ag	299/570	267/513	10.75	8.5	0.27	29.1	3260		42		
6	92.86Pb 4.76In 2.38Ag	300/572	300/572	11.03	5.5	0.25	25	4560	2830			
159	90Pb 10Sn	302/576	275/527	10.50	8.2	0.36	27.9	4400	2400	30	2.76	10
165	97.5Pb 1.5Ag 1Sn	309/588	309/588	11.28	6.0	0.23	30.4	4420		23		9.5
164	92.5Pb 5In 2.5Ag	310/590	300/572	11.02	5.5	0.25	25	4560	2830			
12	90Pb 5In 5Ag	310/590	290/554	11.00	5.5 - 5.6	0.25	27	5730	3180	23		9.0
171	95Pb 5Sn	312/594	308/586	10.80	8.1	0.35	28.4	4000	2100	45		8.0**
11	95Pb 5In	313/595	300/572	11.06	5.11	0.21	29	4330	3220	52		6.0**
183	88Au 12Ge	356/673	356/673	14.67		0.44	13.35	26825	26825		10.55	
184	96.76Au 3.24Si	363/685	363/685	15.40		0.27	12.33	36975	31900		12.04	
229	94.5Pb 5.5Ag	365/	304/579	11.28	6.0	0.23	30.4	4420				
200	100Au	1063/ 1945	1063/ 1945	19.30			14.4	18000 - 20000		39 - 45 (2 in.)	2.2	

Note: Unless otherwise indicated, all values are those at room temperature (20°C).

* Indicates values which vary significantly among ...

Technical Data

Liquidus °C/°F	Solidus °C/°F	Indalloy® Number	Composition	Plastic Range °C/°F	Mass Density (gm/cm³)	Electrical Cond. % of Cu	Thermal Cond. W/Cm°C @ 85°C	Thermal Coefficient of Expansion µ in/in/°C @ 20°C
47/117	47/117	117	44.7Bi 22.6Pb 19.1In 8.3Sn 5.3Cd	Eutectic	9.16	~4.50	0.15	25.0
58/136	58/136	136	49Bi 21In 18Pb 12Sn	Eutectic	9.01	2.43	0.10	23.0
70/158	70/158	158	50Bi 26.7Pb 13.3Sn 10Cd	Eutectic	9.58	~4.20	0.18	22.0
93/199	93/199	8	44In 42Sn 14Cd	Eutectic	7.46	—	0.36	24.0
100/212	100/212	42	46Bi 34Sn 20Pb	Eutectic	8.99	—	—	—
118/244	118/244	1E	52In 48Sn	Eutectic	7.30	11.70	0.34	20.0
124/255	124/255	255	55.5Bi 44.5Pb	Eutectic	10.44	~4.00	~0.04	—
138/281	138/281	281	58Bi 42Sn	Eutectic	8.56	5.00	—	15.0
143/290	143/290	290	97In 3Ag	Eutectic	7.38	23.00	0.73	22.0
145/293	145/293	181	51.2Sn 30.6Pb 18.2Cd	Eutectic	8.45	—	0.35	24.4
154/300	149/288	2	80In 15Pb 5Ag	5/12	7.85	13.00	0.43	28.0
163/325	144/291	97	43Pb 43Sn 14Bi	19/34	8.99	—	—	—
157/315	—	4	100In	Melting Point	7.31	24.00	0.86	29.0
167/333	154/309	9	70Sn 18Pb 12In	13/24	7.79	12.20	0.45	24.0
175/347	165/329	204	70In 30Pb	10/18	8.19	8.80	0.38	28.0
179/354	179/354	104	62.5Sn 36.1Pb 1.4Ag	Eutectic	8.41	11.90	0.50	27.0
179/354	179/354	62/36/2	62Sn 36Pb 2Ag	Eutectic	8.41	11.90	0.50	27.0
181/358	173/343	205	60In 40Pb	8/15	8.52	7.00	0.29	27.0
183/361	183/361	106	63Sn 37Pb	Eutectic	8.40	11.50	0.50	25.0
187/369	181/358	226†	83.6Sn 8.8In 7.6Zn	6/11	7.27	—	—	—
187/369	175/347	227†	77.2Sn 20In 2.8Ag	12/22	7.25	9.80	0.54	28.0
199/390	199/390	201	91Sn 9Zn	Eutectic	7.27	—	0.61	—
210/410	184/363	7	50In 50Pb	26/47	8.86	6.00	0.22	27.0
221/430	221/430	121	96.5Sn 3.5Ag	Eutectic	7.36	16.00	0.33	30.2
231/448	197/387	206	60Pb 40In	34/61	9.30	5.20	0.19	26.0
237/459	143/289	3	90In 10Ag	94/170	7.54	22.10	0.67	15.0
232/450	—	128	100Sn	Melting Point	7.28	15.60	0.73	23.5
240/464	235/455	133	95Sn 5Sb	5/9	7.25	11.90	0.28	31.1
260/500	240/464	10	75Pb 25In	20/36	9.97	4.60	0.18	26.0
275/527	260/500	150	81Pb 19In	15/27	10.27	4.50	0.17	27.0
296/565	287/549	151	92.5Pb 5Sn 2.5Ag	9/16	11.02	—	—	28.7
309/588	309/588	165	97.5Pb 1.5Ag 1Sn	Eutectic	11.28	6.00	0.23	30.4
310/590	300/572	164	92.5Pb 5In 2.5Ag	10/18	11.02	5.50	0.25	25.0
312/594	308/586	171	95Pb 5Sn	4/8	11.06	8.80	0.23	29.8

† Patented

Tensile Strength PSI	Bond Holding Strength (Shear) PSI	WIRE AND RIBBON RESEARCH SOLDER KITS						SOLDER PASTE RESEARCH SOLDER KITS		
		Lead Free Wire	Low Temperature Wire	Special Joining/ Bonding Wire	Microelectronics Wire	General Purpose Wire	General Purpose Ribbon	Custom Paste Kit Choose 5	No-Clean Paste Kit	Water Soluble Paste Kit
5400	—		■							
6300	—		■	■						
5990	—		■							
2632	—			■		■				
—	—		■					■		
1720	1630	■	■	■		■	■	■		
6400	—		■							
8000	500	■	■					■	■	■
800	—	■		■	■		■	■		
6263	—					■				
2550	2150		■	■	■	■	■	■		
—	—							■		
273	890	■		■	■		■			
5320	4190					■				
3450	—				■	■		■		
6380	7540					■	■			
6380	7540							■		
4150	—				■		■	■		
7500	6200					■	■	■	■	■
6600	—	■								
6800	4800	■								
7940	—	■				■				
4670	2680			■	■	■		■		
5620	—	■				■	■	■	■	■
5000	—				■			■		
1650	1600	■		■						
1900	—							■		
5900	—	■				■		■		
5450	3520			■	■	■				
5550	—				■	■	■			
4210	2240							■		
4420	—					■	■			
4560	2830			■	■	■	■	■		
4000	2100					■	■			

ALLOY, PARTICLE SIZE & METAL LOAD SELECTOR

Low, Medium and High Temperature Alloys allow you to experiment with a number of alloys within a given temperature range, or across two or three ranges for applications such as step-soldering (100°C to 310°C).

Please note some of these alloys are indium-containing, some are lead-free and some are both.

Lead-Free Alloys, indicated by a ▲ for quick reference in the Alloy Selector Chart, should be evaluated for suitability in lead reduction programs. The alloys available in the kit were chosen due to their popularity in a wide range of applications. Some of these alloys contain indium as indicated by the ● under the Indalloy heading in the chart.

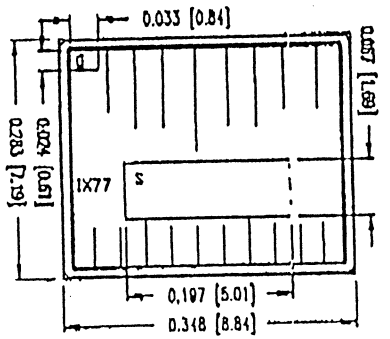
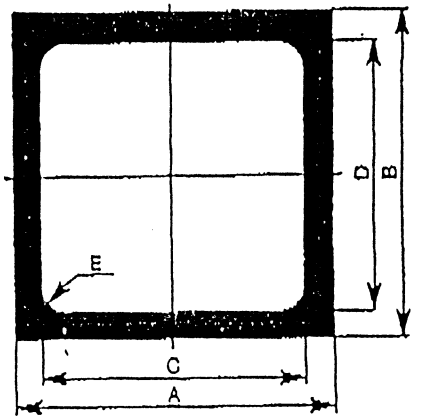
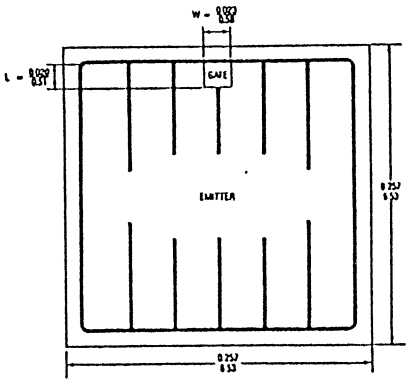
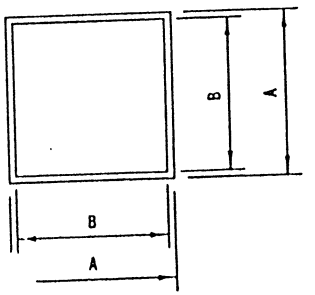
Shelf Life: We recommend storing the paste between 0°C and 21°C for a shelf life of up to six months. Pastes should be brought to ambient temperature before using.

	Indalloy® No. ● Indium Alloy ▲ Lead Free Alloy	Composition	Liquidus °C	Solidus °C	✔ 5 Alloys	✔ Particle Size		✔ Metal Load for		
						-200/+325 (44-74 Microns)	-325/+500 (25-44 Microns)	Disp† 85%	Scrn‡ 88%	Sten‡ 90%
LOW TEMPERATURE	**42**	46Bi 34Sn 20Pb	100	100						
	1E ●▲	52In 48Sn	118	118						
	281 ▲	58Bi 42Sn	138	138						
	290 ●▲	97In 3Ag	143	143						
	2 ●	80In 15Pb 5Ag	154	149						
	97	43Pb 43Sn 14Bi	163	144						
	204 ●	70In 30Pb	175	165						
MEDIUM	**62/36/2**	62Sn 36Pb 2Ag	179	179						
	205 ●	60In 40Pb	181	173						
	106	63Sn 37Pb	183	183						
	7 ●	50In 50Pb	210	184						
	121 ▲	96.5Sn 3.5Ag	221	221						
HIGH	**206 ●**	60Pb 40In	231	197						
	128 ▲	100Sn	232	MP						
	133 ▲	95Sn 5Sb	240	235						
	151	92.5Pb 5Sn 2.5Ag	296	287						
	164 ●	92.5Pb 5In 2.5Ag	310	300						

For technical specifications on any of these solders, please refer to the table on pages 16 and 17.

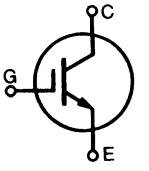
† For dispensing applications, paste will be packed in two syringes per alloy each containing 25 grams for a total of 250 gms. When placing your order, please indicate your choice of manual thumb plunger or piston for air assisted dispensing.

‡ For screening and stenciling applications, paste will be packed in plastic jars of 100 grams each for a total of 500 gms.

	IGBT	Diode
IXYS	283mils x 348mils  IXGD 40N60A (40A/600V) 348X283 mil	 C-DWEP 55-06A (55A/600V) 341X195 mil
IR	 IRGDCC50S (40A/600V) 257X257 mil	 IR210LR-BS02/600 (40A/600V) 210X190 mil 210

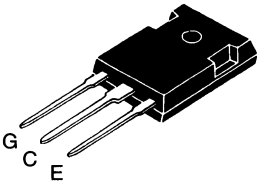
IXYS

		V_{CES}	I_{C25}	$V_{CE(sat)}$
Low $V_{CE(sat)}$ IGBT	**IXGH/IXGM 40 N60**	**600 V**	**75 A**	**2.5 V**
High speed IGBT	**IXGH/IXGM 40 N60A**	**600 V**	**75 A**	**3.0 V**

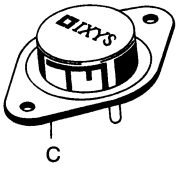


Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C, limited by leads	75	A
I_{C90}	T_C = 90°C	40	A
I_{CM}	T_C = 25°C, 1 ms	150	A
SSOA (RBSOA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 22 Ω Clamped inductive load, L = 30 µH	I_{CM} = 80 @ 0.8 V_{CES}	A
P_C	T_C = 25°C	250	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque (M3)	1.13/10	Nm/lb.in.
Weight		TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD (IXGH)



TO-204 AE (IXGM)



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{CES}	I_C = 250 µA, V_{GE} = 0 V		600			V
$V_{GE(th)}$	I_C = 250 µA, V_{CE} = V_{GE}		2.5		5	V
I_{CES}	V_{CE} = 0.8 • V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 125°C			200 1	µA mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	I_C = I_{C90}, V_{GE} = 15 V	40N60 40N60A			2.5 3.0	V V

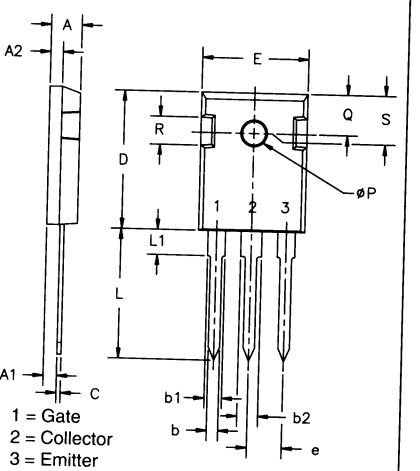
Features
- International standard packages
- 2nd generation HDMOS™ process
- Low $V_{CE(sat)}$
  - for low on-state conduction losses
- High current handling capability
- MOS Gate turn-on
  - drive simplicity
- Voltage rating guaranteed at high temperature (125°C)

Applications
- AC motor speed control
- DC servo and robot drives
- DC choppers
- Uninterruptible power supplies (UPS)
- Switch-mode and resonant-mode power supplies

Advantages
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- High power density

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	$I_C = I_{C90}$; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %		25	35		S
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz			4500		pF
C_{oes}				300		pF
C_{res}				60		pF
Q_g	$I_C = I_{C90}$, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}			200	250	nC
Q_{ge}				45	80	nC
Q_{gc}				88	120	nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**			100		ns
t_{ri}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH			200		ns
$t_{d(off)}$	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 22 Ω			600		ns
t_{fi}	Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G	40N60A		200		ns
E_{off}		40N60A		3		mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**			100		ns
t_{ri}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH			200		ns
E_{on}	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 22 Ω			4		mJ
$t_{d(off)}$				600	1000	ns
t_{fi}	Remarks: Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G	40N60		600	2000	ns
		40N60A		300	800	ns
E_{off}		40N60		12		mJ
		40N60A		6		mJ
R_{thJC}					0.5	K/W
R_{thCK}				0.25		K/W

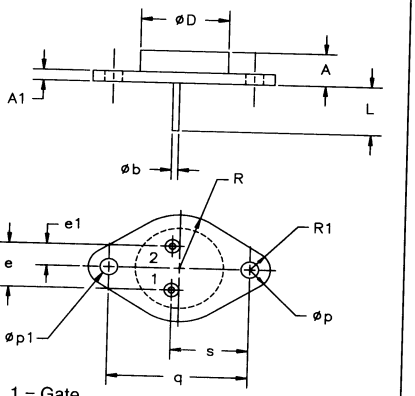
TO-247 AD Outline



1 = Gate
2 = Collector
3 = Emitter
Tab = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A_1	.087	.102	2.2	2.54
A_2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b_1	.065	.084	1.65	2.13
b_2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
øP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

TO-204AE Outline



1 = Gate
2 = Emitter
Case = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.250	.450	6.4	11.4
A1	.060	.135	1.53	3.42
øb	.057	.063	1.45	1.60
øD		.875		22.22
e	.420	.440	10.67	11.17
e1	.205	.225	5.21	5.71
L	.440	.480	11.18	12.19
øp	.151	.165	3.84	4.19
øp1	.151	.165	3.84	4.19
q	1.187 BSC		30.15 BSC	
R	.495	.525	12.58	13.33
R1	.131	.188	3.33	4.77
s	.655	.675	16.64	17.14

Fig. 1 Saturation Characteristics

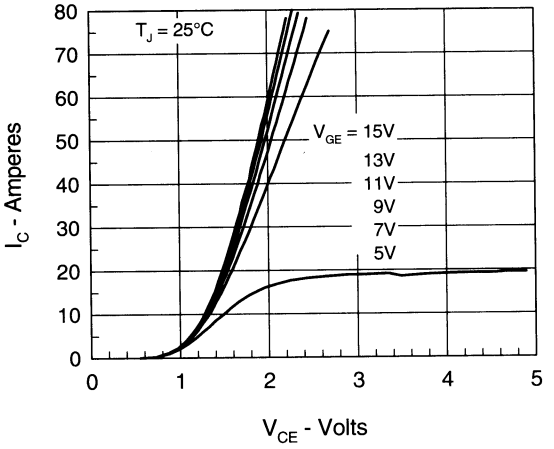


Fig. 2 Output Characterstics

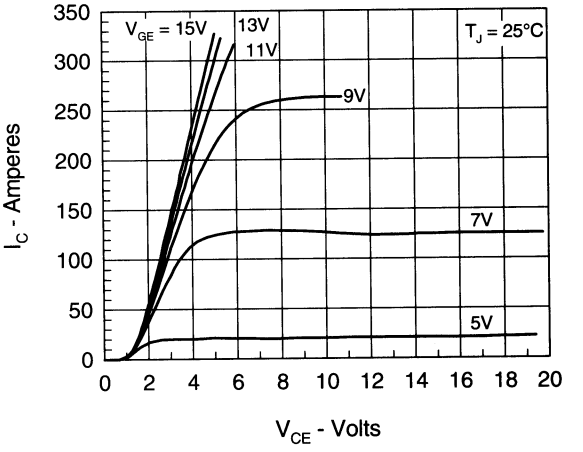


Fig. 3 Collector-Emitter Voltage vs. Gate-Emitter Voltage

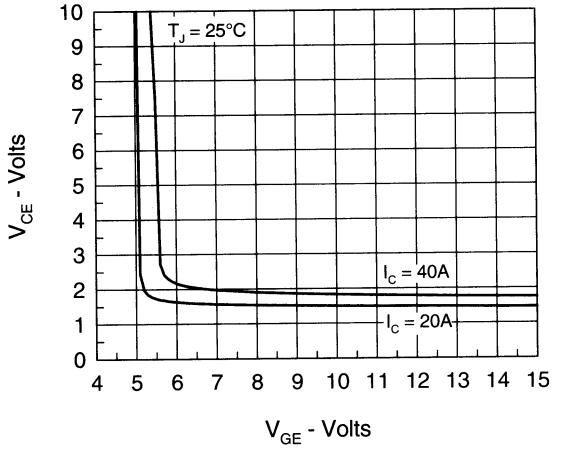


Fig. 4 Temperature Dependence of Output Saturation Voltage

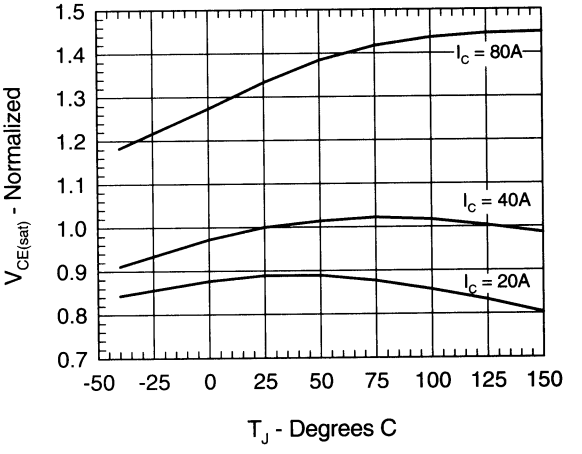


Fig. 5 Input Admittance

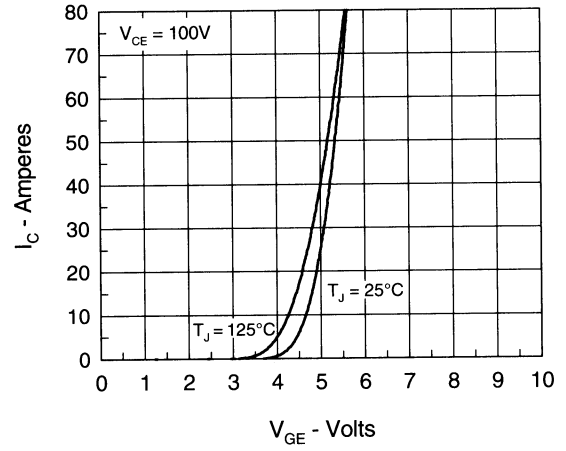


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

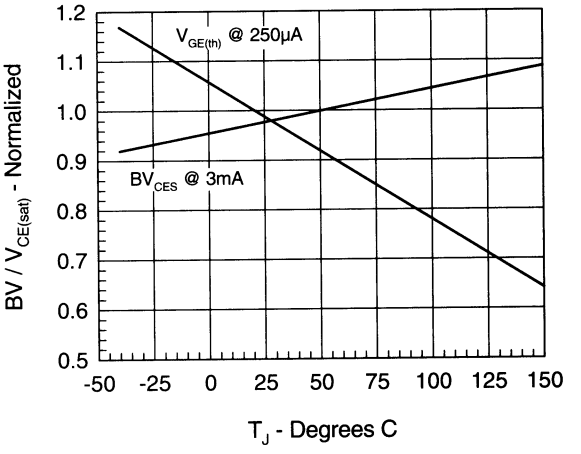


Fig.7 Gate Charge

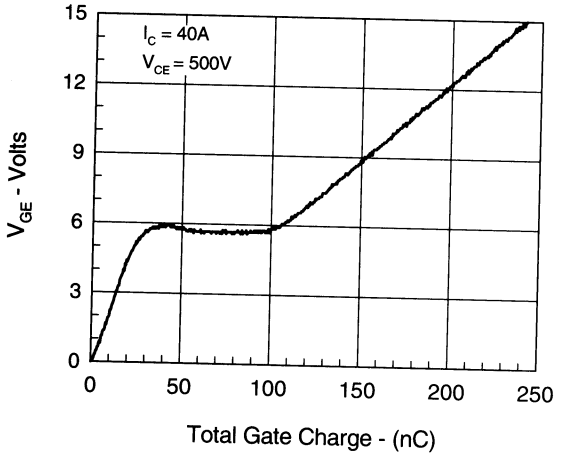


Fig.8 Turn-Off Safe Operating Area

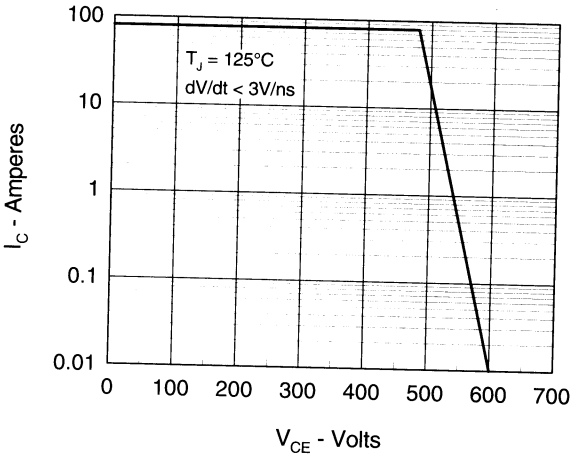


Fig.9 Capacitance Curves

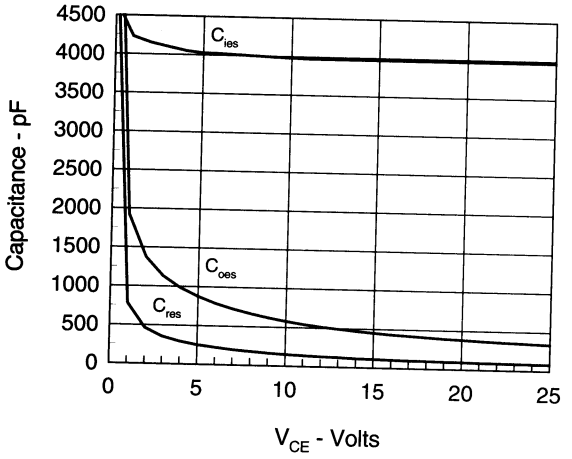
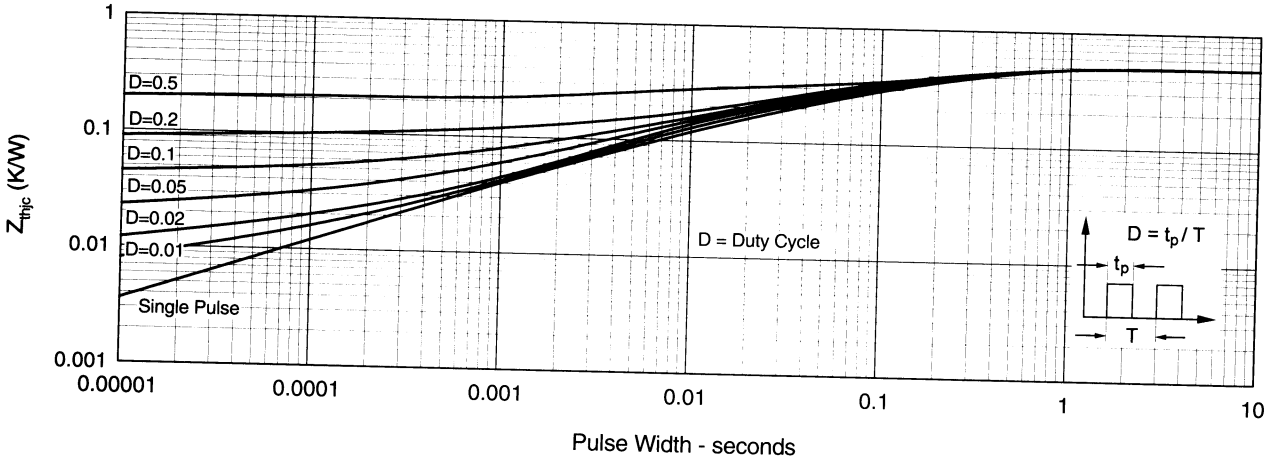


Fig.10 Transient Thermal Impedance

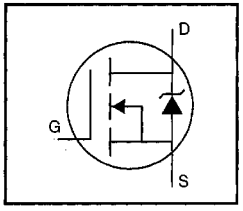


International IOR Rectifier

IRF730

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 400V

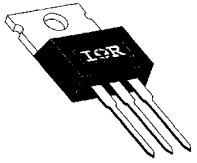
$R_{DS(on)}$ = 1.0Ω

I_D = 5.5A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

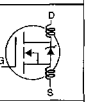
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	5.5	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	3.5	
I_{DM}	Pulsed Drain Current ①	22	
P_D @ T_C = 25°C	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	290	mJ
I_{AR}	Avalanche Current ①	5.5	A
E_{AR}	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

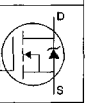
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.54	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.0	Ω	V_{GS}=10V, I_D=3.3A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	2.9	—	—	S	V_{DS}=50V, I_D=3.3A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=400V, V_{GS}=0V
		—	—	250		V_{DS}=320V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	38	nC	I_D=3.5A
Q_{gs}	Gate-to-Source Charge	—	—	5.7		V_{DS}=320V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	22		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	V_{DD}=200V
t_r	Rise Time	—	15	—		I_D=3.5A
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		R_G=12Ω
t_f	Fall Time	—	14	—		R_D=57Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	700	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	170	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	64	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	22		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J=25°C, I_S=5.5A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	270	530	ns	T_J=25°C, I_F=3.5A
Q_{rr}	Reverse Recovery Charge	—	1.8	2.2	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=16mH R_G=25Ω, I_{AS}=5.5A (See Figure 12)

③ I_{SD}≤5.5A, di/dt≤90A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

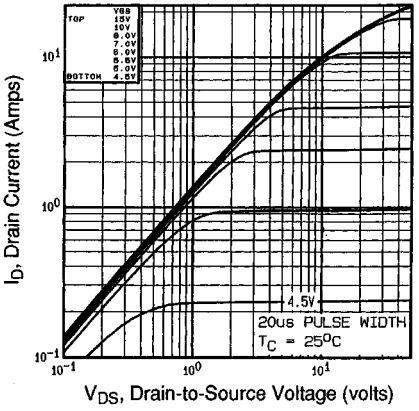


Fig 1. Typical Output Characteristics, T_C=25°C

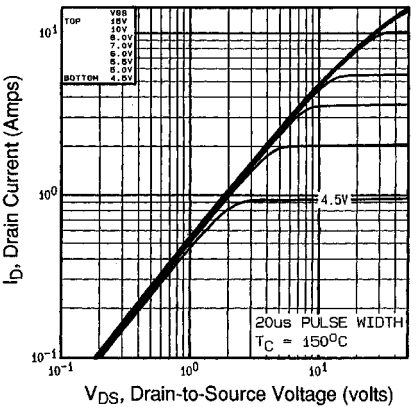


Fig 2. Typical Output Characteristics, T_C=150°C

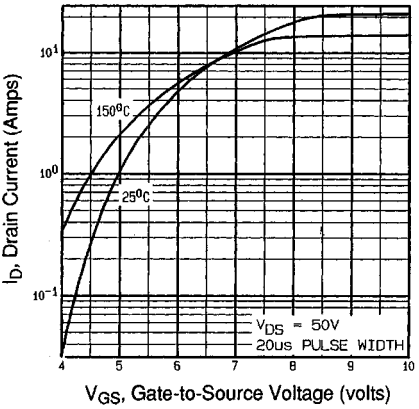


Fig 3. Typical Transfer Characteristics

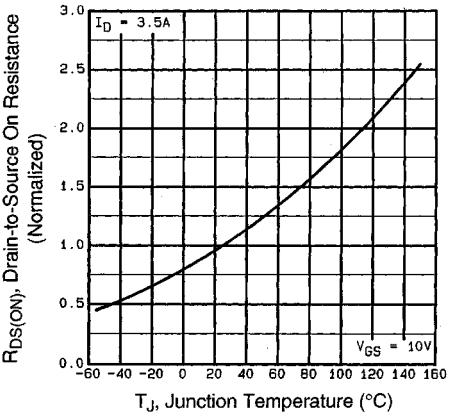


Fig 4. Normalized On-Resistance Vs. Temperature

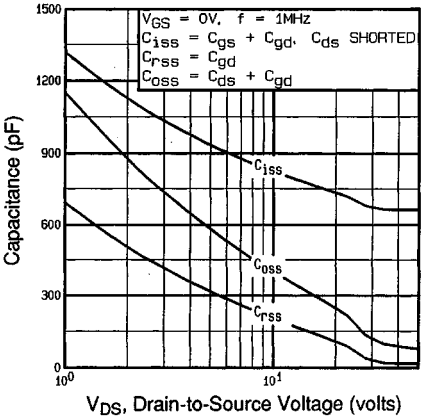


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

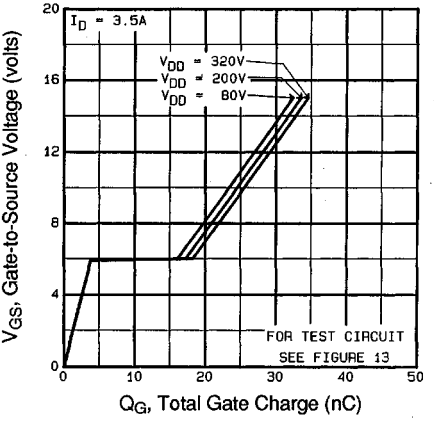


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

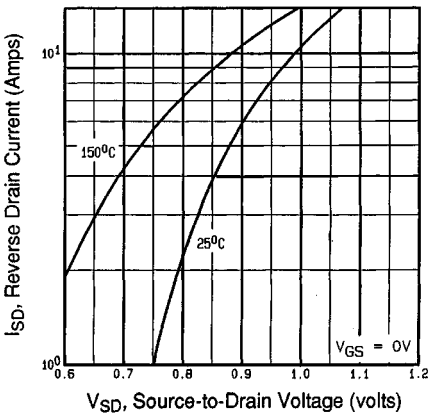


Fig 7. Typical Source-Drain Diode Forward Voltage

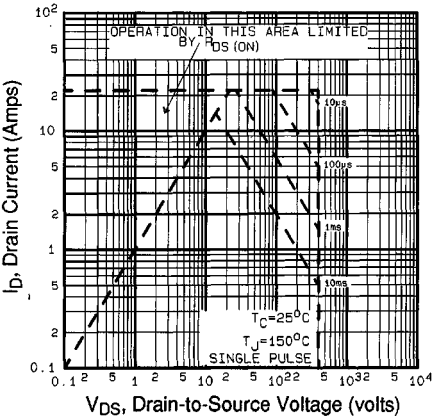


Fig 8. Maximum Safe Operating Area

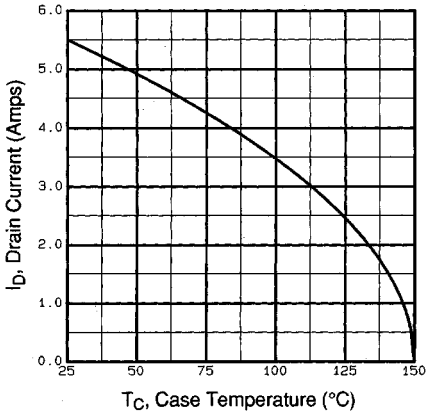


Fig 9. Maximum Drain Current Vs. Case Temperature

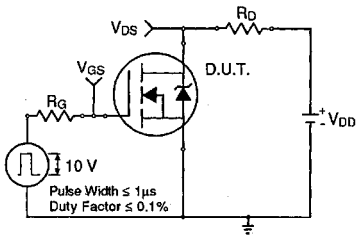


Fig 10a. Switching Time Test Circuit

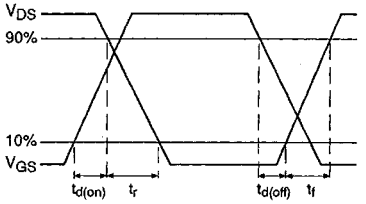


Fig 10b. Switching Time Waveforms

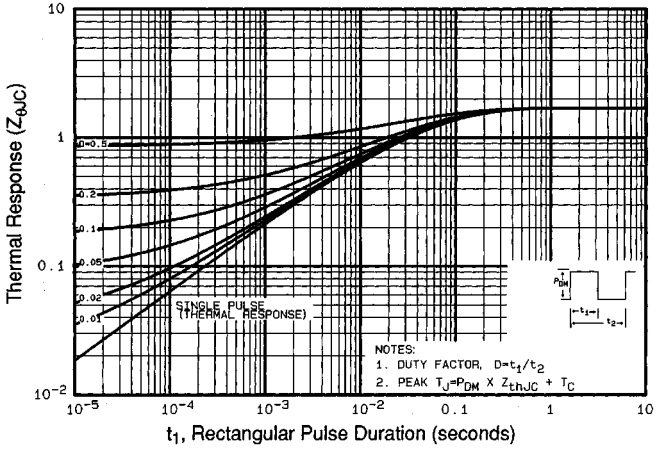


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

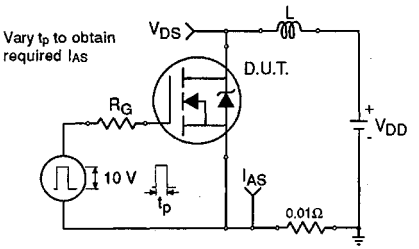


Fig 12a. Unclamped Inductive Test Circuit

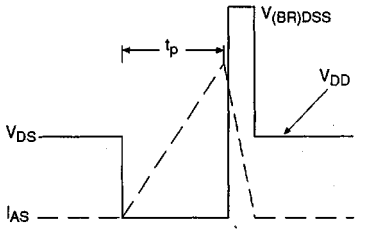


Fig 12b. Unclamped Inductive Waveforms

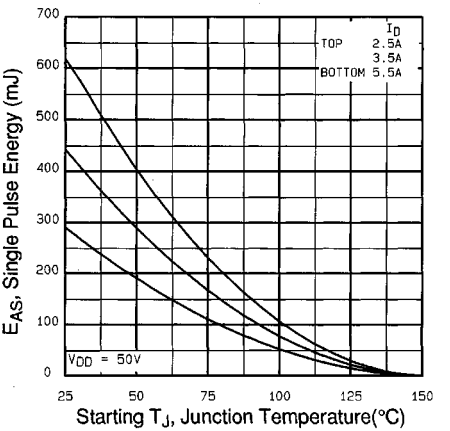


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

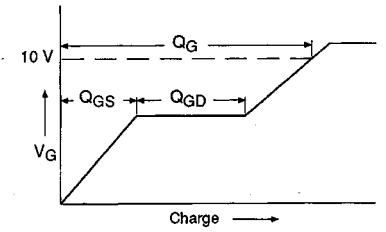


Fig 13a. Basic Gate Charge Waveform

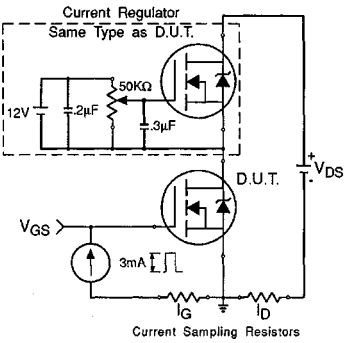


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International IOR Rectifier

IR2155

SELF-OSCILLATING HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Undervoltage lockout
- Programmable oscillator frequency

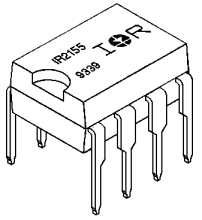
$$f = \frac{1}{1.4 \times (R_T + 150\Omega) \times C_T}$$

- Matched propagation delay for both channels
- Micropower supply startup current of 125 µA typ.
- Low side output in phase with R_T

Product Summary

V_{OFFSET}	600V max.
Duty Cycle	50%
I_O+/-	210 mA / 420 mA
V_{OUT}	10 - 20V
Deadtime (typ.)	1.2 µs

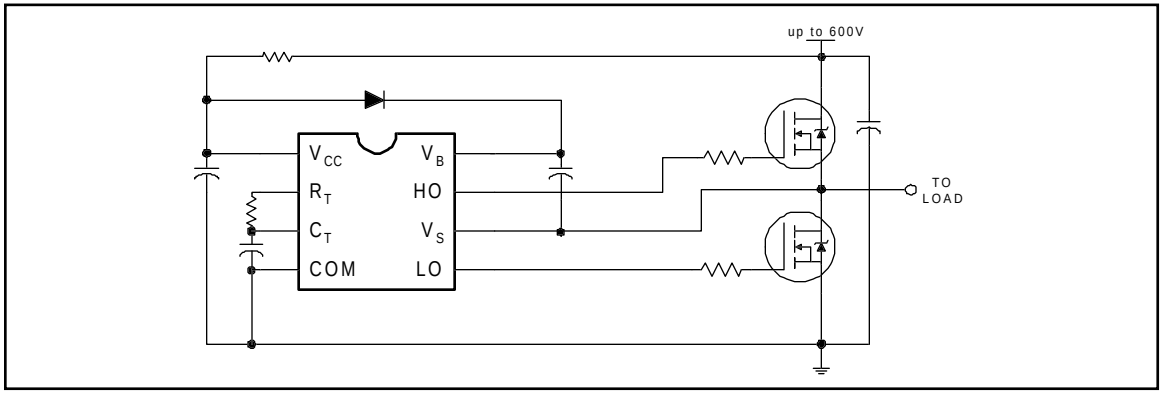
Package



Description

The IR2155 is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross-conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{RT}	R_T Voltage	-0.3	V_{CC} + 0.3	
V_{CT}	C_T Voltage	-0.3	V_{CC} + 0.3	
I_{CC}	Supply Current (Note 1)	—	25	mA
I_{RT}	R_T Output Current	-5	5	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	—	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
I_{CC}	Supply Current (Note 1)	—	5	mA
T_A	Ambient Temperature	-40	125	°C

Note 1: Because of the IR2155's application specificity toward off-line supply systems, this IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip V_{CC} and the rectified line voltage and a local decoupling capacitor from V_{CC} to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than V_{CLAMP}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

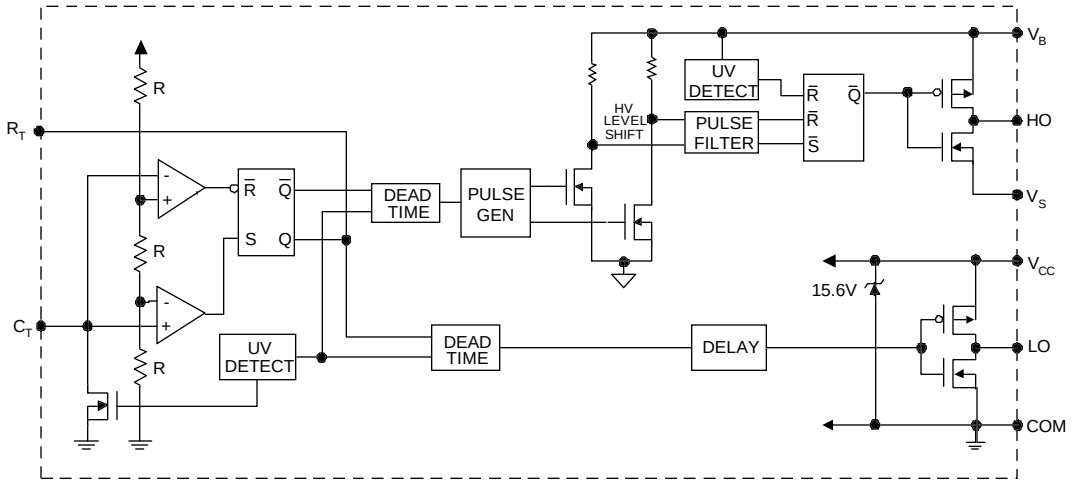
Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_r	Turn-On Rise Time	—	80	120	ns	
t_r	Turn-Off Fall Time	—	40	70		
DT	Deadtime	0.50	1.20	2.25	µs	
D	R_T Duty Cycle	48	50	52	%	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, C_L = 1000 pF, C_T = 1 nF and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f_{OSC}	Oscillator Frequency	19.4	20.0	20.6	kHz	R_T = 35.7 kΩ
		94	100	106		R_T = 7.04 kΩ
V_{CLAMP}	V_{CC} Zener Shunt Clamp Voltage	14.4	15.6	16.8	V	I_{CC} = 5 mA
V_{CT+}	2/3 V_{CC} Threshold	7.8	8.0	8.2		
V_{CT-}	1/3 V_{CC} Threshold	3.8	4.0	4.2		
V_{CTUV}	C_T Undervoltage Lockout	—	20	50	mV	2.5V < V_{CC} < V_{CCUV}
V_{RT+}	R_T High Level Output Voltage, V_{CC} - R_T	—	0	100		I_{RT} = -100 µA
		—	200	300		I_{RT} = -1 mA
V_{RT-}	R_T Low Level Output Voltage	—	20	50		I_{RT} = 100 µA
		—	200	300		I_{RT} = 1 mA
V_{RTUV}	RT Undervoltage Lockout, V_{CC} - R_T	—	0	100		2.5V < V_{CC} < V_{CCUV}
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	70	150		
I_{QBSUV}	Micropower V_{BS} Supply Startup Current	—	55	125		
I_{QCC}	Quiescent V_{CC} Supply Current	—	500	1000		
I_{QCCUV}	Micropower V_{CC} Supply Startup Current	—	70	150		
I_{CT}	C_T Input Current	—	0.001	1.0		
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	7.7	8.4	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.3	8.1	8.9		
V_{BSUVH}	V_{BS} Supply Undervoltage Lockout Hysteresis	100	400	—	mV	
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	7.7	8.4	9.2	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.4	8.1	8.9		
V_{CCUVH}	V_{CC} Supply Undervoltage Lockout Hysteresis	200	400	—	mV	
I_{O+}	Output High Short Circuit Pulsed Current	210	250	—	mA	V_O = 0V
I_{O-}	Output Low Short Circuit Pulsed Current	420	500	—		V_O = 15V

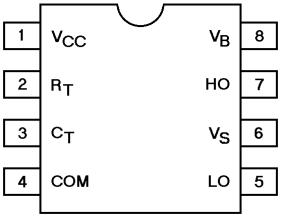
Functional Block Diagram



Lead Definitions

Lead Symbol	Description
R_T	Oscillator timing resistor input,in phase with LO for normal IC operation
C_T	Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 150\Omega) \times C_T}$ where 150Ω is the effective impedance of the R_T output stage
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

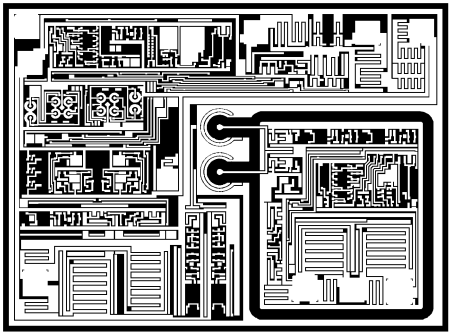
Lead Assignments



8 Lead DIP

IR2155

Device Information

Process & Design Rule		HVDCMOS 4.0 µm
Transistor Count		260
Die Size		88 X 92 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
First Layer	Width	4 µm
	Spacing	6 µm
	Thickness	5000Å
Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)
	Width	6 µm
	Spacing	9 µm
	Thickness	20,000Å
Contact Hole Dimension		8 µm X 8 µm
Insulation Layer	Material	PSG (SiO_2)
	Thickness	1.5 µm
Passivation	Material	PSG (SiO_2)
	Thickness	1.5 µm
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 Lead PDIP / SO-8
	Materials	EME6300 / MP150 / MP190
Remarks:		

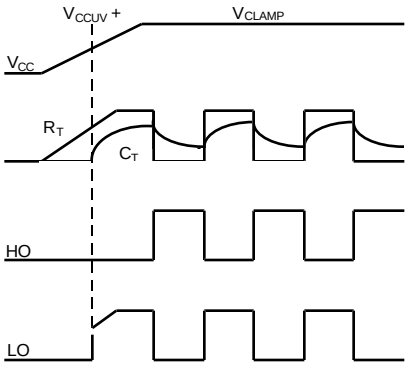


Figure 1. Input/Output Timing Diagram

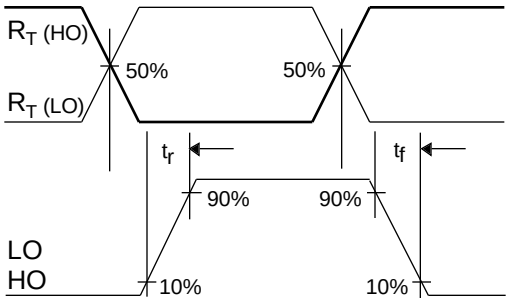


Figure 2. Switching Time Waveform Definitions

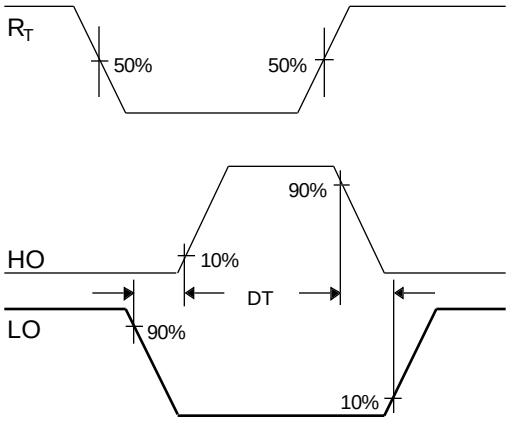


Figure 3. Deadtime Waveform Definitions

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Vita

Alex Lostetter was born in Roseburg, Oregon on August 27th, 1971. After living the first four years of his life in Scotland, his father left the military and his family settled down just outside of Fredericksburg, Virginia. Alex grew up in Stafford County, Virginia, where he learned to love the unique mixture of science and fiction. Writing became a passion, and dreaming a past-time.

In 1989, Alex started college at Virginia Polytechnic Institute and State University in the general engineering program. The next seven years were spent working full time (usually waiting tables) to pay his way through college. In whatever spare time he managed to scrape up, he enjoyed to continue to work creatively with his desire to paint, write, and sketch. Alex graduated from Virginia Tech in 1996 with a B.S. in Electrical Engineering.

The next four months were spent on the most exciting journey of his life. He and a friend packed their bags and made for Alaska, stopping at every cabin and brickhouse on the way there and back. As fun as it was, the journey finally came to an end though.

Alex returned to Virginia Tech where he went on to receive a Master of Science degree in Electrical Engineering in May, 1998. In that time, he was awarded an IMAPS Educational Foundation Research Grant and published a number of papers, including *High Density Power Modules: A Packaging Strategy* which was awarded Best Paper of

Session and Best Student Paper of Conference at the 30th International Symposium on Microelectronics in Philadelphia, 1997.

The next several years will be spent continuing to improve his professional standing by working with Lockheed-Martin, writing the fiction he so much loves, perhaps getting a taste of mountain climbing, and most of all… working towards the ultimate goal which sent him down this path to begin with. A desire to step into space.