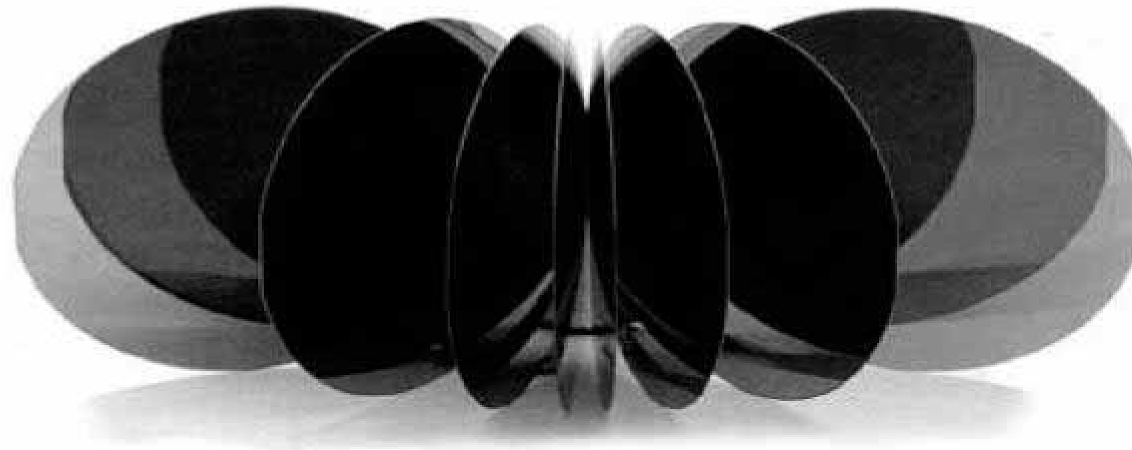
Lecture 2

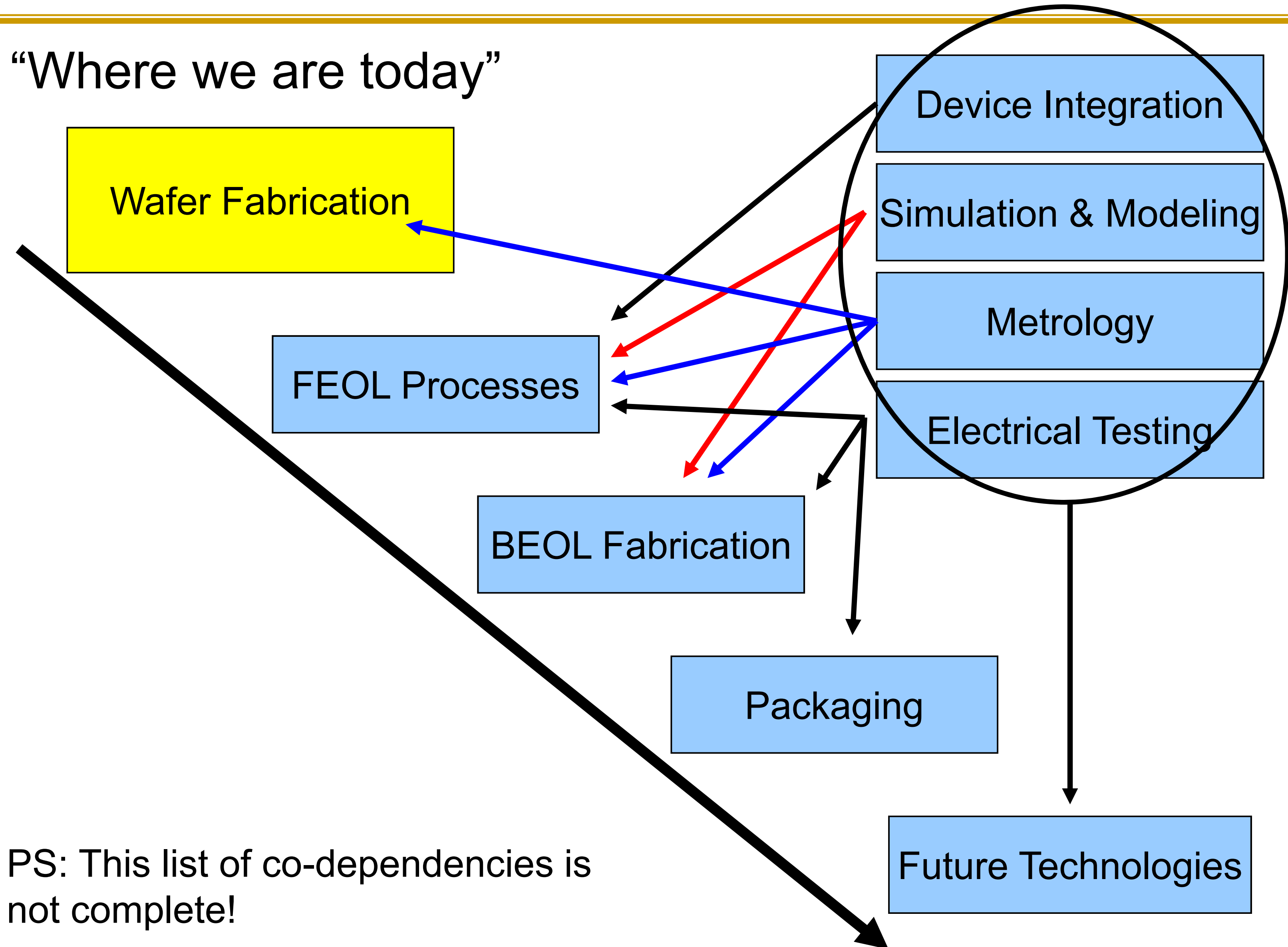
Wafer fabrication and Silicon epitaxy



Recap

- Introduction to IH2655
- Brief historic overview
- Moore's Law and the ITRS (International Technology Roadmap for Semiconductors)
- From Geometrical to Material-based scaling
- Process Flow: CMOS (Complementary Metal Oxide Semiconductor)

Lecture 2: Wafer Fabrication and Silicon Epitaxy



Outline

- The Silicon Crystal
- Silicon Wafer Fabrication
- Silicon Epitaxy

The Silicon Crystal

Silicon has a ***Diamond Cubic Lattice Structure***

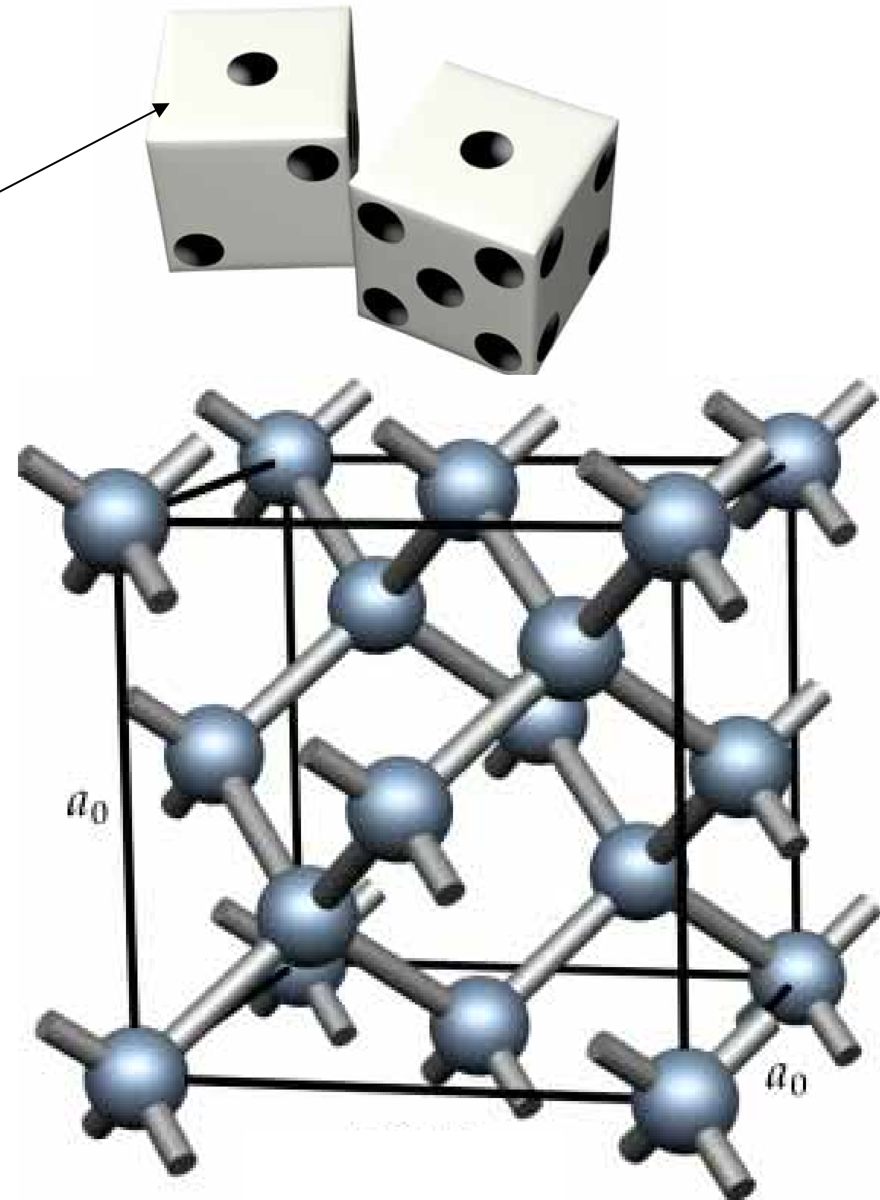
Two merged FCC lattices (Face Centered Cubic)

Shifted by ¼ of a_0 in each crystal direction

Bulk properties are isotropic

Number of surface atoms on the wafer depends on crystal plane

- Highest on Si {111}
- Lowest on Si {100}
- Influence on oxidation rate
- Influence on channel mobility…



The Silicon Crystal: Defects

0-D or Point defects :

- V vacancy (neutral, single- or double-charged, see further Plummer p133-138)
- I interstitial or interstitialcy

1-D defect: dislocation

2-D defect: Stacking fault

3-D defect: Precipitates

- e.g. oxygen precipitation

Surface defects

- e.g. dangling bonds

Defects are mobile

- Stress
- Diffusion

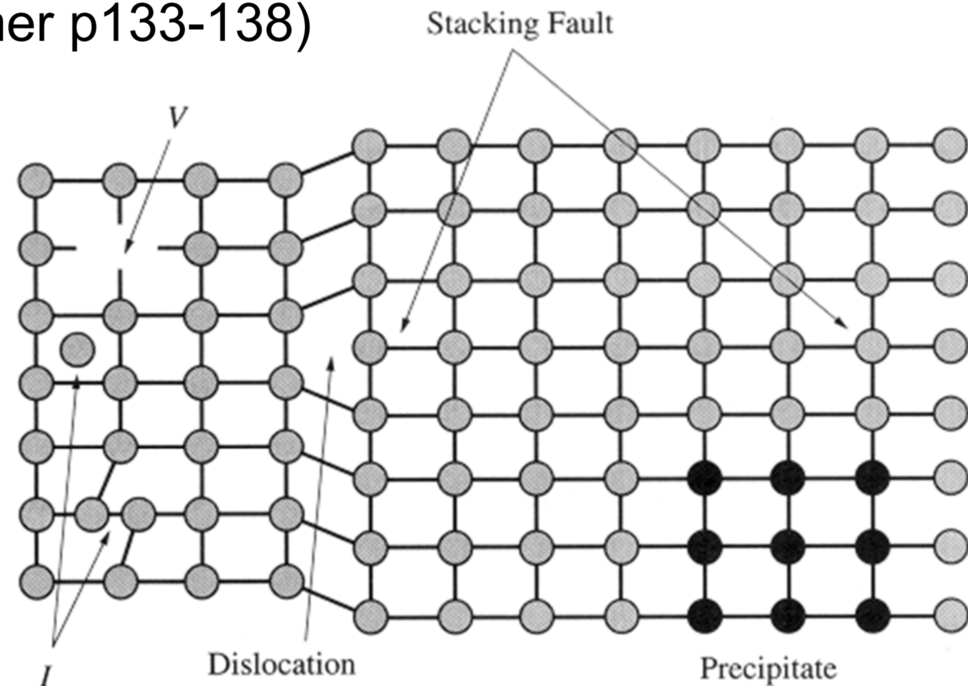


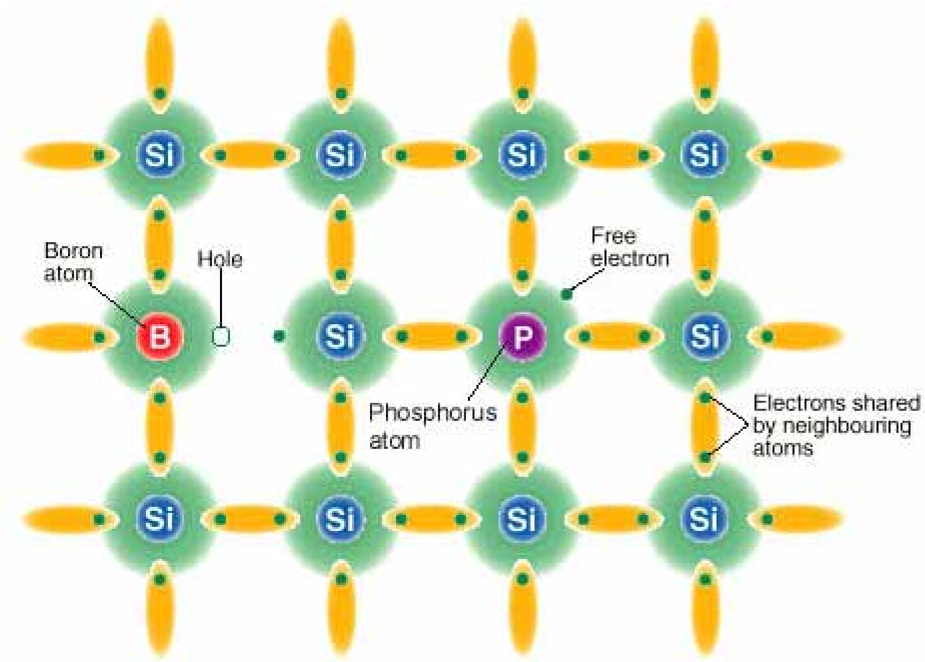
Figure 3–4 Simple 2D representation of some of the common defects found in crystals. *V* and *I* are point defects, the edge dislocation represents a typical line defect, the stacking fault is an area defect, and the precipitate is a volume defect.

(Plummer Fig. 3-4 p 98)

The Silicon Crystal: Doping

Doping: controlled substitution of lattice atoms

- n-type (electron donor)
- p-type (“hole donor”)



See Lecture 6 on diffusion and ion implantation

Outline

- The Silicon Crystal
- Silicon Wafer Fabrication
- Silicon Epitaxy

Silicon Wafer Fabrication

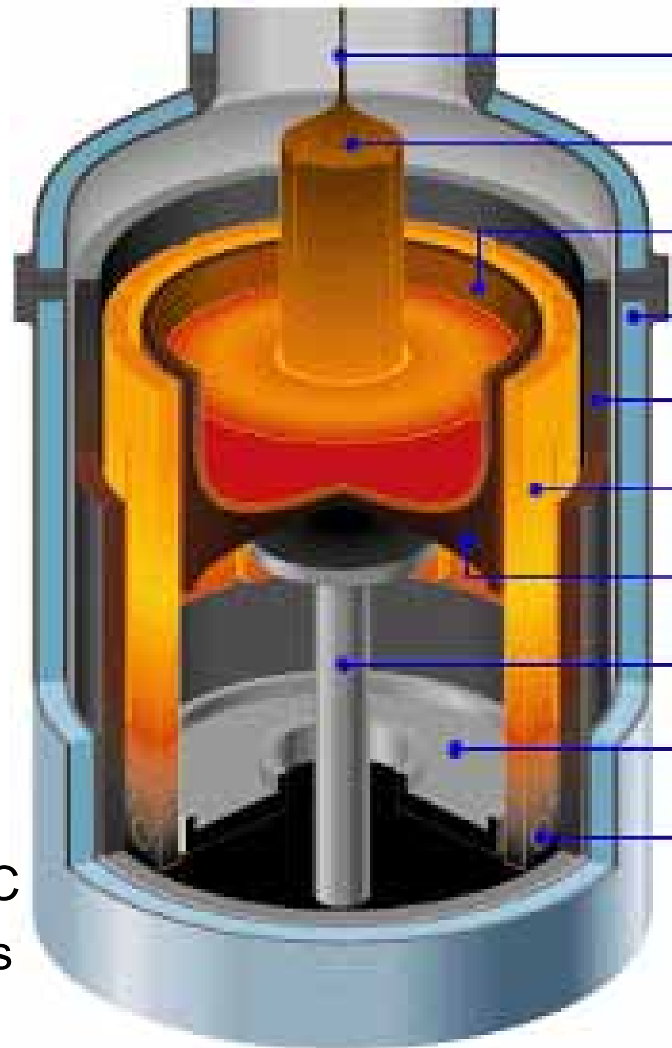
Goal: Single crystal silicon wafers

- Raw material: Quartzite (SiO2, sand), then refined to
- Metallurgical Grade Silicon (MGS)
  - Furnace with coal / coke and SiO_2 @ ~ 2000°C
  - Main reaction: 2 C (solid) + 2 SiO_2 (solid) → Si (liquid) + 2 CO
  - Significant power needed: ~ 13 kWh/kg
  - End result: 98% Silicon
- Electronic Grade Silicon (EGS)
  - MGS + HCl (gas) → SiH_4 (silane)
  - → $SiCl_4$ (silicon tetracloride)
  - → **$SiHCl_3$ (trichlorosilane)**…
  - Boiling purifies $SiHCl_3$
  - Chemical Vapor Deposition **(CVD)** on silicon rod (nucleation surface)
  - Reaction: 2 $SiHCl_3$ (gas) + 2 H_2 (gas) → 2 Si (solid) + 6 HCl (gas)
  - Resulting poly-crystalline silicon (polysilicon) has only part per billion (ppb) impurities (10^{13} – 10^{14} /cm^3)

Silicon Wafer Fabrication: Czochralski Method

Starting material:
electronic Grade Si (EGS)

Loading the high purity poly-Si



Si Melting point: ~1420°C

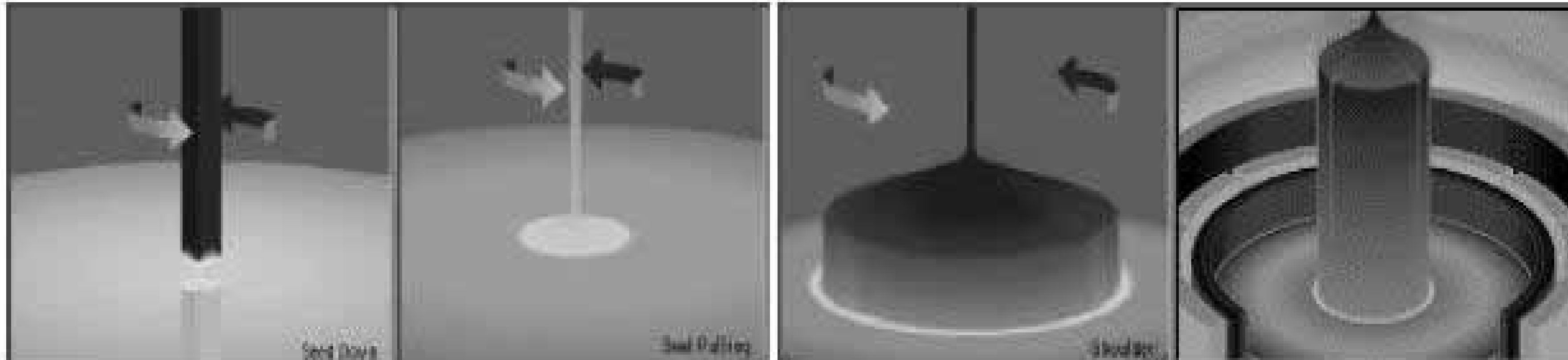
Pulling process: 1-3 days

Power: tens of kW

Silicon Ingot

Silicon Wafer Fabrication: Czochralski Method

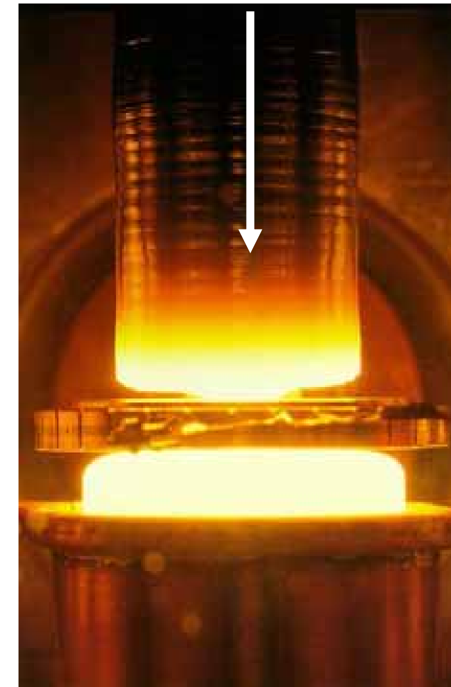
1-3 days



- Seed determines Silicon crystal orientation
- Dash method for moving dislocations to the surface at onset of pulling.
- Oxygen dissolves from quartz crucible; **impurity level: ~10^{18} cm^{-3} !**
  - Si-O-Si bindings resulting in higher mechanical strength (+)
  - Oxygen donors (SiO_4). 10^{16} cm^{-3} form at 400-500°C (-)
  - Bulk precipitation (SiO_2 clusters; can be controlled by gettering) (-)
- Carbon: from graphite susceptor and ESG, impurity level 10^{15}-10^{16} cm^{-3}

Silicon Wafer Fabrication: Float-Zone Method

- No crucible, crystal formed in Ar atmosphere
- RF coil induces large currents in Silicon → resistive heating → melting and recrystalization
- Low oxygen content (no crucible)
- High-resistivity possible
- Controlled doping:
  - Doped poly-silicon rod
  - Doped seed
  - Controlled gas ambient
- More difficult to scale up in wafer diameter
- Applications in power devices, detectors…



Silicon Wafer Fabrication: Czochralski Method

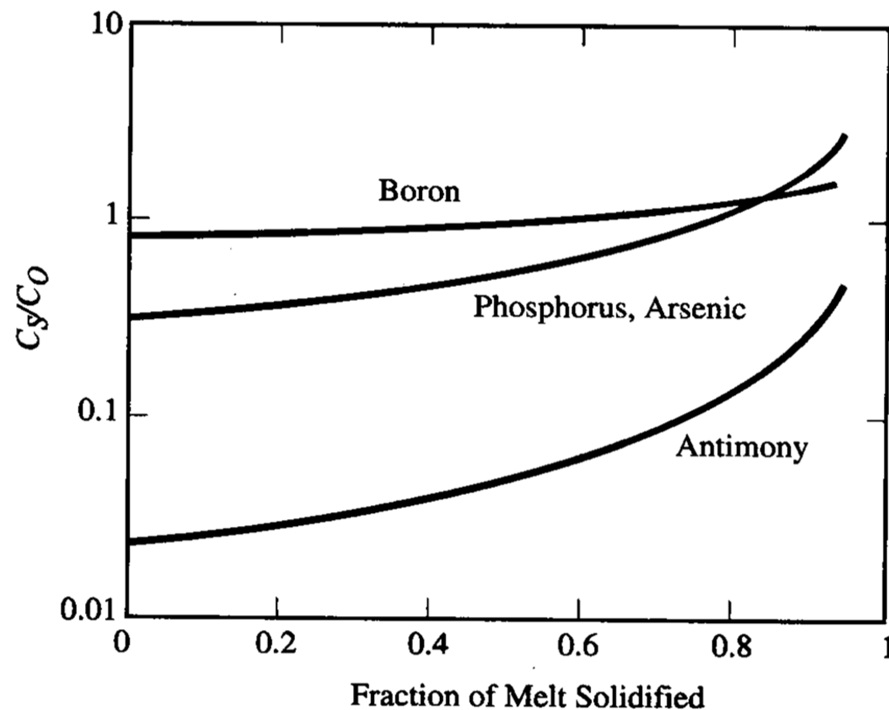
Doping

Dopant incorporation: Segregation coefficient $k_0 = C_{Solid}/C_{liquid}$

Typically $K_0 < 1$ → preference for liquid phase

CZ ingot doping concentration is a function of time, or position in the ingot

FZ process: dopants prefer to remain in the liquid float zone



(Plummer Fig. 3.18 p 128)

Silicon Wafer Fabrication: Wafer Shaping

- Single crystal ingot ground into uniform diameter (e.g. 300mm)
- Notch or Flat added
- Wafer Sawing
  - Slicing into wafers by an inner saw or a wire saw
- Wafer Lapping
  - Removes surface roughness from saw cuts and process damages
  - Mechanical lapping with alumina or silicon carbide abrasive
- Wafer Edge Rounding
- Wafer Etching
  - Mechanical damages induced during previous processes are removed by chemical etching
- Laser Scribing
- Wafer Polishing
  - Chemical-Mechanical Polishing (**CMP**) process yield flat surface using colloidal silica
- Wafer Cleaning and Inspection
  - Wafers are cleaned and inspected to be polished wafers

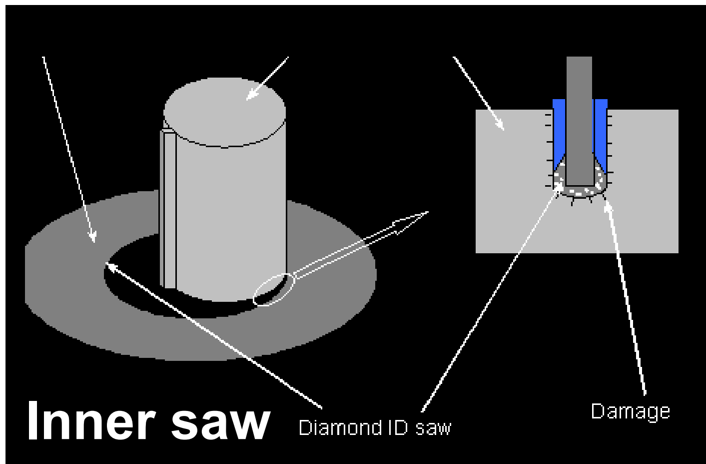
Silicon Ingot

http://product-category.com

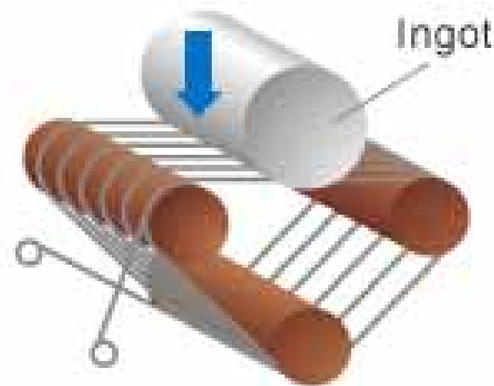
Silicon Wafer Fabrication: Wafer Shaping

- Single crystal ingot ground into uniform diameter (e.g. 300mm)
- Notch or Flat added
- Crystal orientation

- Wafer Sawing
- Slicing into wafers by an inner saw or a wire saw



http://serve.me.nus.edu.sg/nanomachining/wafer_preparation.htm



Structure of a wire saw machine

Wire saw machines

http://www.sumcosi.com/english/products/process/step_02.html

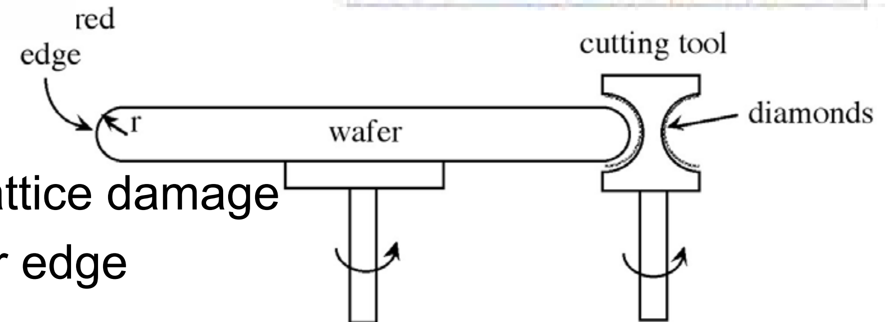
Silicon Wafer Fabrication: Wafer Shaping

http://www.sumcosi.com/english/products/process/step_02.html

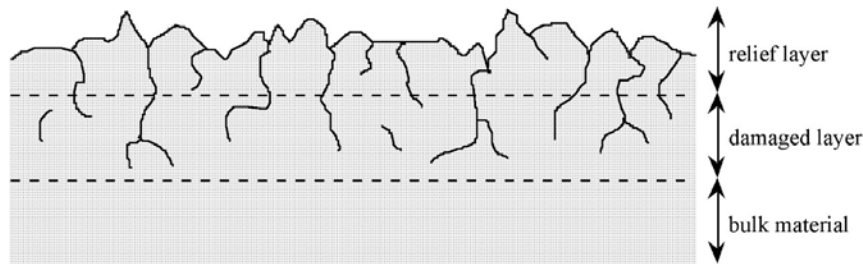
- Wafer Lapping
- Removes surface roughness from saw cuts and process damages
- Removes sub-surface damage from sawing → Lapping damage
- precise thickness uniformity, flatness and parallelism
- Mechanical lapping with alumina or silicon carbide abrasive

Lapping machine

- Wafer Edge Rounding
- Improved resistance to thermal stress
- Reducing particles, chip breakage and lattice damage
- Avoid build-up of photoresist at the wafer edge
- “Mechanical edge contouring”

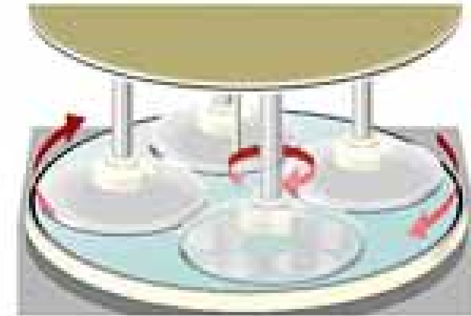


Silicon Wafer Fabrication: Wafer Shaping

- Laser Scribing
- Wafer Etching
- Mechanical damages induced during previous processes removed by chemical etching (Lecture 3)
- Wafer Polishing
- Chemical-Mechanical Polishing (**CMP**) process yield flat surface using colloidal silica
- 5 to 10 µm across the wafer diameter are typical flatness specifications
- cracks, ridges and valleys after lapping
- 

- Wafer Cleaning and Inspection
- Wafers are cleaned and inspected before
- shipping

http://www.sumcosi.com/english/products/process/step_02.html



Polisher

Silicon Wafer Fabrication: Gettering

Capture defects at locations far away from the device region.

Damaged region will act as "sink" for unwanted elements.

Metals diffuse as interstitials (>> diffusivity than dopants)

Metals need defects to become trapped:

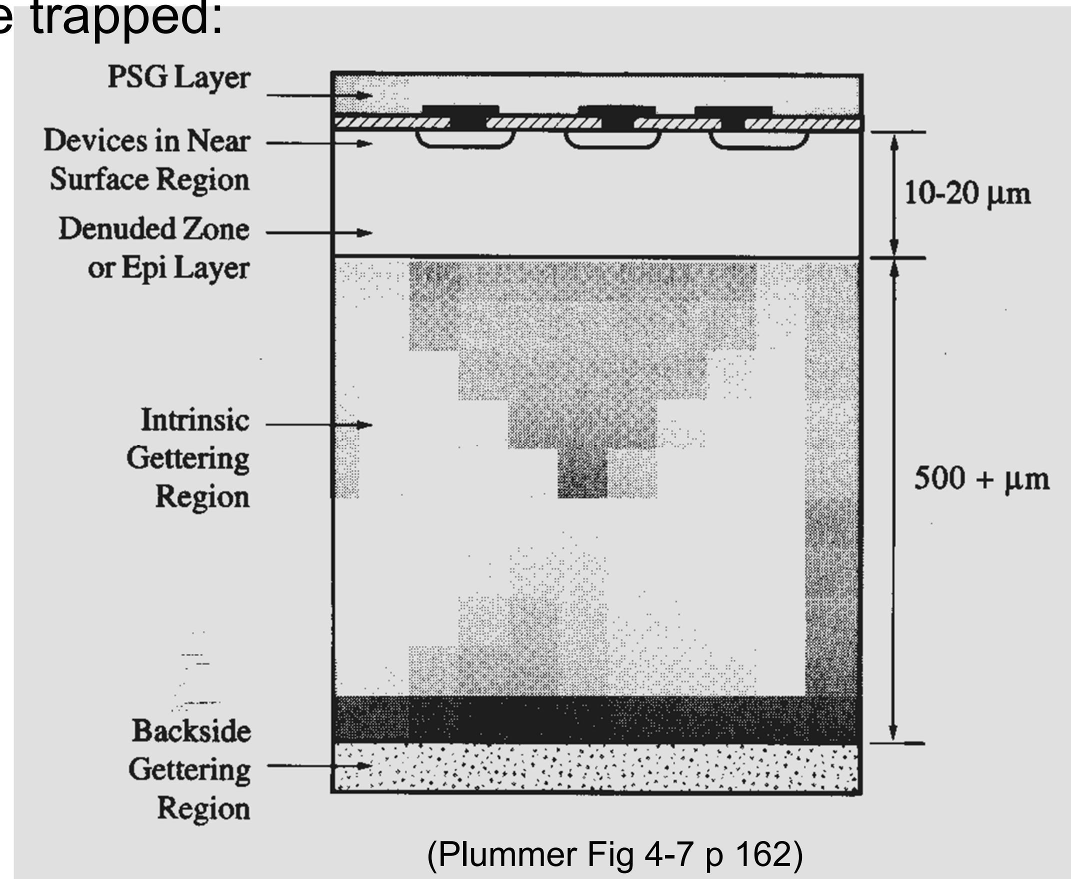
- Dislocations
- Stacking faults
- Grain boundaries
- Precipitates (e.g. O_2)

PSG captures alkali ions

(Phosphosilicate Glas)

General Stategy

1. Free impurities
2. Diffuse to gettering site
3. Trap at gettering site



(Plummer Fig 4-7 p 162)

Silicon Wafer Fabrication: Gettering

Extrinsic **gettering:**

Treatment on backside of wafer, e.g. n^+doping

Deposition of poly silicon on back side

Intrinsic **gettering:**

Intentional SiO_2 precipitation inside bulk CZ silicon

Requires dedicated thermal cycling:

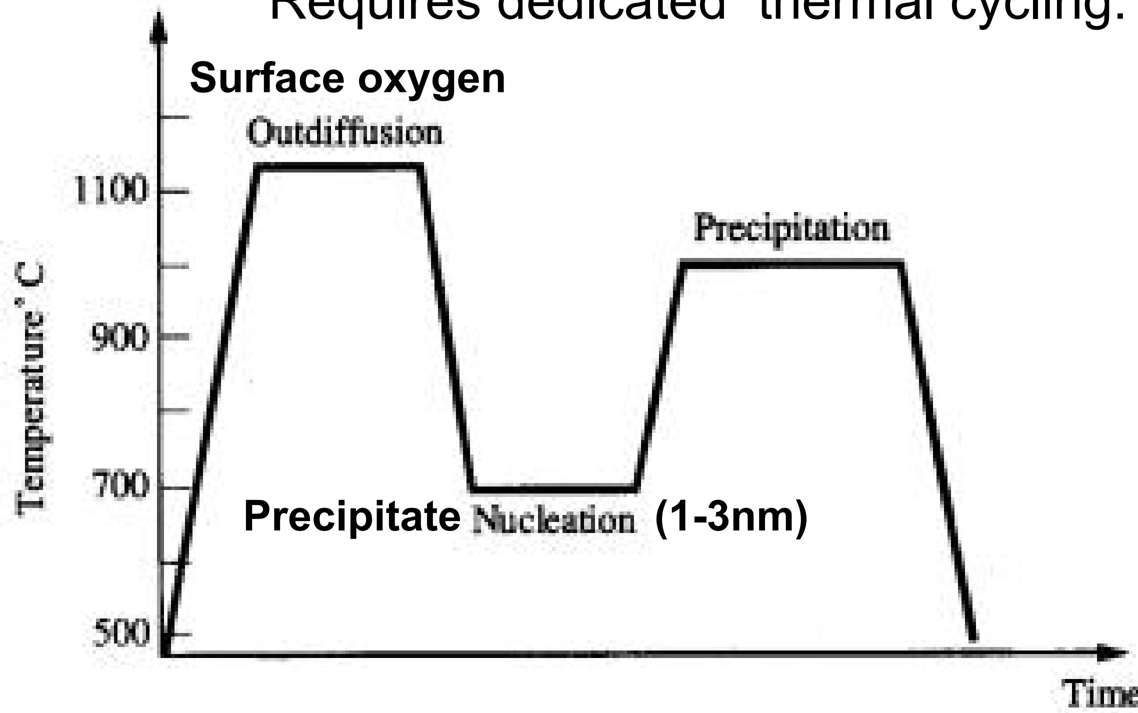


Figure 4–12 Processes and time/temperature cycle for a typical intrinsic gettering process.

(Plummer Fig 4-12)

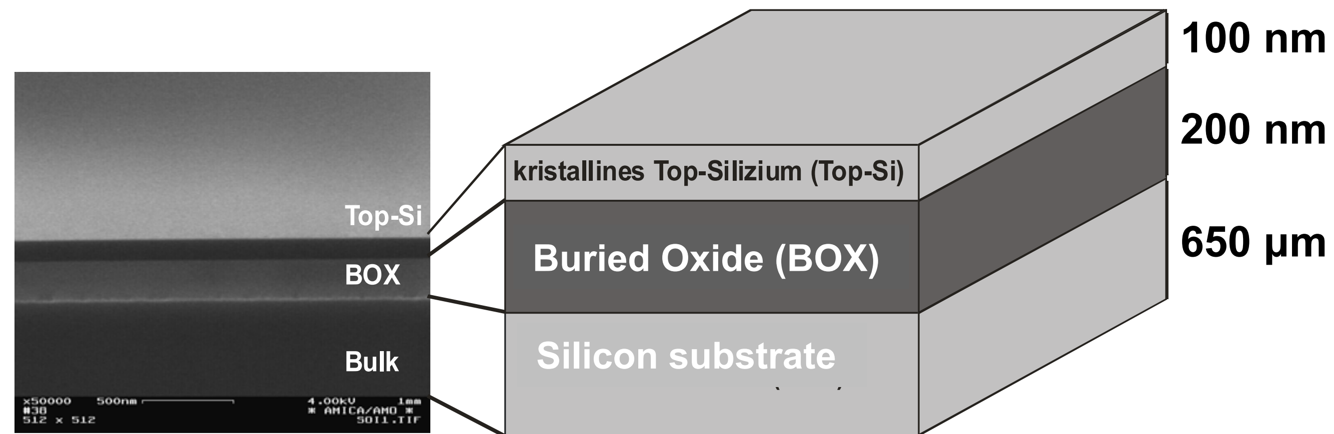
See also Plummer Fig 4-13

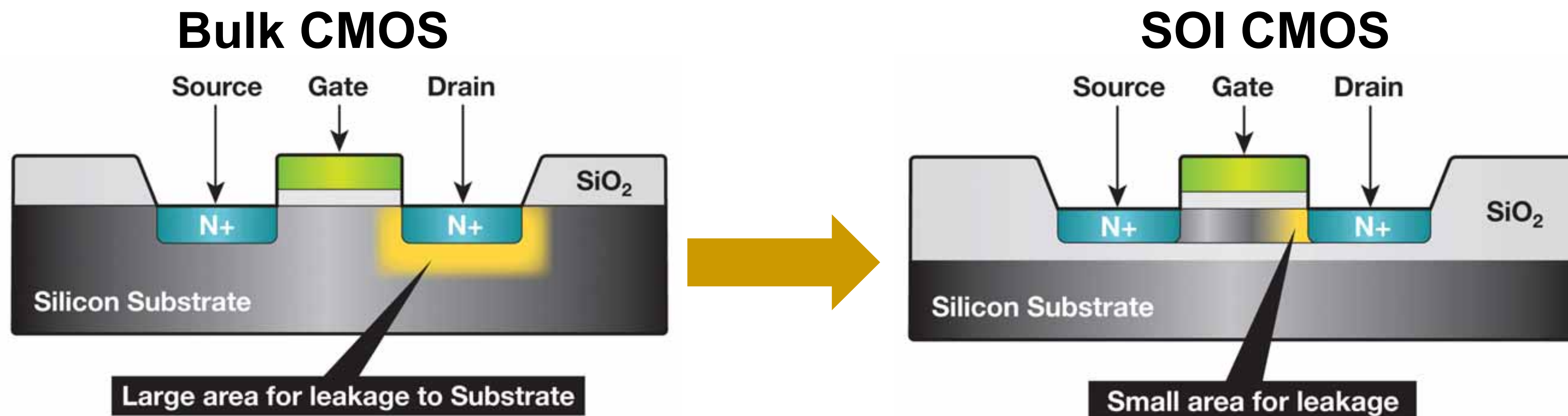
Silicon Wafer Fabrication: Silicon-on-Insulator (SOI)

Idea:

Active devices on insulating oxide to reduce leakage currents

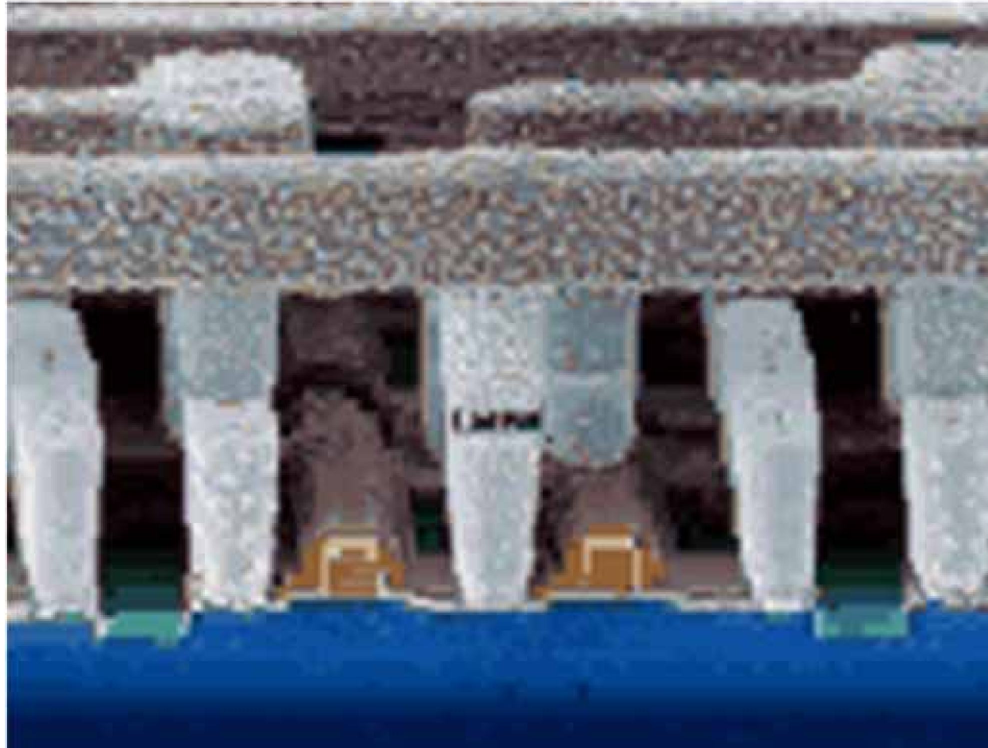
High quality silicon crystal isolated from bulk





Silicon Wafer Fabrication: Silicon-on-Insulator (SOI)

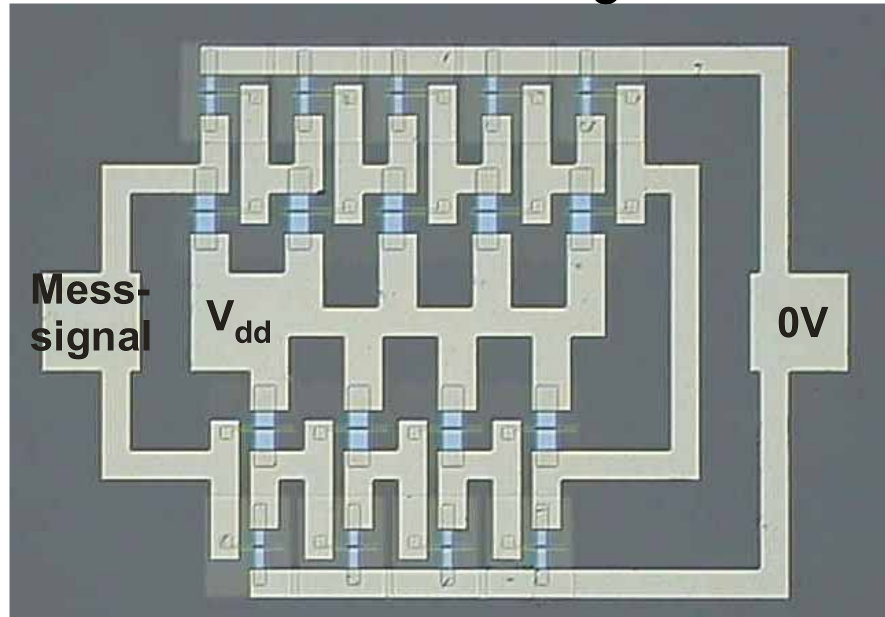
Example: Bulk vs. SOI Transistor



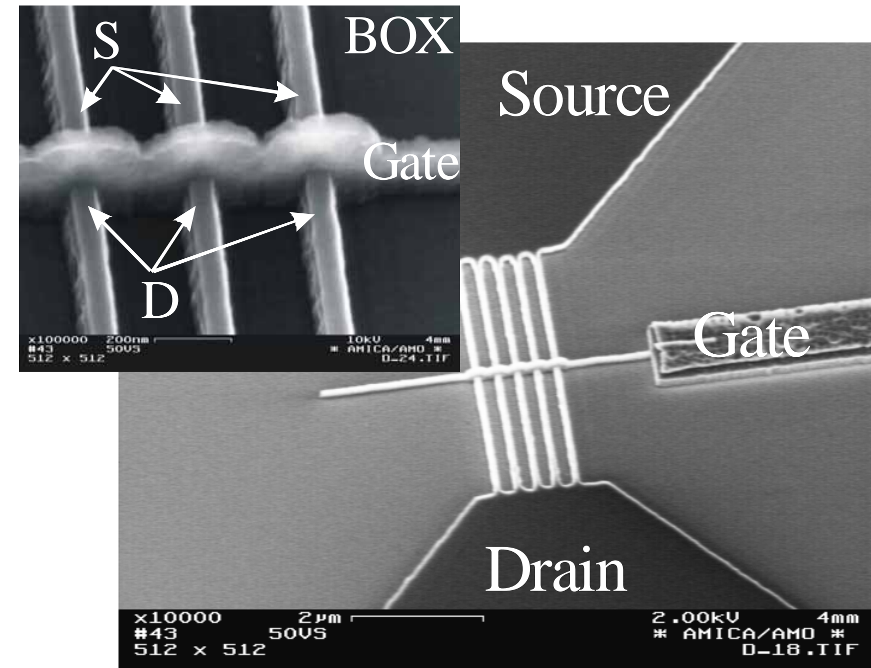
- Reduced leakage to the bulk
- Improved isolation between devices
- Smaller junction capacitance

Silicon Wafer Fabrication: Silicon-on-Insulator (SOI)

SOI-based CMOS Ring-Oscillator



SOI based FinFET

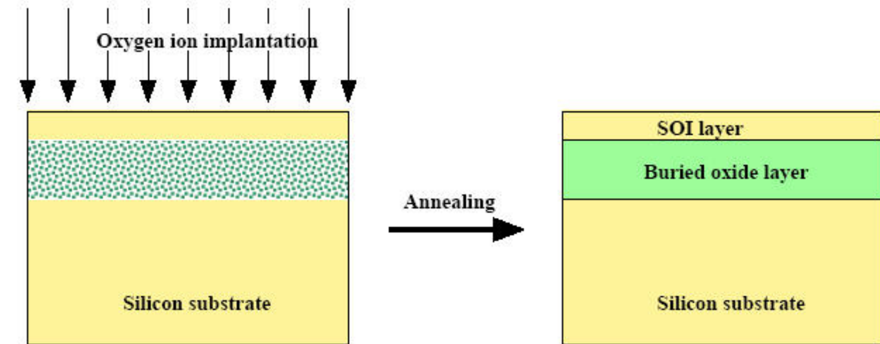


- Reduced leakage to the bulk
- Improved isolation between devices
- Smaller junction capacitance
- Enable 3-D structures (e.g. FinFET)
- Microelectromechanical Systems (MEMS)

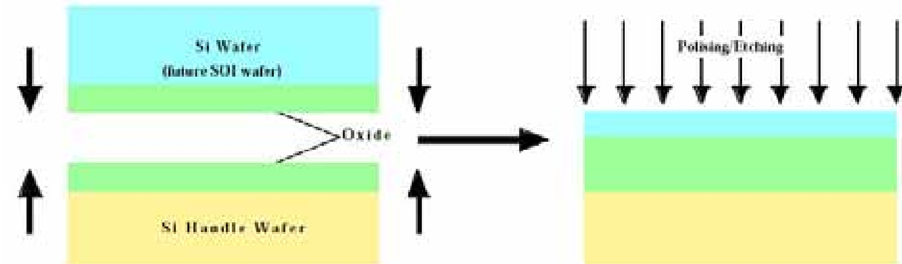
Silicon Wafer Fabrication: Silicon-on-Insulator (SOI)

Buried Oxide: ~ 10nm to 1μm thick

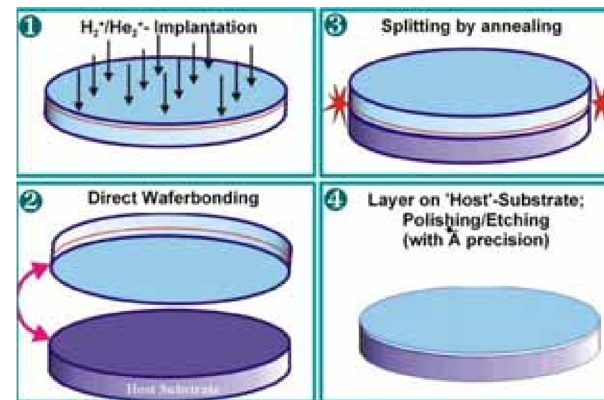
SIMOX:
Separation by implanted oxygen
Annealing to form SiO_2



BESOI:
Bonded and etched-back technology



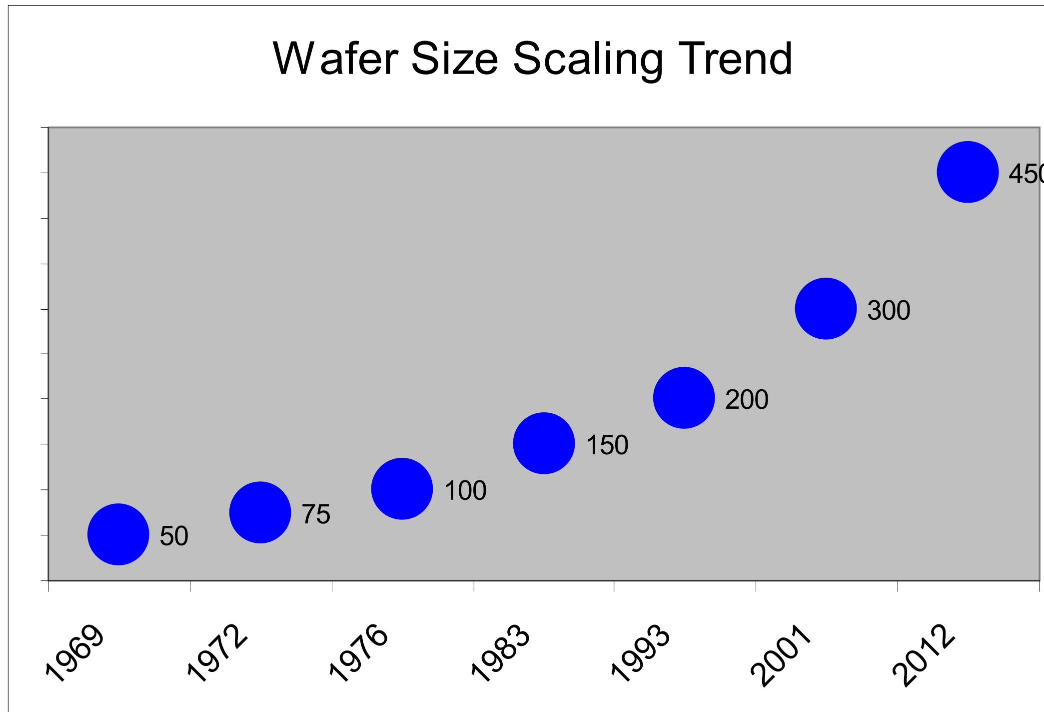
Smart-cut^{tm}:
H implant before BESOI process



SOS wafers: Silicon-on-sapphire

Source: MPI Halle

Silicon Wafer Fabrication: Wafer Size Scaling



http://technologyinside.com

Issues with transition to 450mm:
vibrational effects
gravitational bending (sag)
Flatness
crystal ingots 3 times heavier (1 ton!)
2-4 times longer cooling
2 x process time

Source: Covalent Materials（formerly Toshiba Ceramics)

Silicon Wafer Fabrication: Summary

- **Czochralski (CZ) Method**
- **Float Zone (FZ) Method**
- **From Ingot to Wafer**
- **Gettering**
- **Silicon-on-Insulator (SOI)**

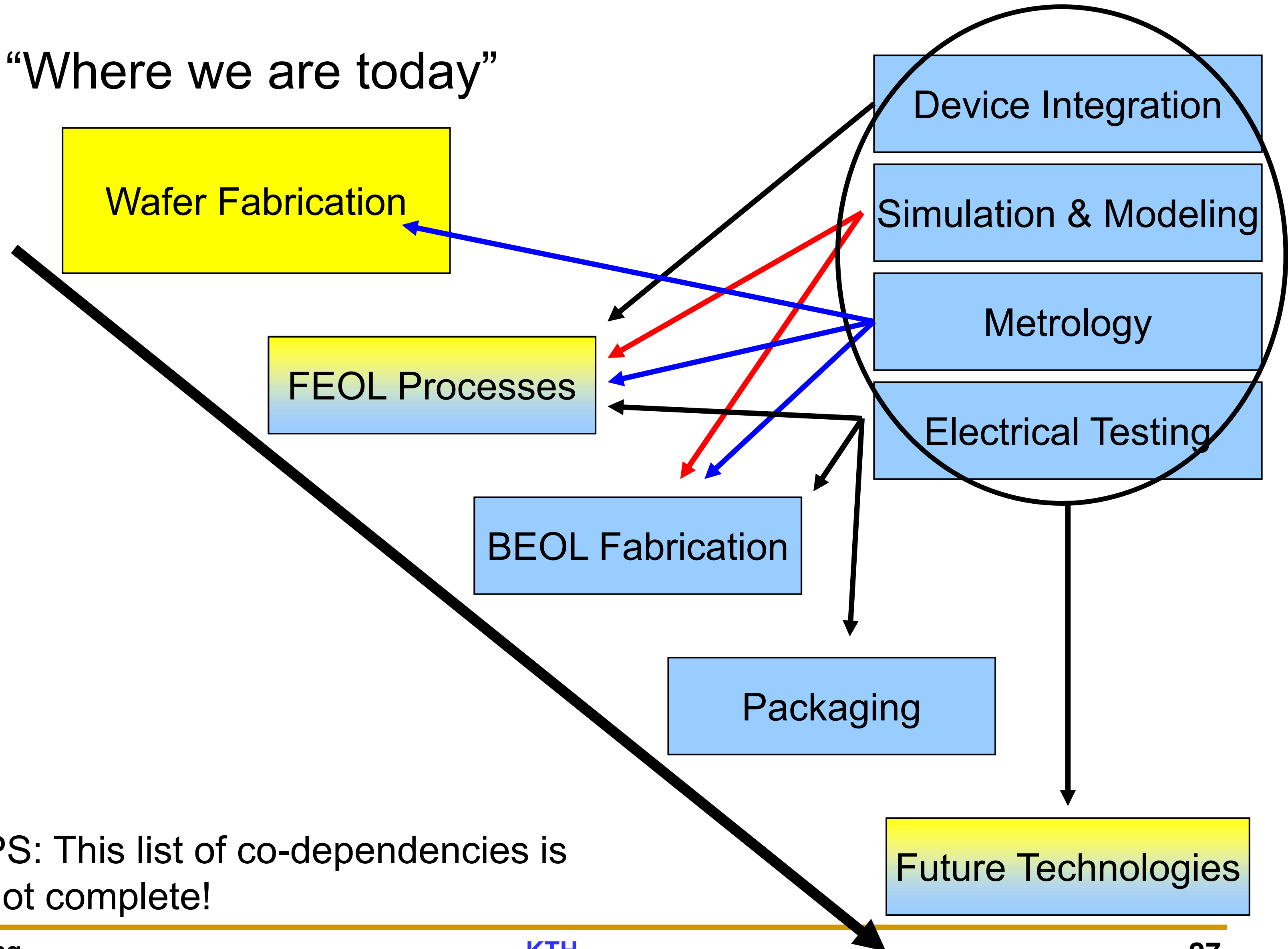
PS: For a short video of the wafer production process see:
http://www.siltronic.com/int/en/press/film/film-overview.jsp

Lecture 2: Wafer Fabrication and Silicon Epitaxy

Outline

- The Silicon Crystal
- Silicon Wafer Fabrication
- Silicon Epitaxy

Lecture 2: Wafer Fabrication and Silicon Epitaxy



PS: This list of co-dependencies is not complete!

Epitaxy

Outline:

Definition and terminology
Chemical vapor deposition
CVD process and source gases
Grove model:
- Mass-transfer or surface-reaction controlled growth rate

Gas flow and pressure in CVD
Chlorine in Si CVD
Doping
- Autodoping

Defects and characterization
Reactor types
- Batch
- Single-wafer
- MBE

Applications of Si epitaxy
- HT epitaxy: Si
- LT epitaxy: SiGe
- Selective epitaxy: Si and SiGe

Book references cited :

S.M. Sze: Semiconductor Devices 1985

S-M.Sze ed: VLSI Technology 1988

Chang and S.M. Sze: ULSI Technology 1996

S. Wolf and R.N. Tauber: Silicon Processing for VLSI vol. 1 1986

J. Plummer, Silicon VLSI Technology 2000

Epitaxy: Definition

Growth of single-crystalline layer on a single-crystalline substrate (bulk)

Epitaxal layer thickness: From one single atom layer up to ca 100 µm

Homoepitaxy : Si on Si

Heteroepitaxy : *e.g.* SixGe1-x on Si

Doping level can vary substantially between the layer and bulk

Advantages of epitaxy:

High purity monocrystalline silicon films for the device region

Lower temperature compared to implantation + diffusion → much more abrupt doping profiles

Large interval of thicknesses, doping profiles, and band gap engineering → ideal for creating "artificial" semiconductor structures, e.g.

- HBTs (Heterojunction Bipolar Transistors, H. Kroemer, Nobel Prize 2000)
- HEMTs (High electron mobility transistor, based on 2-DEG)

Epitaxy: Terminology for Silicon Epitaxy

Conventional, or high-temperature (HT) epitaxy

- T > 1000°C
- On blanket or patterned substrate wafers

Low-temperature (LT or LTE) epitaxy

- T < 1000°C
- Usually on patterned substrate wafers

Selective epitaxy

- always on patterned substrates

Terminology for Chemical Vapor Deposition (CVD) Silicon-Germanium (SiGe) epitaxy

Selective epitaxial growth: SEG

Non-selective epitaxial growth: NSEG

Heteroepitaxy (SiGe on Si)

Strained growth conditions, so-called pseudomorphic growth

h_c = critical thickness

Unstrained → dislocation network which are adverse for device operation

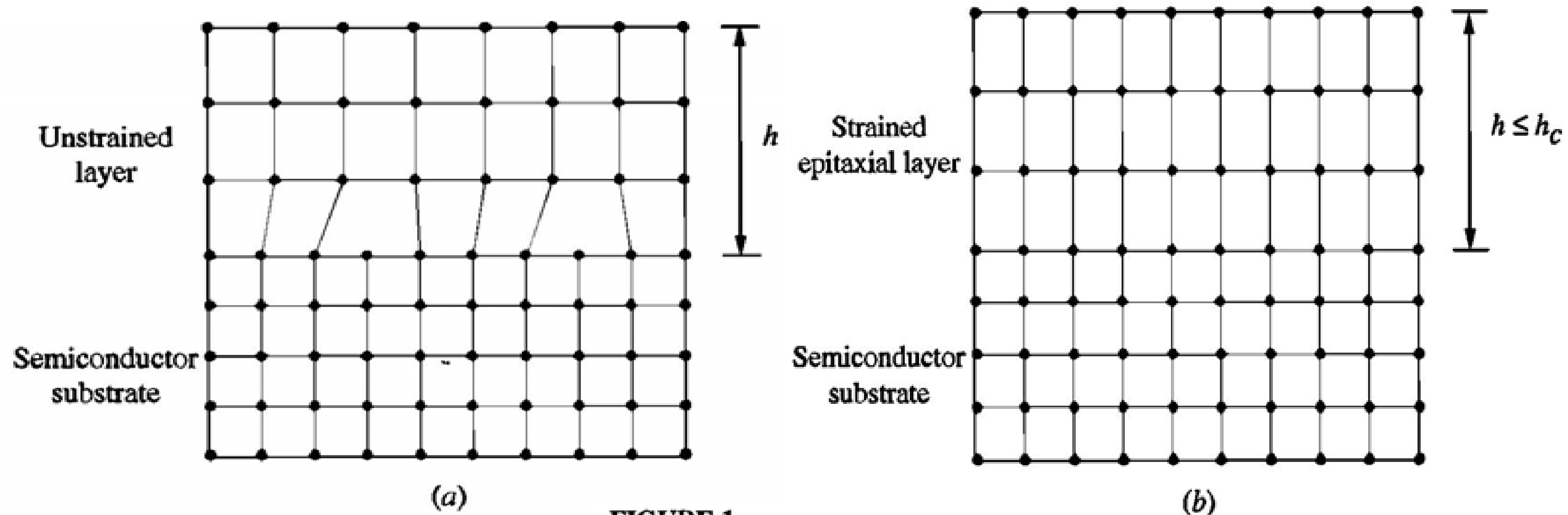


FIGURE 1
Schematic drawings of typical (*a*) unstrained and (*b*) strained heteroepitaxy.

(Chang p.106)

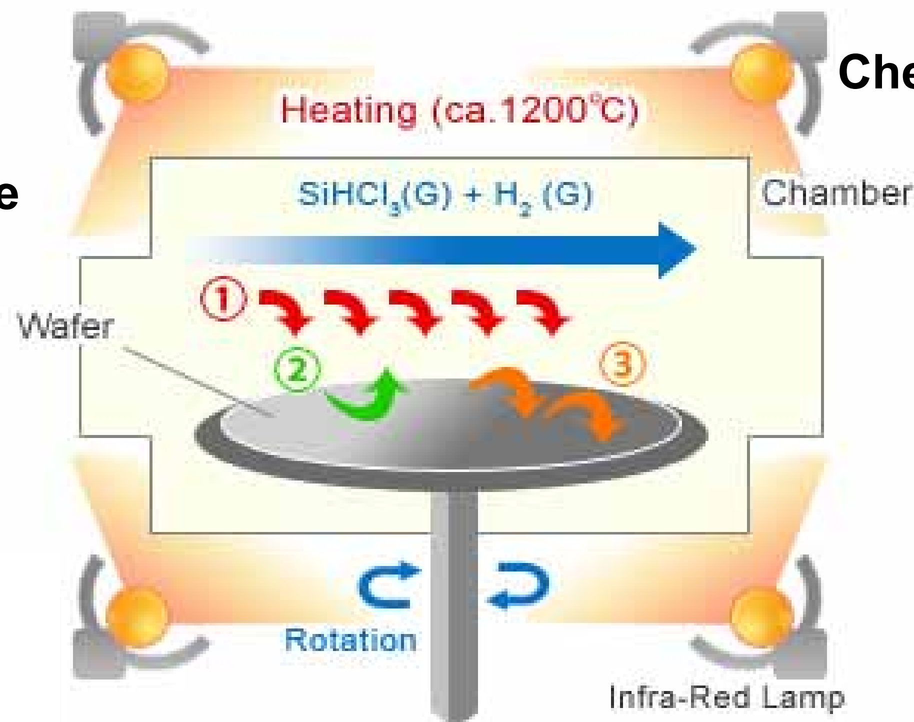
Silicon Epitaxy: Terminology

Technology of choice for Si epitaxial growth in production environment:

Chemical Vapor Deposition (CVD)

- sometimes denoted Vapor Phase Epitaxy (VPE)
- Hydrogen (H_2) carrier gas
- Reactants: $SiCl_4$, $SiHCl_3$, SiH_4, + dopant gases (AsH_3, B_2H_6…)
- HCl for selective growth and/or chamber cleaning
- N_2 for purge

Epitaxial Furnace



Chemical Vapor Deposition (CVD) method

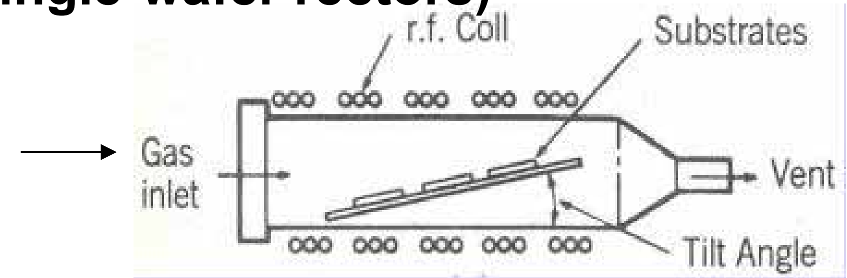
1. Adsorption of Si
2. **Desorption of byproducts**
3. Migration to growth site

http://www.sumcosi.com

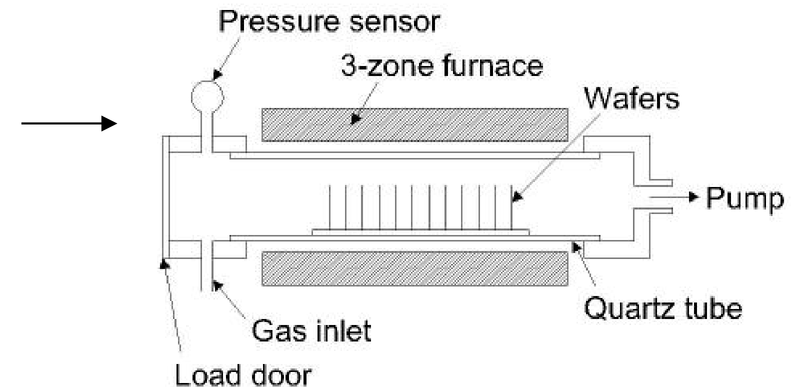
Epitaxy: CVD Reactor Types

Basic Si CVD types (both batch and single-wafer rectors)

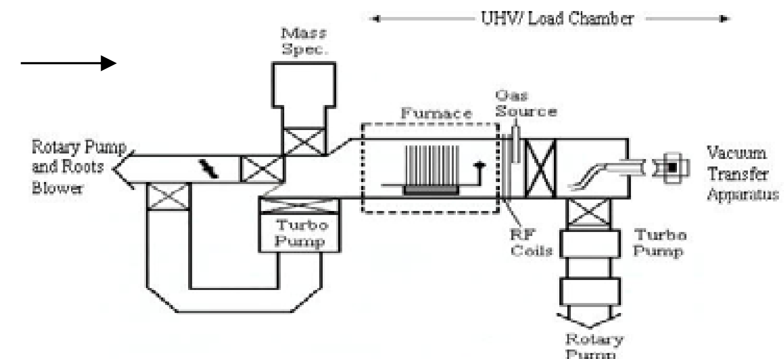
APCVD (atmospheric pressure CVD)
- Only for HT epitaxy (e.g. p-epitaxy on p+ bulk)



LPCVD (low-pressure CVD)
- Deposition around 10-100 torr, e.g. for n+ HT epitaxy,
- LT SiGe epitaxy or SEG



UHVCVD (ultra-high vacuum CVD)
- Deposition around 10-3 torr. For LT SiGe epitaxy
- Non Selective Epitaxial Growth (NSEG)



Epitaxy: CVD Process

1. Transport of reactants to the deposition region
2. Transport of reactants by diffusion from the main gas stream through the *boundary layer* to the wafer surface
3. *Adsorption* of reactants on the wafer surface
4. Surface processes: *migration*, *decomposition, reaction, site incorporation*
5. *Desorption* of byproducts from surface
6. Transport of byproducts through the boundary layer
7. Transport of byproducts from the deposition region

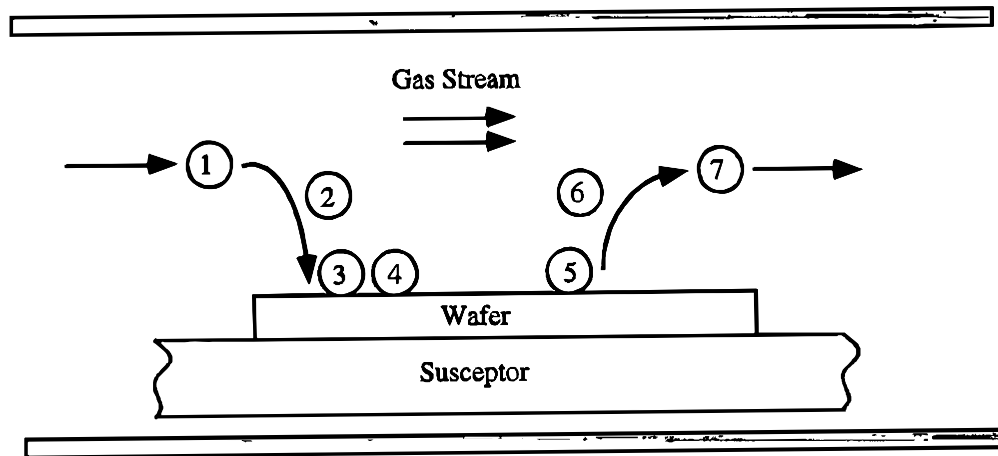


Figure 9–5 Steps involved in a CVD process. Numbered steps are explained in text.

(Plummer Fig 9-5 p 514)

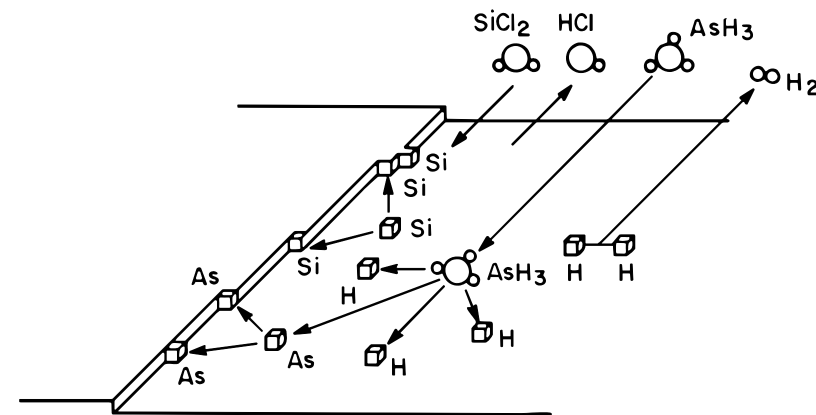
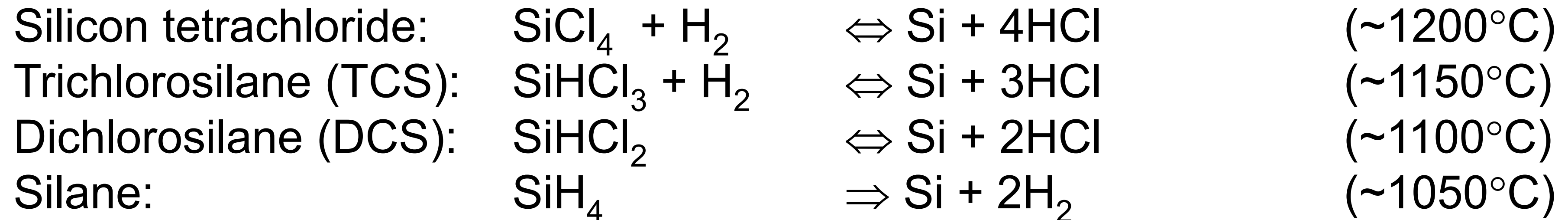


Fig. 19 Schematic representation of arsenic doping and growth processes.[12]

(Sze Fig 19 p323)

Si CVD sources and basic reactions for HT epitaxy



HT epitaxy: TCS or DCS

LT epitaxy: DCS or silane

TABLE 1
Epitaxial growth of silicon in hydrogen atmosphere

Chemical deposition	Nominal growth rate(μm/min)	Temperature range(°C)	Allowed oxidizer level (ppm)
$SiCl_4$	0.4–1.5	1150–1250	5-10
$SiHCl_3$	0.4–2.0	1100–1200	5-10
SiH_2Cl_2	0.2–1	1050–1120	<5
SiH_4	0.2–0.3	950–1250	<2

(Sze VLSI Table I p. 65)

The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

(Sze Fig. 20 p 324; see also Plummer 9-6, p.515)

$$F_1 = h_g (C_g - C_s)$$

$$F_2 = k_s C_s$$

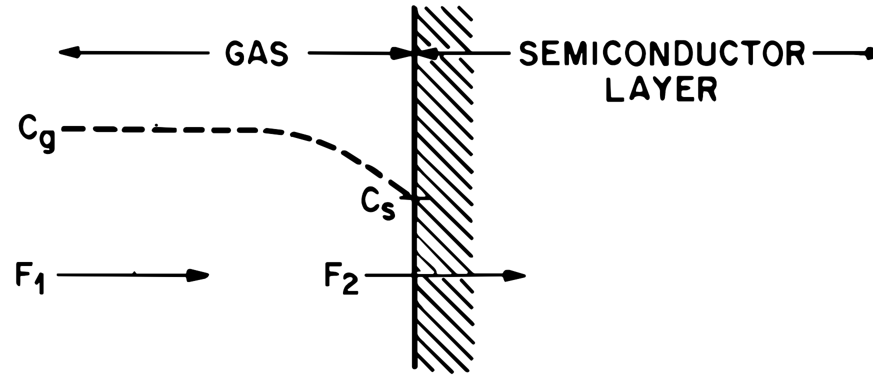


Fig. 20 Model of the epitaxial-growth process.

F_1, F_2: flux of reactant species from gas phase / of reactant consumed at surface
h_g: vapor mass transfer coefficient (cm/s)
C_g, C_s: concentration of reactant species in gas / at surface
K_s: surface reaction constant

Assume:

Steady state: $F_1 = F_2 = F$
Growth rate $n = F/C_a$ where C_a = number of Si atoms/cm^3

The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

Steady state: $F_1 = F_2 = F$
Growth rate $n = F/C_a$ where C_a = number of Si atoms/cm^3

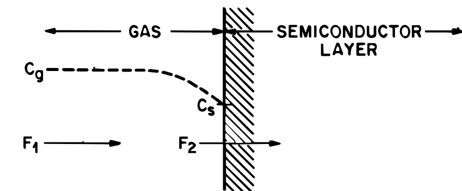


Fig. 20 Model of the epitaxial-growth process.

$C_g = yC_t$ where y is the mole fraction and C_t is the total number of gas molec/cm^3 ➔

$$v = \frac{k_s h_g}{k_s + h_g}\left(\frac{C_t}{C_a}\right)y$$

k_s small ➔ Surface reaction controlled $v \cong k_s\left(\frac{C_t}{C_a}\right)y$; $C_s \rightarrow C_g$

h_g small ➔ Mass-transport controlled $v \cong h_g\left(\frac{C_t}{C_a}\right)y$; $C_s \rightarrow 0$

k_s: surface reaction constant
h_g: vapor mass transfer coefficient (cm/s)

CVD Epitaxial Growth: Temperature Dependence

"Arrhenius-Plots"

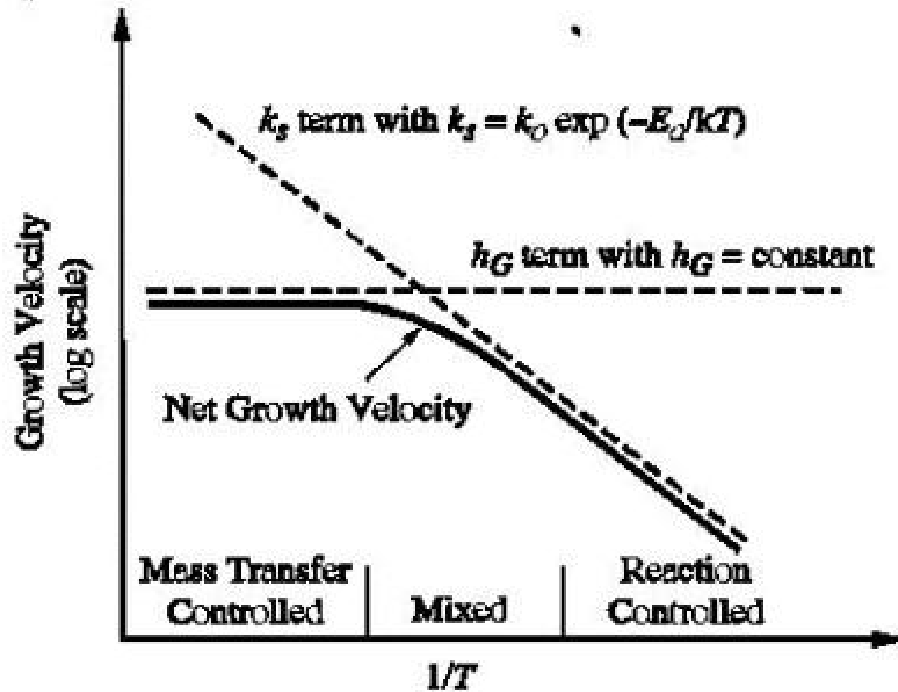


Figure 9–7 Arrhenius plot of growth velocity (or deposition rate) vs. 1/T for CVD process. The net growth velocity is the result of the surface reaction and gas-phase mass transfer processes acting in series so that the slower of the two dominates at any temperature.

(Plummer Fig 9-7)

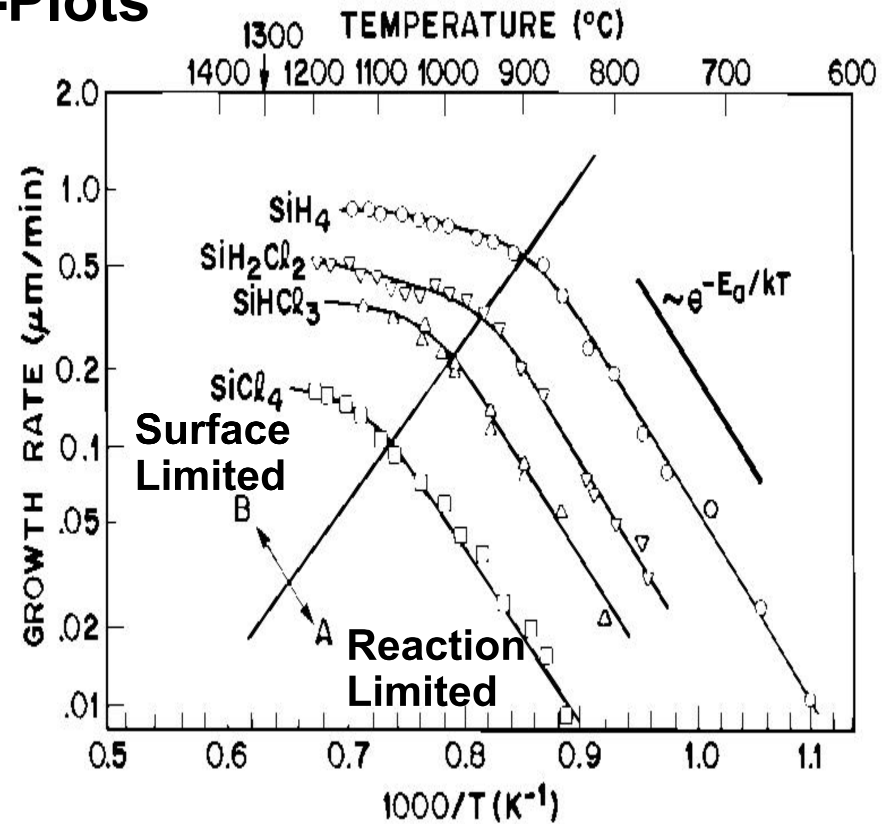


Fig. 21 Temperature dependence of the growth rate for various silicon sources.[13]

(Sze Fig 21 p. 326)

k_s: surface reaction constant

h_g: vapor mass transfer coefficient (cm/s)

CVD Epitaxy in the Mass-Transport Controlled Regime

Gas flow rate

Laminar gas flow with velocity *v* above a *boundary layer* with thickness δ

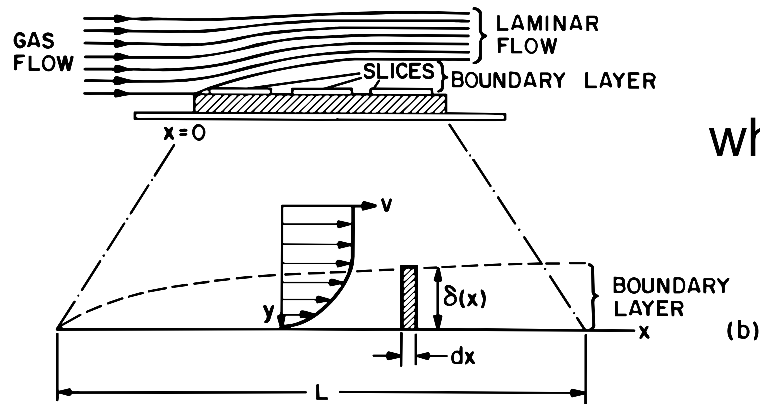


Fig. 22 (*a*) Development of a boundary layer in gas flow over a flat plate. (*b*) Expanded view of the boundary layer.

(Sze Fig. 22 p.327)

Analysis of friction force → $h_g = D_g/\delta$

where D_G is gas diffusion coefficient across δ

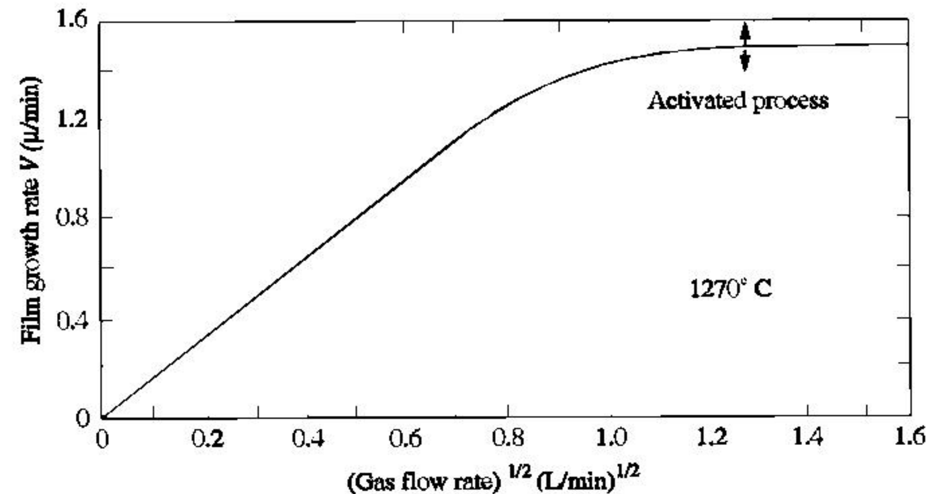


FIGURE 7
The growth rate of an epi-Si versus the free gas flow rate. (*After Wolf and Tauber, Ref. 20.*)

(Chang Fig 7 p 114)

CVD Epitaxy in the Surface Reaction Controlled Regime

Deposition not (very) sensitive to geometrical arrangement of wafers in reactor. However, low growth rates!

Can be solved by reducing total pressure which affects D_G and extends surface-reaction limited region to higher T:

D_G: gas diffusion coefficient across δ

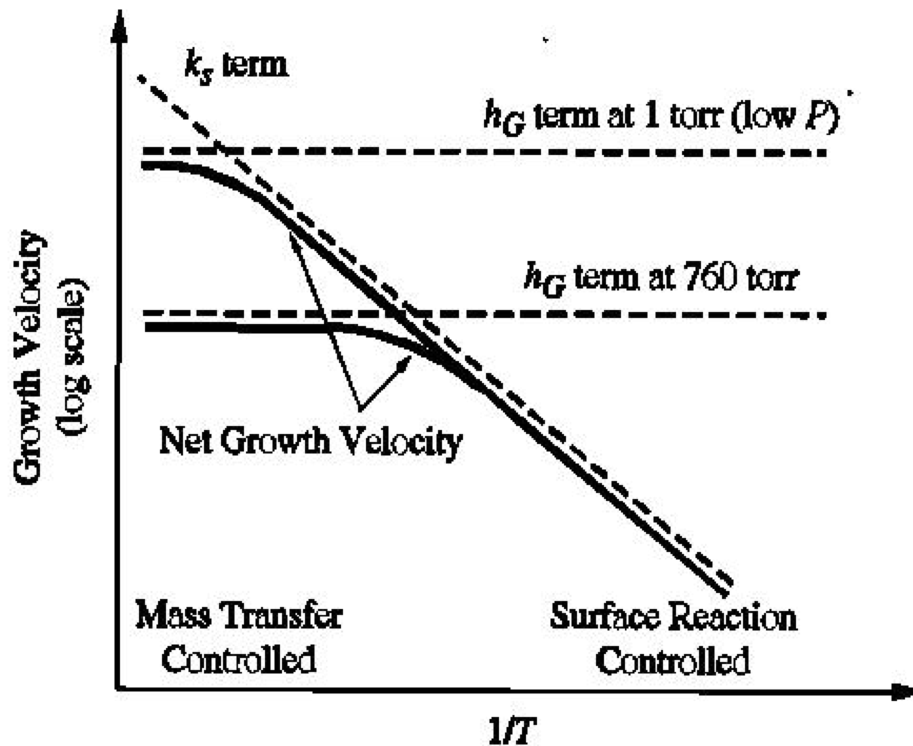
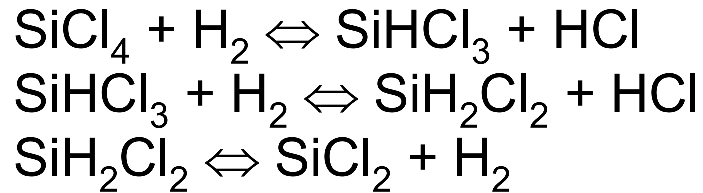


Figure 9–13 Growth velocity vs. $1/T$ for APCVD (760 torr) and LPCVD (1 torr) systems. The lower total pressure (with P_G and C_G remaining fixed) shifts the h_G curve upward, extending the surface reaction regime to higher temperatures.

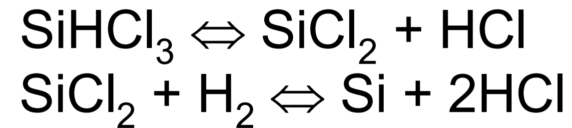
(Plummer Fig 9-13)

Silicon Epitaxy: Cl-based Chemistry

- Either *deposition* or *etching* depending on T, P or concentration (mole Fraction)
- Reaction is complex, e.g. SiCl4

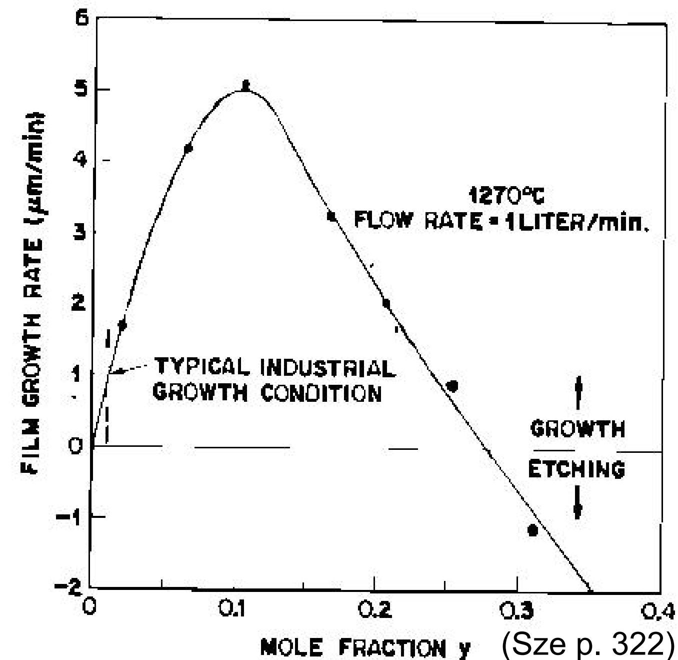


$$SiCl_4 + H_2 \Leftrightarrow SiHCl_3 + HCl$$
$$SiHCl_3 + H_2 \Leftrightarrow SiH_2Cl_2 + HCl$$
$$SiH_2Cl_2 \Leftrightarrow SiCl_2 + H_2$$



$$SiHCl_3 \Leftrightarrow SiCl_2 + HCl$$
$$SiCl_2 + H_2 \Leftrightarrow Si + 2HCl$$

Reversible reactions!



(Sze p. 322)

Fig. 2 Silicon growth rate as a function of $SiCl_4$ concentration[52].

Silicon Epitaxy: Cl-based Chemistry

Crystallinity also depends on growth rate:

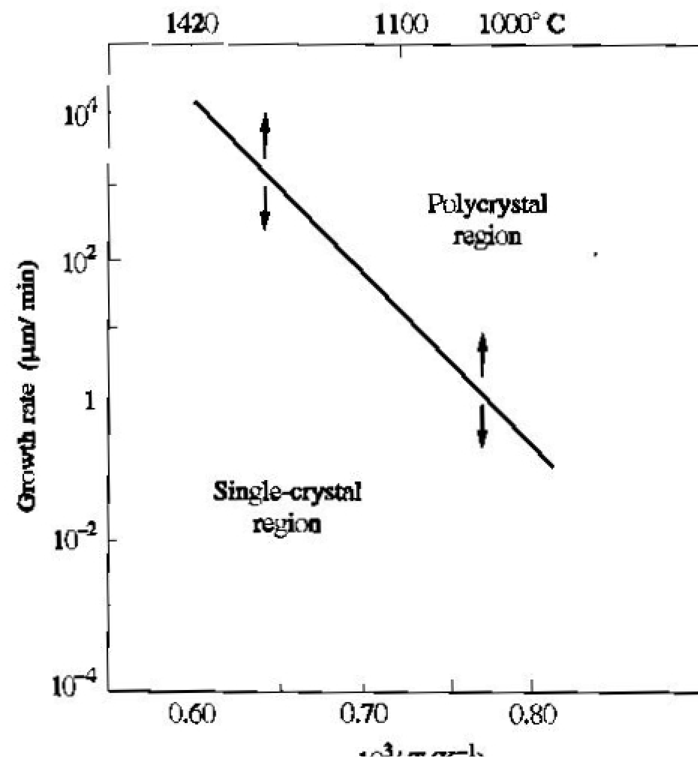


FIGURE 10
Crystallinity with respect to growth rate and growth temperature. (*After Bloem, Ref. 10.*)

(Chang Fig 10 p)

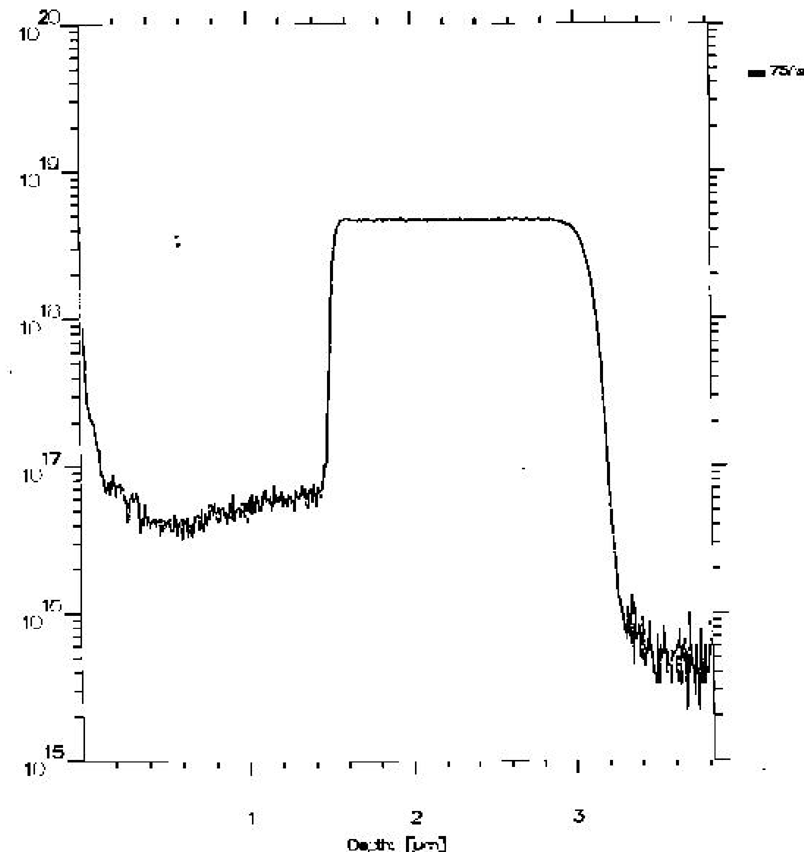
Silicon Epitaxy: Doping

Doping sources: B_2H_6 (diborane), AsH_3 (arsine) and PH_3 (phosphine).
Not standard: $SbCl_5$

Dopant incorporation dependent upon T, growth rate, dopant/Si ratio in gas phase, reactor geometry

B_2H_6 enhances growth rate
PH_3 reduced growth rate

Example from KTH:
Double-epi (n^-/n^+) using AsH_3 on p^- bul



Radamson & Grahn 98

Autodoping

Lightly doped n-epi-layer grown on n^+ substrate → autodoping, i.e. *unintentional doping from substrate, susceptor, adjacent wafers etc.*

Both *vertical* and *lateral* autodoping may occur , e.g. during epitaxy on buried n^+-layer

Remedies:
Low-pressure CVD for HT n-type epi
Reduced deposition temperature
Observe: Autodoping is not a problem for B!

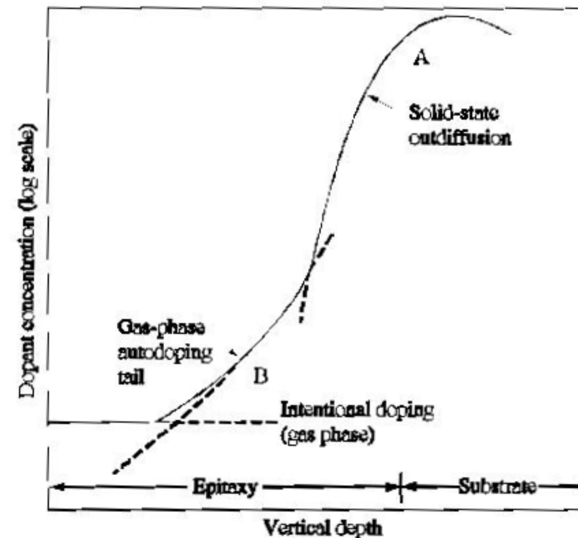


FIGURE 16
A typical doping profile of an epi-Si grown over a heavily doped Si substrate. (*After Srinivasan, Ref. 18.*)

(Chang Fig 16 p. 120)

Defects in Epitaxial Layers

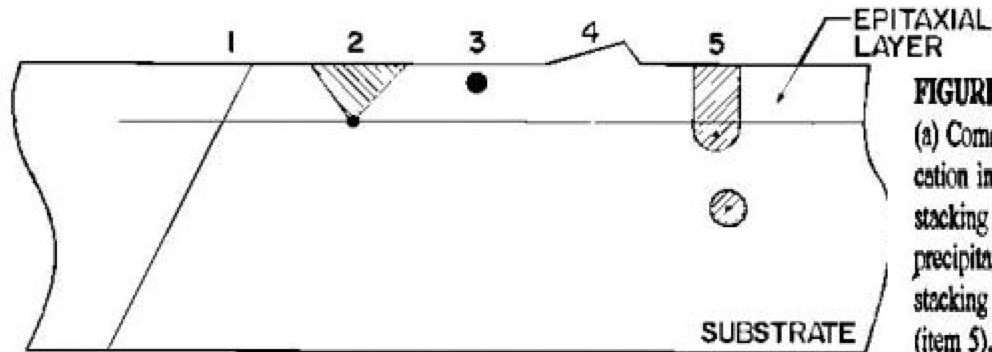


FIGURE 20

(a) Common defects occurring in epitaxial layers. Schematic representation of line (or edge) dislocation initially present in the substrate and extending into the epitaxial layer (item 1), an epitaxial stacking fault nucleated by an impurity precipitate on the substrate surface (item 2), an impurity precipitate caused by epitaxial process contamination (item 3), growth hillock (item 4), and bulk stacking faults, one of which intersects the substrate surface, thereby being extended into the layer (item 5).

(Sze VLSI Fig. 20 p 76)

- Dislocations (line defect)
- Stacking faults (area defect) visible as squares for (100) and triangles for (111)
- Precipitates (volume defect)
- Hillocks or voids (volume defects)

Substrate surface quality and cleaning prior to epitaxy are crucial, in particular LT epitaxy.

Slip in HT epitaxy:
Dislocation network caused by temperature gradient across wafer during RTA-CVD (single-wafer machines)

Epi Thin Film Characterization

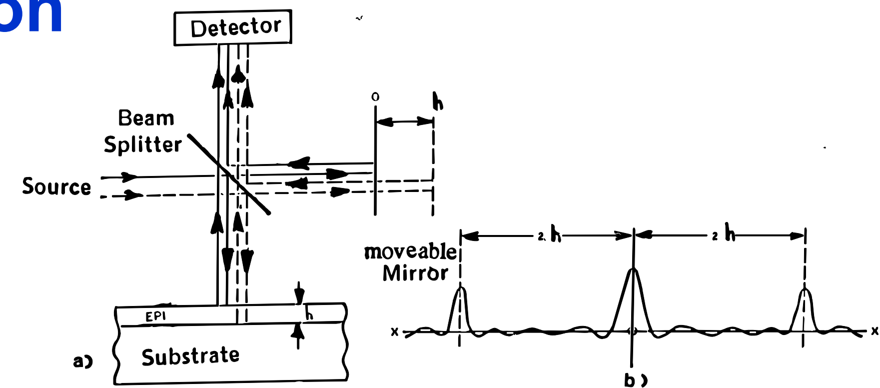


Fig. 24 Schematic representation of interferometric measurement of epitaxial layer thickness. (a) interferometer showing path lengths, (b) interferogram showing a coherence peak and side-bursts.

(Wolf Fig 24 p 151)

Surface smoothness:
Optical microscopy
Nomarski contrast microscopy
Atomic force microscopy (AFM)

Film thickness and doping:
Secondary ion mass spectroscopy (SIMS)
Fourier-transform Infrared Spectroscopy (FTIR)
Spectroscopic Ellipsometry

Crystallographic quality:
High-resolution X-ray diffractometry for Ge content and thickness in SiGe

Electrical properties:
Film resistivity vs doping
Minority carrier life time measurement
Device characteristic

Destructive, non-destructive or device-based methods!

Reactor Types for Si Epitaxy

Batch reactor types
Almost only for HT epitaxy (exception UHVCVD)

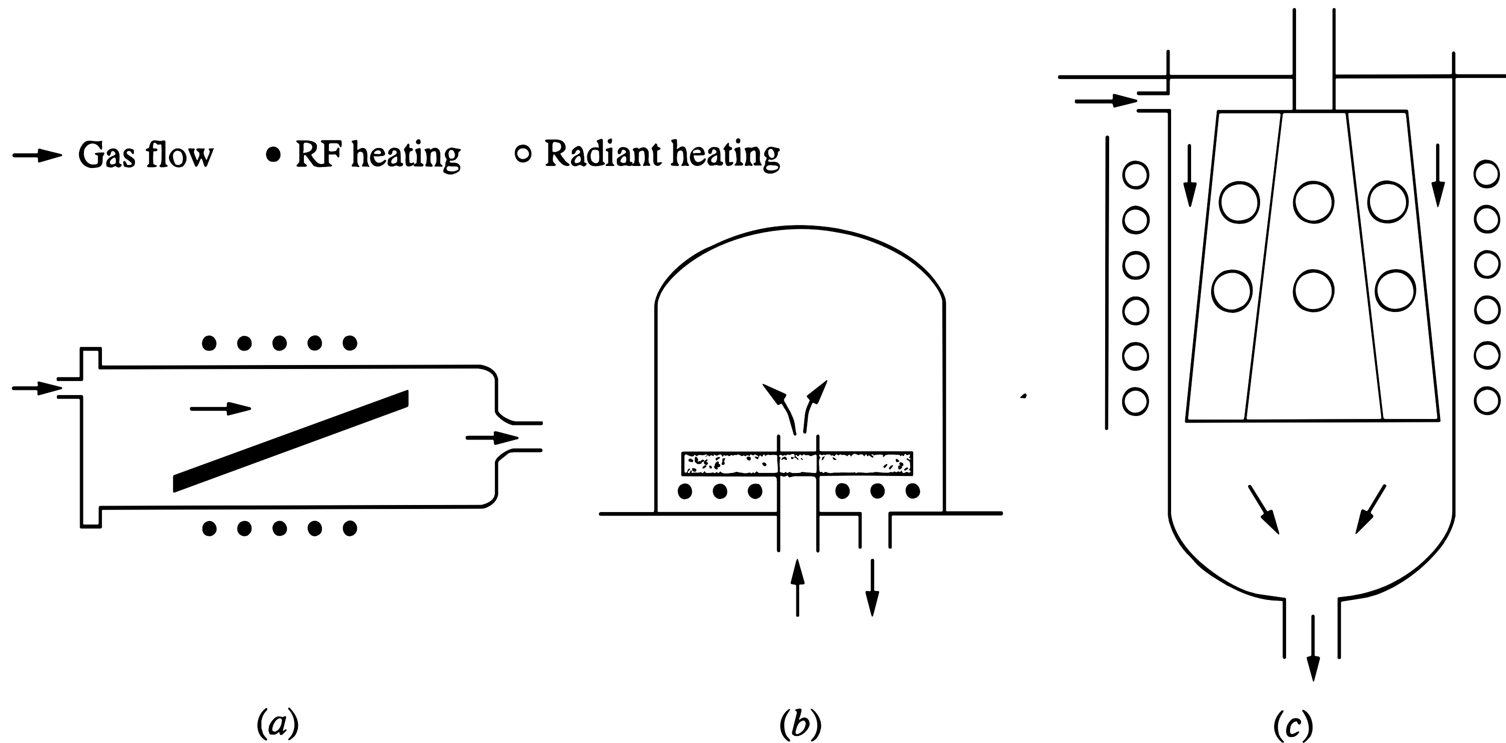


FIGURE 20
Types of conventional epitaxial reactors: (*a*) horizontal reactor; (*b*) vertical reactor; (*c*) barrel reactor. (*After Pearce, Ref. 27.*)

(Chang Fig. 20 p124)

Reactor Types for Si Epitaxy: Batch Type

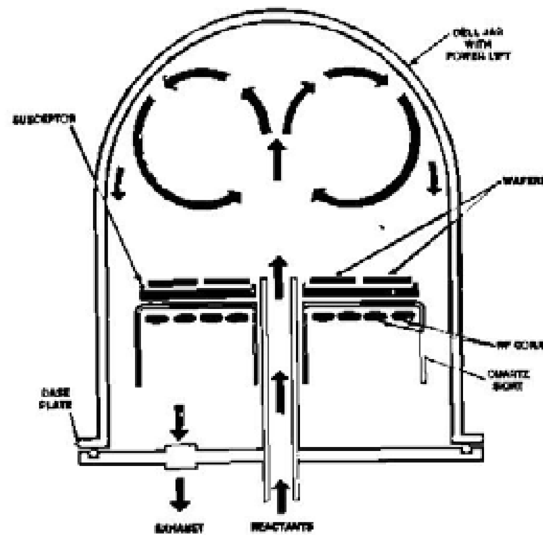


Fig. 21 Schematic of an induction heated vertical pancake reactor. Courtesy of Microelectronic Manufacturing and Testing.

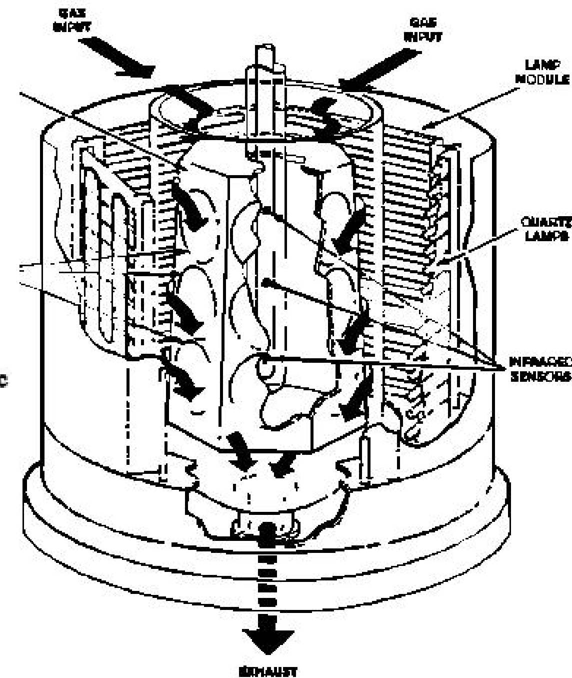


Fig. 22 Schematic of a radiantly heated barrel reactor. Courtesy of Applied Materials Inc.

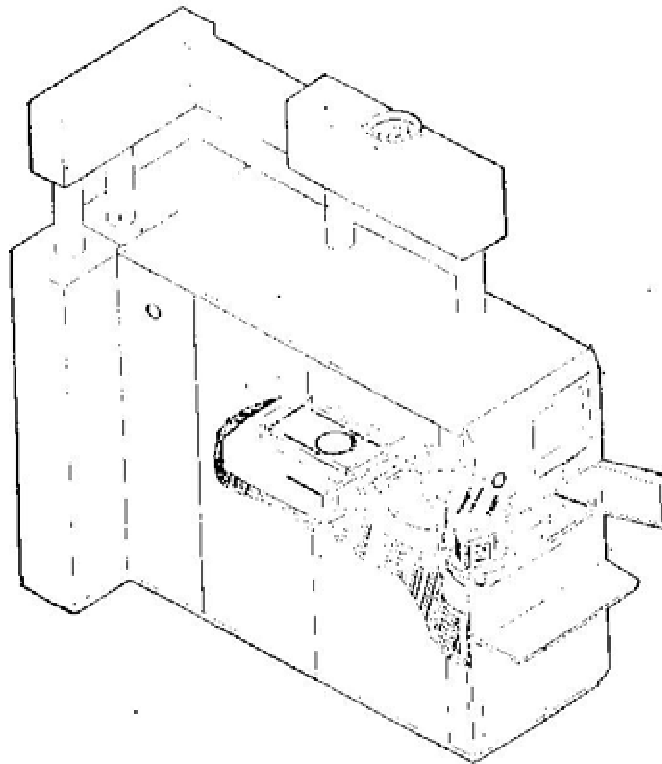
Reactor Types for Si Epitaxy: Single-wafer Si Epitaxy

RTP process!

Both for HT and LT epitaxy (Si/SiGe)

Used for production of wafers, epi on buried layers and LT epi SiGe.

Example:



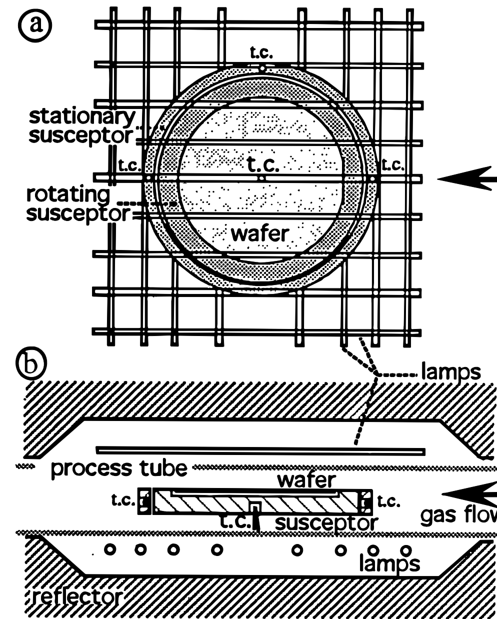


Fig.1 - Top view (a) and cross section (b) of the reactor chamber, showing the geometry and the position of the heating lamps with respect to the wafer, susceptor and thermocouples (t.c.).

(ASM Epsilon 2000 at KTH)

Ultra High Vacuum CVD (UHVCVD)

LT non-selective epi method developed by IBM specially for SiGe
Batch method at very low temperature 500-600°C

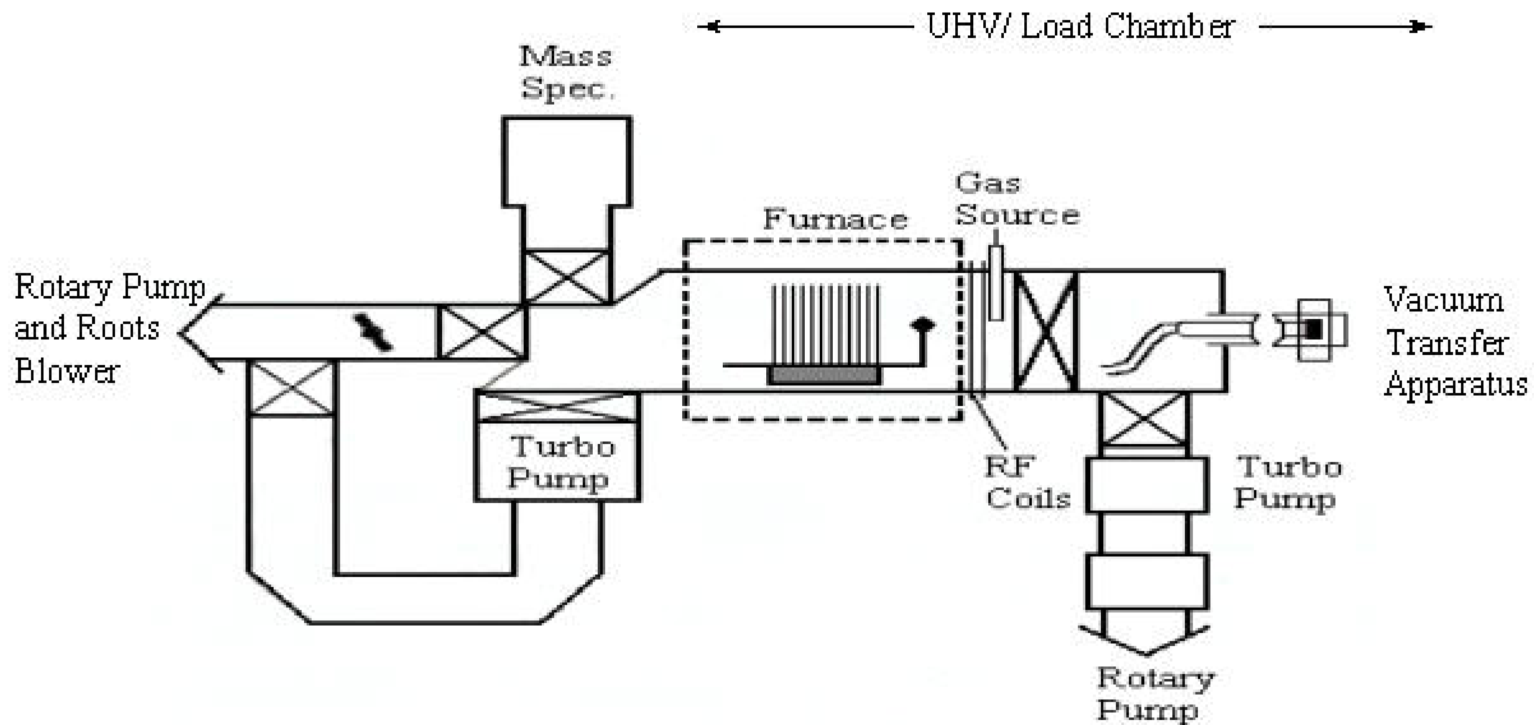


FIGURE 22
Schematic drawing of a UHV/CVD system. (*After Meyerson, Ref. 29.*)

(Chang Fig 22 p 128)

Silicon Molecular Beam Epitaxy (MBE)

Physical vapor deposition (PVD) method

Typical for thin film research for SiGe(C) epitaxy (not in production!)

- Vacuum evaporation with excellent thickness control
- Ultra-high vacuum
- Extremely low growth temperatures < 500°C
- *In situ* analysis of growing film
- As (arsenic) and, in particular, Ph (phosphor) dopants difficult. Often Sb (antimony) for n+

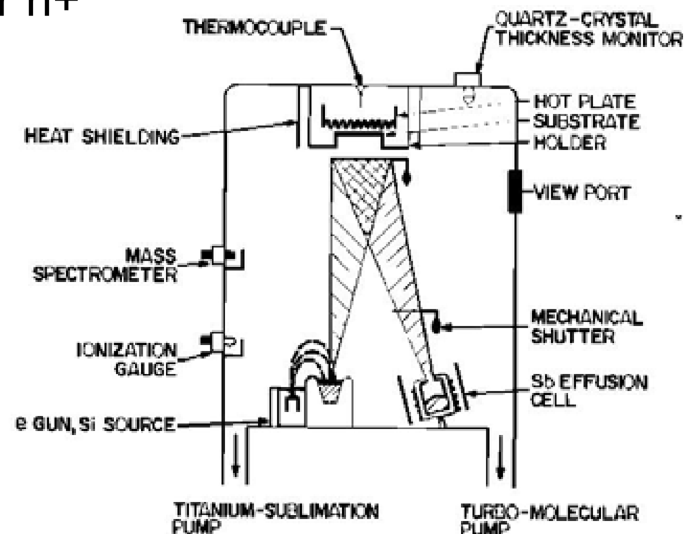


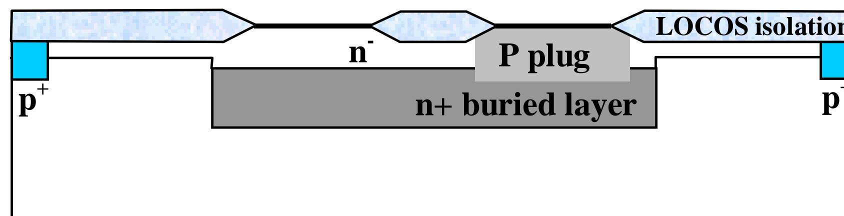
FIGURE 23
Schematic of MBE growth system. (*After Konig, Kibbel, and Kasper, Ref. 54.*)

(Sze VLSI Fig 23 p.80)

Applications of Si epitaxy

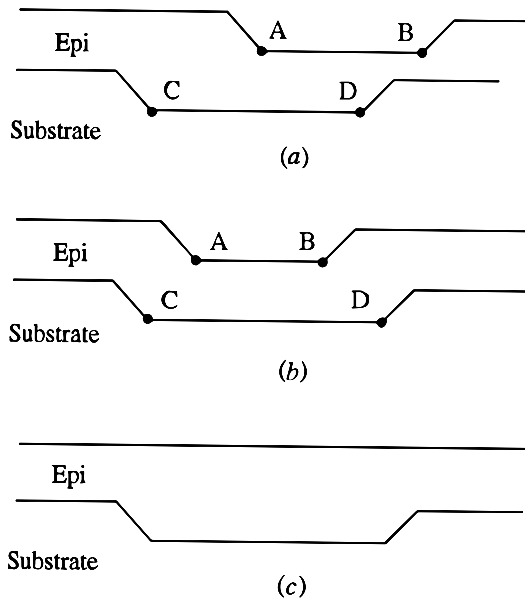
HT epitaxy:

p- epi on p+ bulk in CMOS for suppression of latch-up
n- epi on n+ buried collector layer in bipolar devices for reduced series resistance



Grahn ASM User meeting'99

Problem: *Pattern shift* during n-epi on buried layer:



- different crystal planes lead to significantly different growth rates
- geometry of a feature can influence growth rate (feature edges)
- Important to control for wafer alignment on buried layer!

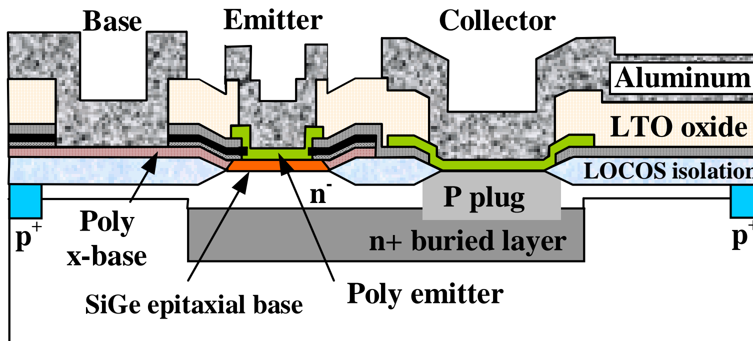
FIGURE 19
Schematic illustrations of (*a*) pattern shift, (*b*) pattern distortion, and (*c*) pattern washout. (*After Wolf and Tauber, Ref. 24.*)

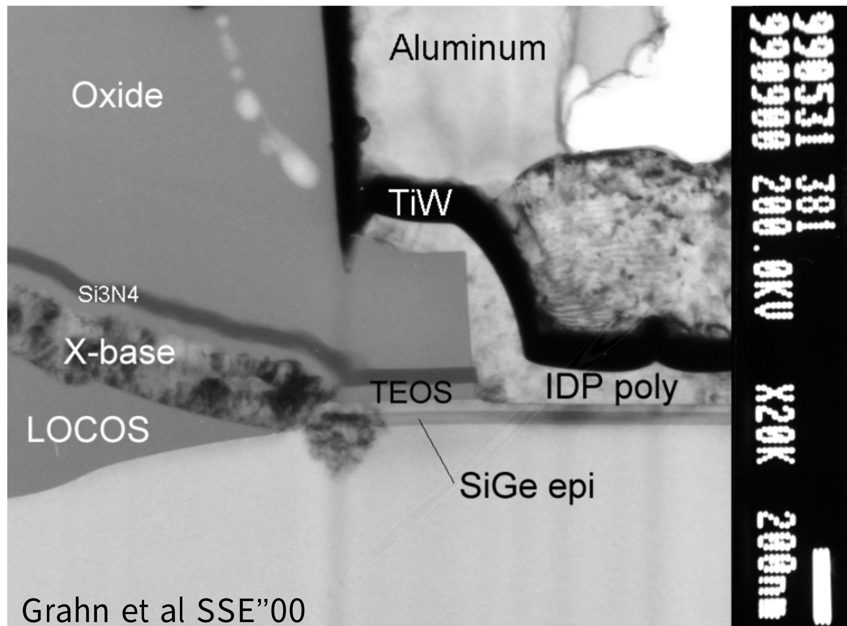
(Chang p.123)

Applications of SiGe epitaxy

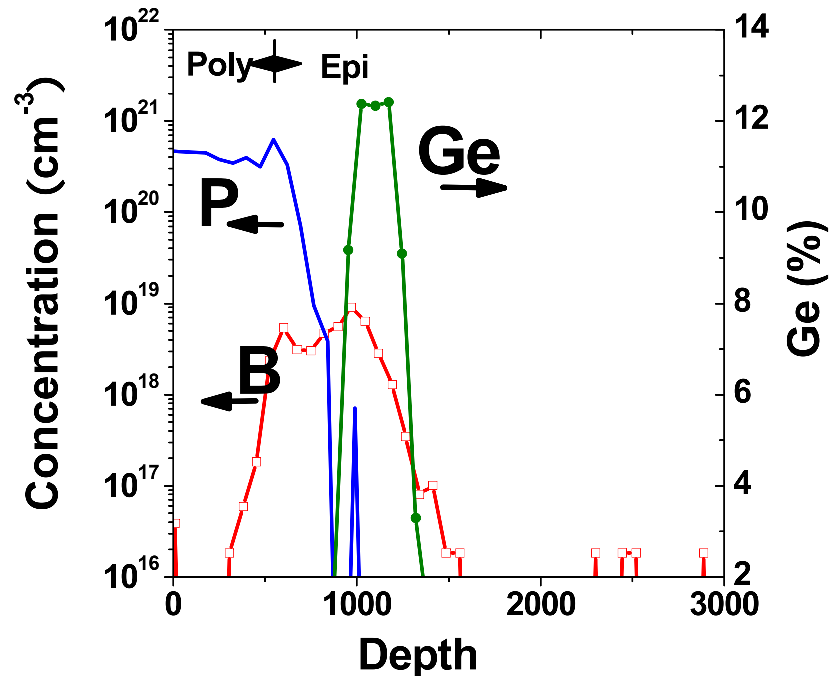
LT epitaxy:

SiGe epi for base in bipolars, channel for MOS





KTH SiGe HBT using NSEG SiGe



Applications of SiGe epitaxy

SiGe LT epitaxy

Typically at 550-650°C using UHVCVD, LPCVD or APCVD

Selective or non-selective growth

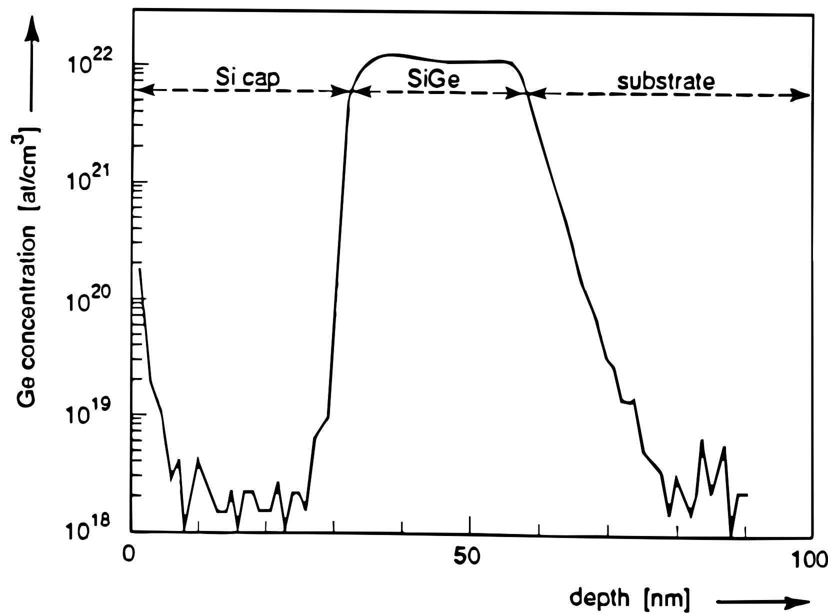


Figure 4. SIMS profile of a SiGe layer capped with a Si layer, grown at 625°C by APCVD. The Ge transitions at the SiGe/Si interfaces are exceptionally steep and totally determined by the SIMS resolution.

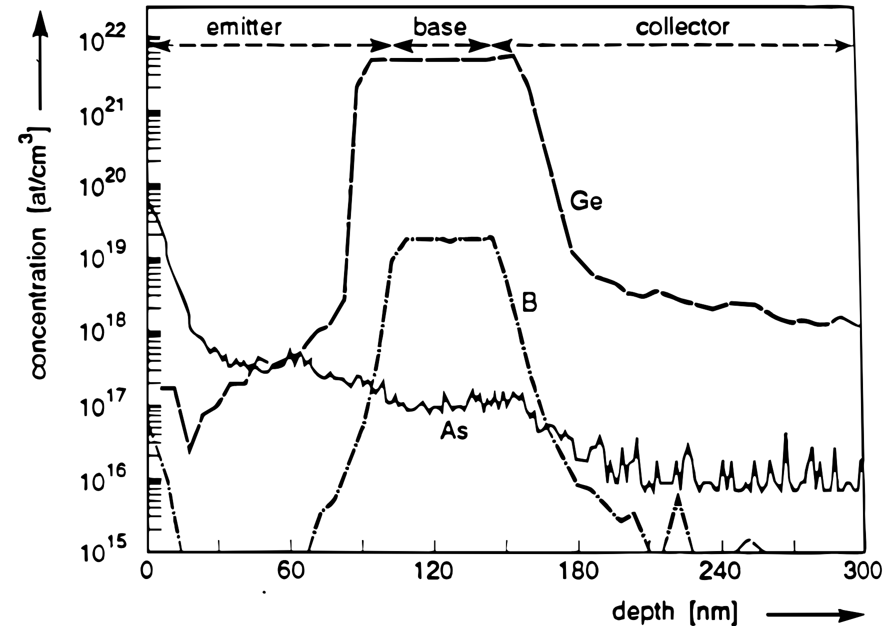


Figure 7. SIMS profiles of an HBT structure grown by APCVD at 900°C (collector) and 700°C (base and emitter). The box-shaped profiles allow very accurate control of the base width and dopant content. The As signal in the SiGe material is meaningless due to interference of As and GeH.

de Boer MRS 94

Silicon Selective Epitaxial Growth (SEG)

Chemistry:

Addition of HCl to DCS makes Si epi selective with respect to field oxide
SEG is a difficult process in VLSI!
STI isolation is the preferred process choice

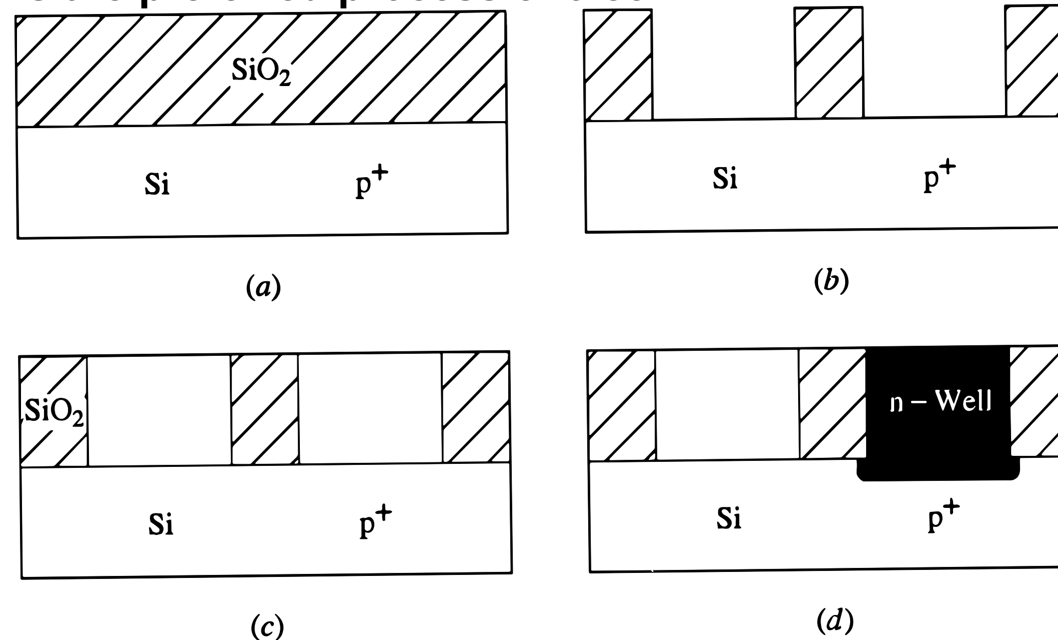
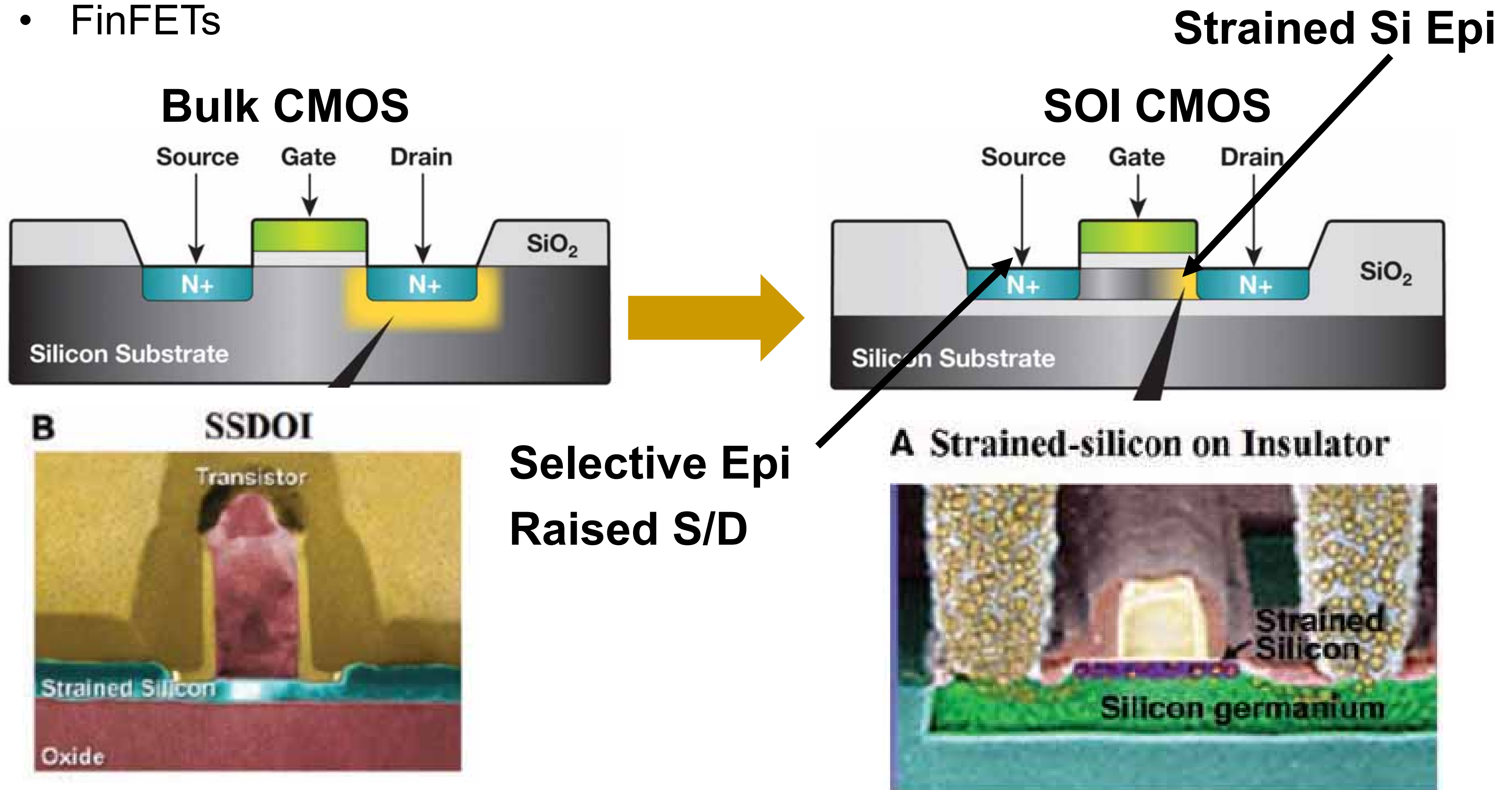


FIGURE 25
Schematic illustration of a typical SEG process for device isolation: (*a*) oxide deposition; (*b*) window formation; (*c*) epi growth; (*d*) n-well drive-in. *(After Borland and Drowley, Ref. 57.)*

Applications of Silicon Selective Epitaxial Growth (SEG)

Source-Drain regions of nanoscale MOSFETs, especially in novel structures:

- Ultra-Thin-Body-SOI MOSFETs
- FinFETs



M. Ieong et al. , Silicon Device Scaling to the Sub-10-nm Regime, Science 306, 2057-2060, 2004

Applications of Epitaxy in the CMOS process

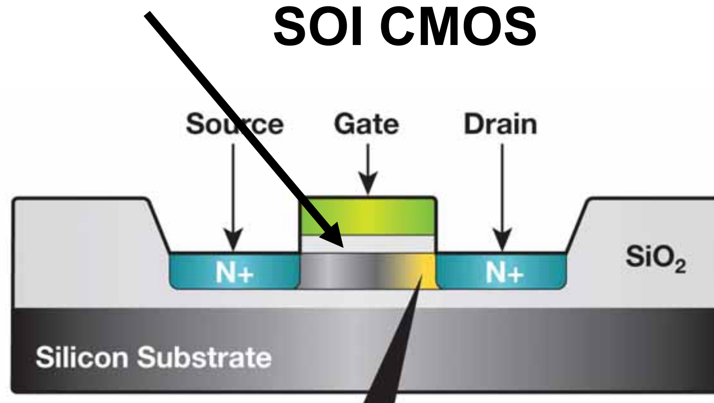
Epitaxial high-k gate dielectrics

- Potential technology for “End-of-ITRS” CMOS Technology

CMOS integration of epitaxial Gd2O3 high-k gate dielectrics

Epi Gate Oxide

SOI CMOS



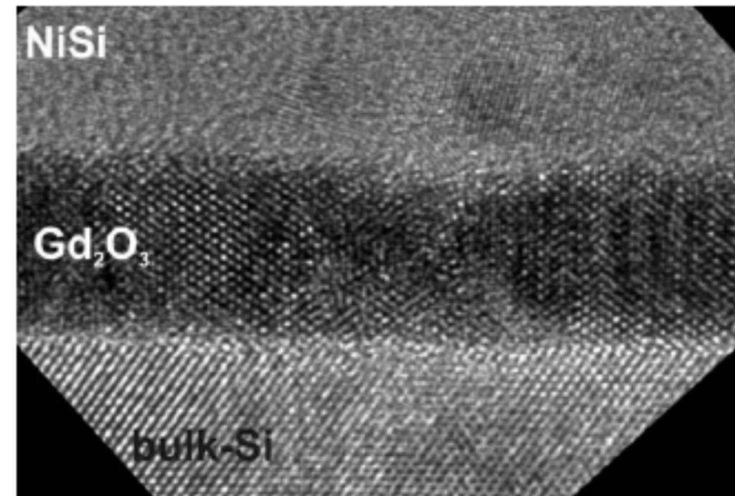


Fig. 3. HRTEM image of a crystalline Gd_2O_3 layer on Si (001) and fully silicided NiSi electrode.

H. Gottlob et al. , Solid State Electronics, 2006

Applications of Epitaxy in the CMOS process

Epitaxial high-k gate dielectrics

- Potential technology for “End-of-ITRS” CMOS Technology

CMOS integration of epitaxial Gd2O3 high-k gate dielectrics

Table 1
Overview of investigated process compatibility with Gd_2O_3 gate dielectric and NiSi or TiN gate electrode

Process step	Compatibility		Comment
	NiSi	TiN	
Acetone	✓	✓	
Propanol	✓	✓	
MF-86 MX (developer)	✓	✓	
TMAH 50 °C	*	✓	* NiSi: not applicable
O_2 Plasma (resist stripping)	✓*	✓	* NiSi: slight change of VFB
UVN-30 (resist)	✓	✓	
H_2SO_4	✓	×*	* Etches TiN
H_2O_2:H_2SO_4 = 1:3	×	×*	* Etches TiN
Forming gas annealing 30 min @ 350 °C in N_2/H_2	?*	✓*	* NiSi: increase of NiSi resistivity * TiN: no effect
RTA 10 s @ 800 °C	×*	✓*	* NiSi: high leakage current * TiN: RTA increases CET
HBr and HBr + Cl_2 RIE	✓	✓	

H. Gottlob et al. , Solid State Electronics, 2006

Summary: Epitaxy

- Definition and Terminology
- Chemical Vapor Deposition (CVD) / Vapor Phase Epitaxy (VPE)
  - Grove Model: Mass-transport vs. Surface Reaction Regime
  - Reactors
  - Chemistry
- Reactor Types
- Applications