Fundamentals of Accelerated Aging of Semiconductor Devices with Power Cycling

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Overview

The reliability of high-power IGBT and MOSFET modules has been studied and presented in a number of scientific investigations [1, 2] and found to depend heavily on thermally-induced stresses in two critical locations within the module:

a) The electrical interconnection of leadframe-to-substrate and wirebonds [3]
b) The thermal pathway comprised of the multi-layer stack substrate of IGBT/MOSFET modules.

The end-of-life due to electrical interconnection failure is an electrically intermittent or disconnected device. The end-of-life due to thermal pathway degradation is excess-junction-temperature device-failure. Yet both types of device failures have their origin in thermally induced mechanical stresses [3] stemming from:

1) Differential thermal expansion of dissimilar materials having non-equal coefficients of thermal expansion (aka., CTE mismatch)
2) Non-uniform temperature profiles leading to stress distributions and warping strain-deformations

Investigation of these phenomena toward the development of reliability models, including failure modes and mechanisms, requires accelerated-aging test data with a sufficient range of parameter variation to delineate the parametric failure dependencies. This essentially encompasses the overall waveform of the accelerated-aging power cycle, expressed in junction temperature excursion including:

i) Minimum junction temperature
ii) Maximum junction temperature
iii) Temporal description of the junction temperature waveform
iv) The device base plate reference temperature

This paper presents the background for reliability testing of power semiconductor devices using accelerated-aging with device power cycling.

Device Aging Caused by Thermally Generated Stresses

All materials exhibit dimensional expansion with higher temperature. This property is expressed in the coefficient of thermal expansion, or "CTE" and is unique for each material. When the temperature distribution within a solid body is non-uniform, higher temperature portions of the mass expand more than lower temperature regions leading to a thermally induced mechanical stress distribution leading to strain-deformation, bending, and warping. The severity of this stress/strain field depends on the degree of thermal non-uniformity. Non-uniform temperature in a solid body inherently means temperature gradients that can only exist with conduction heat flow. This is the condition typically found in the dense heat-flux core of a power module: high heat fluxes, large temperature gradients, and intense thermally induced stress/strain fields. These thermally induced mechanical stresses are termed *thermal gradient stresses*. Generally, the higher the conduction heat flow rate per unit area (heat flux density) within a material, the greater the thermal gradient stresses. Such stresses are generated by thermal gradients even in a homogenous solid having a uniform coefficient of thermal expansion (CTE).

But a power module is comprised of a sandwich of layers, each with a different CTE. This leads to thermally generated stresses at the material boundaries since each side of the interface will expand according to its individual CTE and the local temperature. These stresses are called *CTE-mismatch stresses* and are generated even with uniform temperature distributions at material interfaces where CTE mismatches exist.

Thermally generated stress fields also can vary with time, making them time-dependent from transient to steady-state conditions. For example, the internal thermal stresses generated by constant power dissipation within a device can be dramatically different than those generated by a time-varying power dissipation where the stress distribution will wax and wane with the power dissipation cycle. Higher local rates of change of temperature lead to higher transient thermal gradient stresses in that location within the thermal conduction pathway.

Ultimately, the thermally generated stresses for power cycle accelerated aging depend on:

1) Internal temperature field caused by power dissipation
2) CTE mismatch designed into the device structure
3) Time dependency of power dissipation

Device Aging by Metallurgical and Cyclic Fatigue Mechanisms

Many of the critical thermal interfaces within power modules use some form of solder. It has been observed that the thermal gradient stress and CTE mismatch stresses promote solder fatigue failure leading to the formation and growth of voids and cracks in the solder layers of the main thermal pathway of power modules. Ultimately this degradation of the primary thermal pathway for the device leads to excess-junction-temperature failure.

Considerable amounts of research have been devoted to reliability concerns of soldered interfaces in electronic assemblies. The topic of cyclic solder joint fatigue has been studied for decades since the substantial introduction of surface mount soldering technology. [4-7] Fatigue mechanisms in solder-interfaces are somewhat unique due to the fact that solder is somewhat close to its melting point under normal conditions in electronics applications. This fact means that metallurgical reactions such as creep, grain-growth, and propagation of dislocation-boundaries can occur relatively quickly and are highly temperature dependent. [7] This makes the cyclic fatigue mechanisms of soldered joints critically dependent on both dwell time AND temperature. For example, an accelerated aging temperature cycle on a solder sample from 0 to 120 C with a 6 minute cycle period will have a dramatically different aging impact than one with a 60 minute cycle due to the fact that the progression of these metallurgical reactions are time dependent. In tests using purely mechanical stresses to mimic thermal stresses, the observed solder joint fatigue and failure shows the same sort of stress-versus-dwell time and temperature dependency as with thermally generated stresses. [8]

Lead frames and wirebonds are also subject to debonding/delamination because of the thermally induced stresses generated by temperature gradients and CTE mismatch. Although these are not solder-based structures, the principles of thermally induced cyclic fatigue apply although without the dwell time-dependent creep characteristics of solder.

In summary, thermally induced material fatigue mechanisms depend on

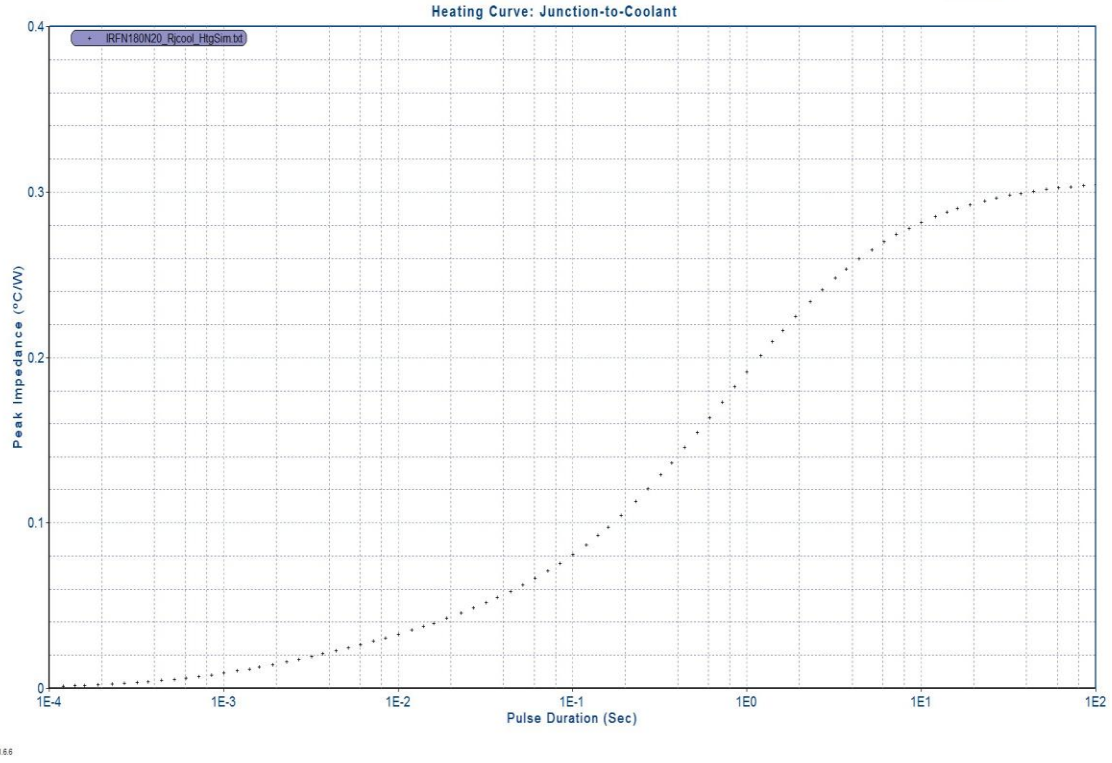
1) Temperature and gradient as a driver of mechanical stresses caused by spatial and temporal non-uniformity as well as CTE mismatch
2) Temperature as a key catalyst of metallurgical reactions, especially in solder
3) Temporal description of the temperature distribution relative to metallurgical reaction times for creep and grain growth in solder
4) Temporal description of the heating power cycle as a driver of transient thermally induced mechanical stresses

Power Cycle Parameter Selection

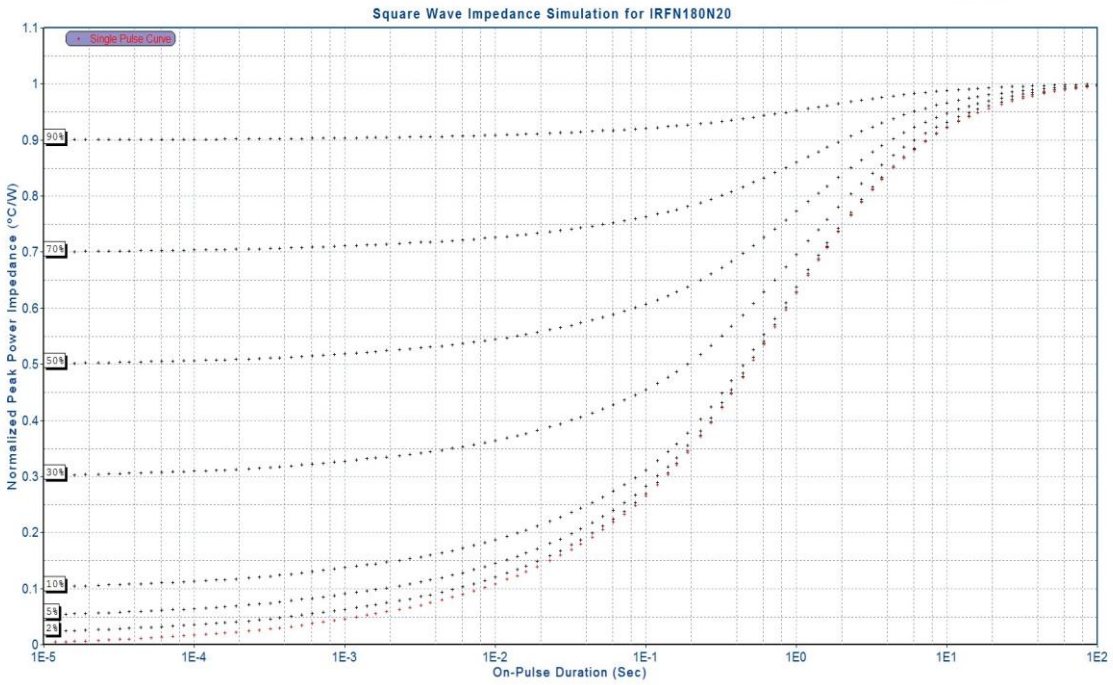
For a particular device, the severity and mechanism of device aging depends heavily on the selection of the fundamental power cycle parameters:

1) Device on-power dissipation
2) The on-power duration (t_{on}) … alternatively: Cycle Period ($t_{on} + t_{off}$)
3) The off-power duration (t_{off}) … alternatively: Duty cycle ($t_{on} / (t_{on} + t_{off})$)

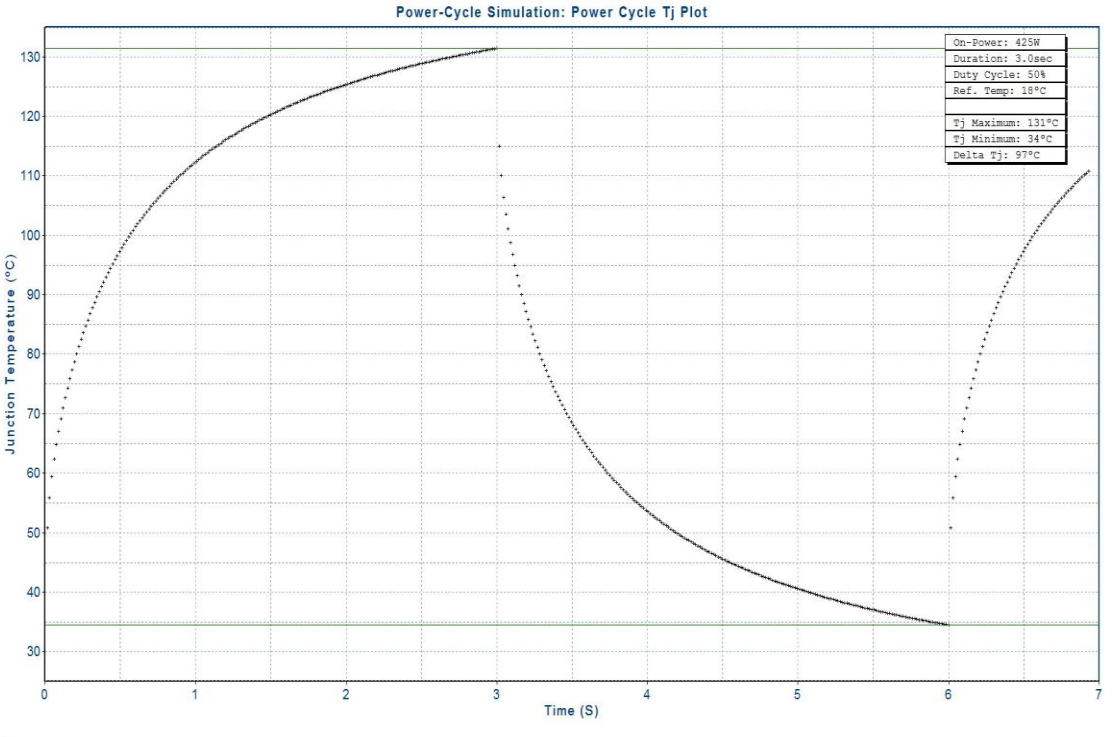
The choice of the on-power duration is significant since it dramatically affects the aging process. The most effective approach to selecting the power cycle parameters is to start with a complete transient thermal characterization of the DUT. A typical cooling curve for the DUT mounted on a liquid cooled heat sink is shown below.



This heating curve is referenced to the coolant temperature, not case temperature, since the coolant is the essential reference for the determination of the device junction temperature. Using a dynamic thermal model that embodies this transient response, the predicted device impedance response to any cyclic heating waveform can be determined and expressed in a plot as a function of the on-power duty cycle.



Once an approximate set of parameters has been determined, the dynamic thermal model can be exercised to predict the actual junction temperature excursion during the proposed power pulse:



Usually the selection of power cycle parameters starts with an approximate target junction temperature range, Tj max and Tj min. Regardless of the chosen target range, as the on-power duration is decreased below the device thermal equilibrium duration, the following apply

a) The heating power must be increased to achieve the desired temperature rise within the reduced heating interval.
b) The increased heating power leads to higher induced mechanical strains.
c) These higher strain levels will be more concentrated closer to the heat source as the distributed heat capacity of the device will buffer the temperature rise in layers further from the die before the reduced-duration heating pulse ends.
d) The solder fatigue aging will be diminished in layers further from the die due to reduced temperature gradient and reduced duration needed for metallurgical degradation of solder.

Generally, these effects mean that decreasing the on-power durations significantly below the device thermal equilibrium duration will tend to focus the cyclic power aging processes more toward the wire bonds and die attachment and away from the thermal pathway comprised of the substrate stack.

The off-power duration selection must allow sufficient passive cooling time for the junction temperature to reach the target minimum junction temperature, Tj minimum, before heating begins at the start of the next cycle.

Once the preliminary selected power cycle parameters have been determined, they can be tested on a device with the actual junction temperatures are measured at the end of on-power and off-power intervals.

Measurements Required During Power Cycling

During power cycling the following parameters should be monitored

1) A contiguous transient evaluation of the device thermal pathway quality
2) The junction temperature measured at the end of the on-power interval
3) The junction temperature measured at the end of the off-power interval
4) The heating power during on-power interval
5) The heat sink temperature

The most sensitive and effective means for evaluation of the device thermal pathway is with a transient power pulse test, also known as “die-attach test”. This test applies a brief (typically 50-200 milliseconds) pulse of heating power into the device and measures the

resulting junction temperature rise, thus providing a highly sensitive measure of the device internal thermal impedance. The brevity of the pulse is chosen to capture the internal package thermal impedance without regard to thermal pathways external to the device under test.

The junction temperature measurements at the ends of the heating and cooling phases of the thermal cycle provide a good indication of the operation of the overall heat sinking from the device-to-cold plate TIM to the coolant.

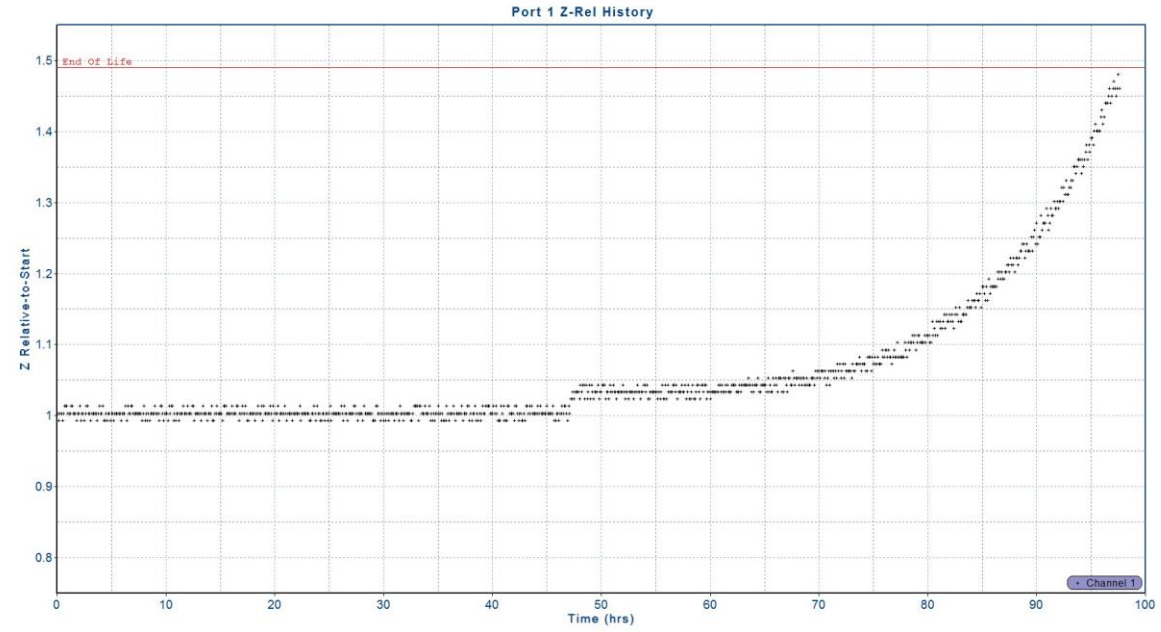
Additionally, the power should be held constant on all devices during the entire aging period. Devices operated in parallel in 3-terminal mode, all with the same applied voltage and balanced heating current is the ideal method to ensure that the power will remain constant and independent of potentially varying device parameters.

When devices are operated in 2-terminal mode by turning the devices fully ON (saturation) at a constant controlled current, the power dissipation will vary with the device temperature since at any given heating current (saturation current), the associated device saturation voltage is temperature dependent. This problem is compounded when devices are tested in series since the entire series string shares the same heating current but each device will exhibit different heating voltage and thus power dissipation that changes with device temperature. Since the hotter device will have a greater power dissipation, aging devices will tend to experience greater power dissipation in response their degraded internal thermal pathways. Parallel, 3-terminal power cycle operation completely avoids this data contamination by maintain the power dissipation constant for all device through the entire evolution of device aging.

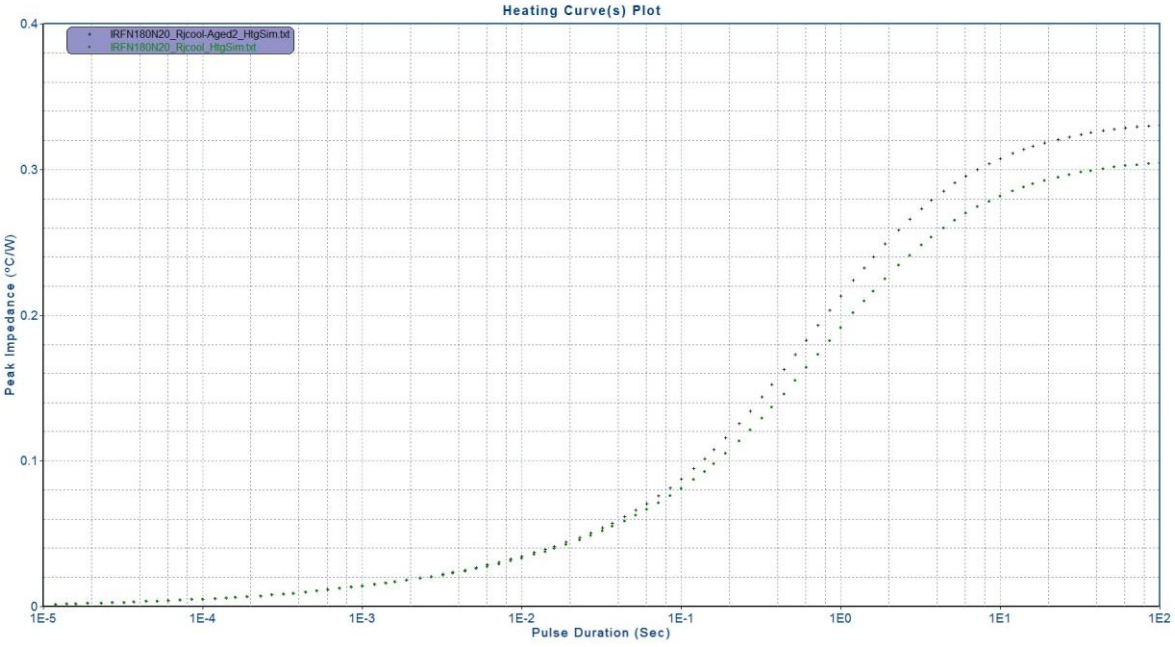
Typical Power Cycle Data

As a typical demonstration test, power cycling was performed on a MOSFET that was cycled at 426 watts, 6 second cycle period, 50% duty cycle. Power pulse testing (aka., die attach testing), was performed every 6 minutes. Thus there were 600 power cycles completed per hour and 10 die attach evaluations per hour. The previous simulation plot of the cyclic junction temperature excursion matched well with the recorded maximum Tj temperature at the end of heating phase of 130.4 C versus 131C predicted and the minimum Tj temperature at the end of cooling phase of 33.1 versus 34C predicted.

Clearly, there is a change in the device internal thermal impedance at about 47 hours. A complete heating characterization was performed at about 75 hours and the resulting heating curve and cumulative structure function plots show that there appears to be a deterioration of the die attachment compared to the initial transient profiles.


Port 1 Z-Rel History
End Of Life
Z Relative-to-Start
Time (hrs)
Channel 1
1.5
1.4
1.3
1.2
1.1
1
0.9
0.8
0
10
20
30
40
50
60
70
80
90
100

v1.7.1


Heating Curve(s) Plot
IRFN180N20_Rjcool-Aged2_HtgSim.txt
IRFN180N20_Rjcool_HtgSim.txt
Peak Impedance (°C/W)
Pulse Duration (Sec)
0.4
0.3
0.2
0.1
0
1E-5
1E-4
1E-3
1E-2
1E-1
1E0
1E1
1E2

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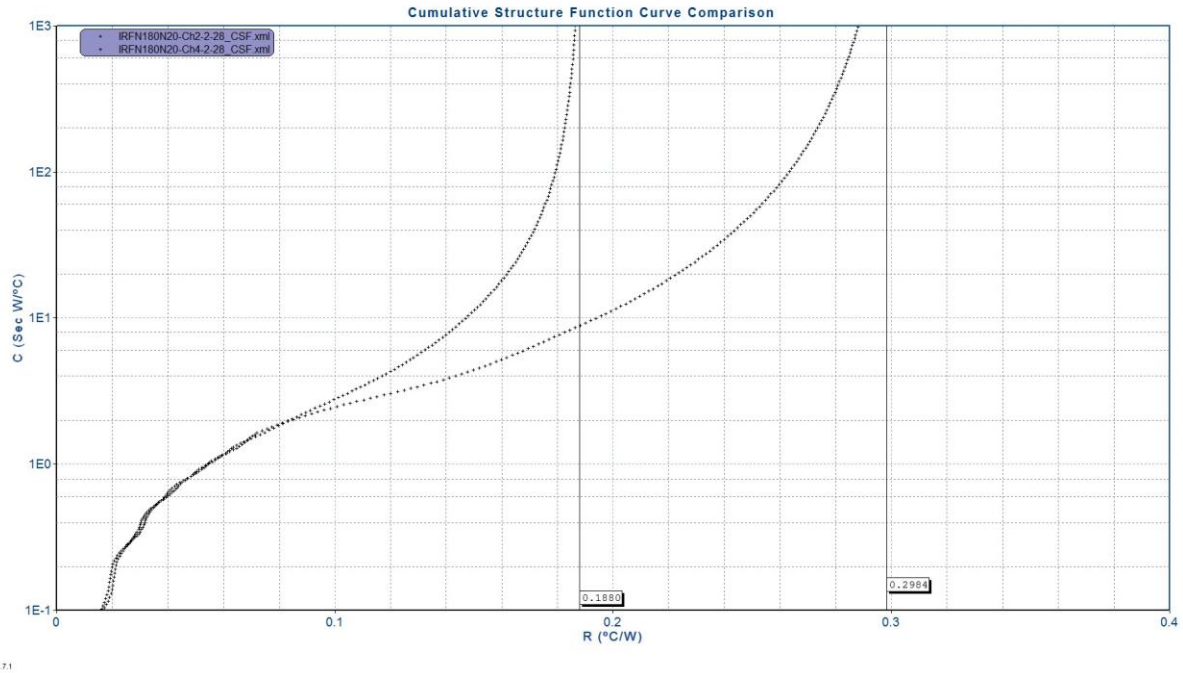

Additional questions on power cycling methodology should be directed to Analysis Tech.

Keywords: accelerated-aging power cycle testing

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[3] Celaya J., Saxena, A., Kulkarni, C.,Saha, S., Goebel, K. “Prognostics Approach for Power MOSFET under Thermal-Stress Aging”, *Reliability and Maintainability Symposium*, 2012, Reno, NV

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