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ELECTROSTATIC DISCHARGE

TRAINING MANUAL

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PUBLISHED BY DIRECTION OF
COMMANDER, NAVAL SEA SYSTEMS COMMAND

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FOREWORD

MANY ELECTRONIC PARTS SUCH AS MICROCIRCUITS, DISCRETE SEMICONDUCTORS, FILM RESISTORS AND CRYSTALS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE (ESD). COMPREHENSIVE ESD CONTROL PROGRAMS ARE REQUIRED TO PROTECT THESE PARTS DURING MANUFACTURE, ASSEMBLY, TEST, REPAIR/REWORK, MAINTENANCE, AND OTHER HANDLING OPERATIONS. SUCH CONTROL PROGRAMS MUST BE IMPLEMENTED THROUGHOUT THE LIFE CYCLE OF THESE ELECTRONIC PARTS. THE INTENT OF THIS TRAINING MANUAL IS TO COMPLEMENT AN ESD AWARENESS TRAINING COURSE WHICH IS A KEY PART OF ANY EFFECTIVE ESD CONTROL PROGRAM.

THIS MANUAL COVERS TOPICS SUCH AS: PRINCIPLES OF STATIC ELECTRICITY, CHARGING AND DISCHARGING, PRIME STATIC GENERATORS, STATIC ELECTRIFICATION OF ELECTRICAL AND ELECTRONIC PARTS, ELEMENTS OF AN ESD CONTROL PROGRAM, ESD PROTECTIVE MATERIALS, ESD PROTECTIVE EQUIPMENT, PACKAGING AND MARKING OF ESDS ITEMS, ESD IN DESIGN, ESD HANDLING PRECAUTIONS AND PROCEDURES, AND MONITORING OF ESD CONTROL PROGRAMS..

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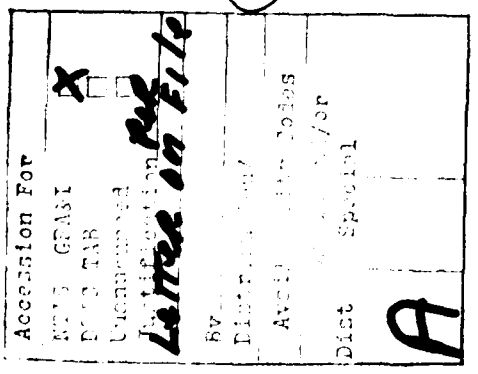

NAVAL SEA SYSTEMS COMMAND
DEPARTMENT OF THE NAVY
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I. INTRODUCTION

A. BACKGROUND

STATIC ELECTRICITY IS FAMILIAR TO US ALL AS LIGHTNING, STATIC CLING OF CLOTHING AND SPARKING WHEN TOUCHING A DOOR KNOB OR OTHER METALLIC OBJECTS IN COOL, DRY WEATHER.

ORDINARY VINYL CLEAN ROOM DRAPERIES CAUSED CONSIDERABLE INTERFERENCE WITH THE MARINER SPACECRAFT RECEIVERS AT JET PROPULSION LABORATORIES IN PASADENA, WHENEVER A PASSING TECHNICIAN BRUSHED HIS BUNNY-SUIT AGAINST THE CLEAR VINYL CURTAIN WHICH FORMED THE WALLS OF THE PORTABLE DOWN-FLOW ROOM IN WHICH THE MARINER WAS ASSEMBLED.

STATIC ELECTRICITY AND THE DIRT IT ATTRACTS CAN CAUSE DATA LOSS IN A COMPUTER. BOTH ARE RESPONSIBLE FOR MAJOR PROBLEMS SUCH AS PRINTER MALFUNCTION, PAPER JAMS, DESTRUCTION OF SENSITIVE LOGIC CIRCUITS AND THE ATTRACTION OF CONTAMINANTS TO READ/WRITE HEADS AND MAGNETIC RECORDING SURFACES. ADDITIONALLY, STATIC CAN PRODUCE NOISE TRANSIENTS IN SYSTEM INTERFACE LINES CAUSING EQUIPMENT MALFUNCTION OR DEGRADATION OF SYSTEM PERFORMANCE. FOR EXAMPLE, IN 1974, STATIC LEVELS AS HIGH AS 17,000 VOLTS WERE DISCHARGED IN THE COMPUTER ROOM AT NEW YORK TELEPHONE AT VARIOUS TIMES OF THE DAY, CAUSING THE IBM 1130 COMPUTING SYSTEM TO BE OUT OF PARITY. THIS OCCURRED ON THE AVERAGE OF FIVE TIMES DAILY RESULTING IN AN ENORMOUS NUMBER OF BILLING ERRORS.

B. ESDS PART FAILURE

STATIC VOLTAGES UP TO AND SOMETIMES EXCEEDING 15,000 VOLTS CAN BE GENERATED BY SIMPLE MOTIONS SUCH AS GETTING UP FROM A CHAIR,

WALKING ACROSS A ROOM, ROCKING IN A CHAIR, RUBBING OF CLOTHING AND THOUSANDS OF OTHER NORMAL, EVERYDAY PERSONNEL MOVEMENTS. SUCH STATIC VOLTAGES CAN DAMAGE ELECTRICAL AND ELECTRONIC COMPONENTS AND DEVICES (PARTS) SUCH AS INTEGRATED CIRCUITS (ICs), DISCRETE SEMICONDUCTORS, THICK AND THIN FILM DEVICES AND CRYSTALS. THE STATIC DANGER TO SOLID STATE SEMICONDUCTORS IS DUE TO THE EXTENSIVE USE OF THIN OXIDE LAYERS (E.G., MOS DEVICES) AND THE MICROMINIATURIZATION OF ACTIVE JUNCTIONS WHICH ARE SEVERELY LIMITED IN THE POWER THEY CAN HANDLE. FILM RESISTORS ARE DAMAGED BY METALLIZATION MELT; CRYSTALS BY MECHANICAL OVERSTRESS IN REACTION TO HIGH ESD VOLTAGE.

THE ESD SENSITIVITY OF PARTS IS BECOMING MORE EVIDENT DURING PRODUCTION, USE, TESTING, AND FAILURE ANALYSIS. THE CONSTRUCTION AND DESIGN FEATURES OF CURRENT MICROTECHNOLOGY HAS RESULTED IN PARTS WHICH CAN BE DAMAGED BY ESD VOLTAGES AS LOW AS 20 VOLTS. THE TREND IN THIS TECHNOLOGY IS TOWARDS GREATER COMPLEXITY AND INCREASED PACKAGING DENSITY; HENCE SMALLER ACTIVE ELEMENTS AND THINNER DIELECTRICS BETWEEN ACTIVE ELEMENTS. THIS RESULTS IN PARTS THAT ARE BECOMING MORE AND MORE SENSITIVE TO ESD.

WHILE CATASTROPHIC FAILURES OF ICs ARE A MAJOR PROBLEM, THEY BECOME OBVIOUS RATHER QUICKLY TO THE EQUIPMENT USER. SUBASSEMBLIES, ASSEMBLIES AND EQUIPMENT CONTAINING THESE ESDS PARTS ARE NORMALLY AS SENSITIVE AND IN SOME CASES MORE SENSITIVE THAN THE PARTS THEMSELVES. FOR EXAMPLE, PRINTED CIRCUIT BOARD RUNS CAN ACT AS ANTENNAS GATHERING GREATER STATIC VOLTAGES ACROSS SENSITIVE PART LEADS THAN SUBJECTING THESE INDIVIDUAL PARTS TO ELECTROSTATIC FIELDS.

C. TRANSIENT UPSET FAILURE

A MORE SUBTLE PROBLEM, HOWEVER, IS THAT OF ELECTROSTATIC DISCHARGES INDUCING NOISE INTO ESDS PARTS OR CIRCUITRY. UNLIKE CATASTROPHIC

FAILURES, THESE SUBTLE FAULTS CAN GO UNDETECTED FOR A CONSIDERABLE PERIOD OF TIME AND, ONCE DETECTED, CAN BE VERY DIFFICULT TO DIAGNOSE. DIGITAL CIRCUITS ARE MUCH MORE SUSCEPTIBLE THAN LINEAR CIRCUITS TO THIS TYPE OF PROBLEM BECAUSE THEIR OPERATION DEPENDS UPON THE RECOGNITION AND PROCESSING OF PULSES. THE PRESENCE OF A STATIC DISCHARGE PULSE-LIKE NOISE SPIKE CAN UPSET THE IC'S LOGIC PROCESS. FOR EXAMPLE, IN AMERICAN TELECOMMUNICATION COMPANY'S AUTOMATIC DIALING EQUIPMENT, STATIC DISCHARGES CAUSED ERASURE OF THE TELEPHONE NUMBERS STORED IN MEMORY.

D. TRANSMITTED FAILURES

SIMILARLY, STATIC DISCHARGES CAUSED COUNTING FAULTS (AND EVENTUAL FAILURE) IN INTERNATIONAL COMPUTING SCALE COMPANY'S COUNTING SCALES. THE PROBLEM WAS RELATED TO THE ELECTROSTATIC CHARGE TRANSMITTED THROUGH THE FRONT-PANEL LEDs TO ITS ASSOCIATED PC BOARD BEHIND THE PANEL CAUSING FAILURE OF SOME BOARD-MOUNTED ICs. MANY PARTS ALTHOUGH NOT SENSITIVE THEMSELVES TO ESD, CAN CONDUCT ESD PULSES THROUGH CIRCUITRY TO ESDS PARTS AND CAUSE THEIR FAILURE.

E. THE ESD PROBLEM

TODAY, ESD CONTROLS ARE NOT WIDELY IMPLEMENTED FOR ELECTRONICS. COMPREHENSIVE ESD CONTROL PROGRAM REQUIREMENTS GENERALLY HAVE NOT BEEN CONTRACTUALLY SPECIFIED TO DATE AND RELATIVELY FEW CONTRACTORS HAVE TAKEN THE INITIATIVE TO IMPLEMENT ESD CONTROL PROGRAMS INTERNALLY AND IMPOSE EFFECTIVE ESD CONTROL REQUIREMENTS ON THEIR SUBCONTRACTORS. WITH THE ADVENT OF DOD-STD-1686 (REFERENCE 1), THIS WILL CHANGE IN THE NEAR FUTURE.

PERHAPS ONE OF THE PRIME CAUSES FOR THE LACK OF IMPLEMENTATION OF ESDS CONTROLS IS THE LACK OF ESD AWARENESS FOR ALL

FUNCTIONS FOR WHICH ESD CONTROLS ARE NECESSARY, SUCH AS: PROGRAM MANAGEMENT, PROCUREMENT, ENGINEERING, MANUFACTURING, PACKAGING, STORAGE, FIELD MAINTENANCE AND QUALITY CONTROL. FEW CONTRACTORS HAVE ESTABLISHED AND IMPLEMENTED INTERNAL ESD TRAINING PROGRAMS FOR THESE FUNCTIONS. ADDITIONALLY, THE HARDWARE, PACKAGING, DRAWINGS OR TECHNICAL MANUALS ARE GENERALLY NOT MARKED SO THAT THE USERS ARE AWARE THAT THE HARDWARE THEY PROCURE, OPERATE AND MAINTAIN IN THE FIELD CONTAIN ESDS ITEMS. LACK OF ESD TRAINING OR AWARENESS IS NOT LIMITED TO INDUSTRY. MILITARY PERSONNEL USING ESDS EQUIPMENT ALSO GENERALLY LACK ESD TRAINING, AND ESD AWARENESS IS SELDOM INCLUDED IN EQUIPMENT TRAINING PROGRAMS CONDUCTED FOR MILITARY PERSONNEL BY CONTRACTORS.

A PRIMARY REASON FOR THE LACK OF ESD AWARENESS TO DATE IS THE LACK OF BASIC TECHNICAL DATA RELATING TO ESD. NUMEROUS PAPERS HAVE BEEN PUBLISHED IN VARIOUS MAGAZINES, PERIODICALS AND SYMPOSIUM PROCEEDINGS. HOWEVER, IT IS DIFFICULT FOR PEOPLE INTERESTED IN ESD TO GATHER ALL THIS INFORMATION AND TO OBTAIN INFORMATION ON ALL ASPECTS OF AN ESD CONTROL PROGRAM FROM RANDOM ARTICLES. ADDITIONALLY, THERE ARE NUMEROUS AREAS RELATING TO ESD FOR WHICH FEW ARTICLES HAVE BEEN PUBLISHED AND FOR WHICH CONSIDERABLE RESEARCH IS REQUIRED.

ESD IS NOT TAUGHT IN COLLEGE COURSES AND FEW BOOKS HAVE BEEN WRITTEN ON THE SUBJECT. SYMPOSIUMS LIKE THE ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE (EOS/ESD) ARE METHODS FOR DISSEMINATING INFORMATION ON ESD. HOWEVER, SUCH SYMPOSIUMS ARE NOT ATTENDED BY ENOUGH PEOPLE, ARE TOO INFREQUENT, TOO SHORT, AND OFTEN UNTIMELY, TO PROVIDE ANSWERS TO THE EVERYDAY ESD PROBLEMS PEOPLE ENCOUNTER IN THE FIELD OF ELECTRONICS. A FORMAL CENTRALIZED ESD INFORMATION EXCHANGE IS REQUIRED TO COLLECT ESD DATA, PERFORM ENGINEERING ANALYSIS, AND DISSEMINATE THE LATEST INFORMATION ON

ESD; THE LATEST LISTING OF ESDS PARTS AND THEIR SENSITIVITIES THAT ARE CONSTANTLY CHANGING WITH THE STATE-OF-THE-ART ADVANCEMENTS IN SOLID STATE TECHNOLOGY; AND THE NEW PRODUCTS AND MATERIALS BEING DEVELOPED THAT CAN SOLVE SOME OF THE MORE DIFFICULT PROBLEMS RELATING TO ESD. SUFFICIENT INFORMATION IS SELDOM PUBLISHED ON MATERIALS MARKETED FOR ESD CONTROLS. CHEMICAL AND PHYSICAL CHARACTERISTICS, USEFUL LIFE, STORAGE LIFE, AND KEY ELECTROSTATIC CHARACTERISTICS SUCH AS PROTECTION AGAINST TRIBOELECTRIC GENERATION, ELECTROSTATIC SHIELDING ATTENUATION AND PROTECTION AFFORDED FROM CONTACT WITH CHARGED PERSONS OR OBJECTS ARE SELDOM PROVIDED BY THE MATERIAL MANUFACTURERS. THIS MAY IN PART BE DUE TO THE LACK OF FORMAL TEST MATERIALS AND STANDARD SPECIFICATION REQUIREMENTS FOR SUCH MATERIALS.

ANOTHER BASIC PROBLEM IS THAT FAILURES ARE OFTEN NOT RECOGNIZED AS RELATED TO ESD. FAILURES CAUSED BY ESD ARE OFTEN ANALYZED AS ELECTRICAL OVERSTRESS FAILURES AND BLAMED ON POWER LINE TRANSIENTS OR TECHNICIANS IMPROPERLY HOOKING UP, PROBING OR TESTING AN ASSEMBLY WITH TOO HIGH A VOLTAGE. OTHER FAILURES CAUSED BY ESD ARE OFTEN CATEGORIZED AS RANDOM, UNKNOWN, INFANT MORTALITY, OR MANUFACTURING DEFECT DUE TO THE LACK OR DEPTH OF FAILURE ANALYSIS PERFORMED. A MAJOR REASON FOR THE ABOVE IS THAT FEW FAILURE ANALYSIS LABORATORIES ARE EQUIPPED WITH SCANNING ELECTRON MICROSCOPES OR OTHER EQUIPMENT AND TECHNOLOGY REQUIRED TO TRACE FAILURES TO ESD. ALSO, ESD CAUSED FAILURES CAN OFTEN BE OVERLOOKED IF THE FAILURE ANALYSIS TECHNICIANS ARE NOT PROPERLY TRAINED. MANY MANUFACTURERS OF ELECTRONIC EQUIPMENT CONTAINING ESDS PARTS ACCEPT A PERCENTAGE OF PART FAILURES AS NORMAL PRODUCTION FALLOUT WHEN MANY MAY BE CAUSED BY ESD. THE USER IN THE FIELD OFTEN ACCEPTS THE HIGHER OPERATIONAL FAILURE RATES OF EQUIPMENT CONTAINING ESDS ITEMS AS NORMAL AND INSTEAD OF INVESTIGATING THE CAUSE OF THE HIGH NUMBER OF FAILURES SIMPLY PROCURES GREATER QUANTITIES OF SPARES.

LACK OF ESD AWARENESS OFTEN RESULTS IN PERSONNEL LIMITING ESD HANDLING PRECAUTIONS TO THE MOST NOTORIOUS ESDS PARTS (E.G., METAL OXIDE SEMICONDUCTORS (MOSs)) WITHOUT KNOWING THAT FAILURES OF NUMEROUS OTHER PARTS ARE BEING CAUSED BY ESD. THE LACK OF ESD AWARENESS ALSO CONTRIBUTES TO THE FALSE SENSE OF SECURITY THAT AN ESDS PART CONTAINING BUIT-IN PROTECTIVE CIRCUITRY IS COMPLETELY PROTECTED FROM ESD, NOT KNOWING THAT MOST PROTECTIVE CIRCUITRY NORMALLY DECREASES SENSITIVITY BY ONLY SEVERAL HUNDRED VOLTS. ESD CAN RESULT IN LATENT DEFECTS WHERE THE ITEM WILL OPERATE WITHIN SPECIFICATION LIMITS DURING TEST, BUT WILL FAIL AFTER BEING DELIVERED TO THE USER. IN ALL OF THE ABOVE INSTANCES, ESD AS A CAUSE OF FAILURE IS NOT ALWAYS RECOGNIZED AND HENCE ESD CONTROL MEASURES ARE NOT IMPLEMENTED.

RECOGNIZING THESE PROBLEMS, THE NAVAL SEA SYSTEMS COMMAND HAS DEVELOPED DOD-STD-1686 FOR DEFINING ESD CONTROL PROGRAM REQUIREMENTS AND DOD-HDBK-263 TO PROVIDE GUIDELINES FOR IMPLEMENTING THESE REQUIREMENTS.

F. ESTABLISHED ESD CONTROL PROGRAM REQUIREMENTS

ESD CONTROL PROGRAM REQUIREMENTS ARE NOT COMPLETELY NEW. MANY ESTABLISHED MILITARY SPECIFICATIONS AND STANDARDS COMMONLY IMPOSED ON EQUIPMENT MANUFACTURERS REQUIRE CONTROLS FOR PROTECTION OF ESDS ITEMS. FOR EXAMPLE, MIL-Q-9858 "QUALITY PROGRAM REQUIREMENTS" (REFERENCE 2) REQUIRES THAT WORK INSTRUCTIONS BE DEVELOPED FOR ALL WORK AFFECTING THE QUALITY OF EQUIPMENT INCLUDING HANDLING, ASSEMBLING, FABRICATING, PROCESSING, INSPECTION, TESTING, MODIFICATIONS, ETC., AND THAT HANDLING, STORAGE, PRESERVATION, PACKAGING AND SHIPPING WORK AND INSPECTION INSTRUCTIONS PROTECT THE QUALITY OF PRODUCTS AND PREVENT LOSS, DETERIORATION OR DEGRADATION OF PRODUCTS.

MIL-STD-785, "RELIABILITY PROGRAM FOR SYSTEMS AND EQUIPMENT DEVELOPMENT AND PRODUCTION" (REFERENCE 3) REQUIRES THE EFFECTS OF PACKAGING, TRANSPORTATION, HANDLING AND MAINTENANCE ON THE RELIABILITY OF THE END PRODUCT BE DETERMINED AND THAT CRITICAL CHARACTERISTICS OF ITEMS THAT DETERIORATE WITH ENVIRONMENTAL CONDITIONS BE IDENTIFIED.

PERHAPS THE STRONGEST ESTABLISHED REQUIREMENTS FOR ESD CONTROLS ARE FOUND IN MIL-STD-882, "SYSTEM SAFETY PROGRAM REQUIREMENTS" (REFERENCE 4) WHICH INCLUDE: IDENTIFICATION OF CRITICAL PATHS, ASSEMBLIES, PRODUCTION TECHNIQUES, ASSEMBLY PROCEDURES, FACILITIES, TESTING AND INSPECTION REQUIREMENTS WHICH MAY AFFECT SAFETY (INCLUDING MATERIAL SAFETY); ENSURE SAFETY WITHIN THE PRODUCTION PROCESS; PROVIDE WARNINGS AND CAUTIONS IN TECHNICAL MANUALS AND PRODUCTION PROCESSES, OPERATION, STORAGE, PACKAGING AND HANDLING; USE DESIGN TECHNIQUES AND SAFETY DEVICES TO MINIMIZE HAZARDS TO SAFETY (INCLUDING MATERIAL SAFETY); ELIMINATION OR CONTROL OF HAZARDS RESULTING FROM ENVIRONMENTAL CONDITIONS INCLUDING SPECIFICALLY: "ELECTROSTATIC DISCHARGE"; INCLUSION OF SAFETY (INCLUDING MATERIAL SAFETY) PROCEDURES IN INSTRUCTORS' LESSON PLANS AND STUDENT EXAMINATIONS FOR THE TRAINING OF ENGINEERS, TECHNICIANS, OPERATING AND MAINTENANCE PERSONNEL AND REQUIREMENTS FOR AN AUDIT PROGRAM TO ENSURE THAT THE OBJECTIVES AND REQUIREMENTS OF THE SAFETY PROGRAM ARE BEING ACCOMPLISHED.

THE ABOVE IS A SMALL SAMPLING OF ESTABLISHED MILITARY DOCUMENTS WHICH REQUIRE SOME OF THE BASIC ELEMENTS OF AN ESD CONTROL PROGRAM THAT ARE COMMONLY IMPOSED UPON DOD CONTRACTORS. A MORE COMPLETE LISTING OF THESE DOCUMENTS AND THEIR REQUIREMENTS PERTAINING TO AN ESD CONTROL PROGRAM ARE SUMMARIZED IN NAVSEA S6000-AB-GTP-010, "MILITARY SPECIFICATIONS, STANDARDS AND CONTRACT CLAUSES SPECIFYING CONTROLS FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGE" (REFERENCE 5).

F. IMPACT OF NOT IMPLEMENTING ESD CONTROLS

THE IMPACT OF NOT IMPLEMENTING EFFECTIVE AND COMPREHENSIVE ESD CONTROLS CAN BE COSTLY TO BOTH THE MANUFACTURER AND THE USER.

ESD FAILURES AT THE MANUFACTURER'S PLANT RESULT IN REPLACEMENT COSTS FOR FAILED PARTS AND REWORK AND REPAIR COSTS IF FAILURES OCCUR AT THE ASSEMBLY LEVEL OR AFTER THE EQUIPMENT ASSEMBLY HAS BEEN COMPLETED. THE HIGHER THE ASSEMBLY LEVEL AT WHICH THE FAILURE OCCURS THE GREATER ARE THE COSTS.

UNSCHEDULED MAINTENANCE RESULTING FROM ESD RELATED FAILURES COULD IMPACT DELIVERY SCHEDULES. THE EQUIPMENT DOWNTIME NEEDED TO EFFECT A REPAIR IS NOT NORMALLY EXCESSIVE FOR ELECTRONIC EQUIPMENT GIVEN THAT SUFFICIENT REPLACEMENT PARTS ARE AVAILABLE. IF A MANUFACTURER DESTROYS HIS INVENTORY OF A SPECIFIC PART DUE TO THE LACK OF ADEQUATE ESD CONTROLS, THE EQUIPMENT COULD BE DOWN FOR A SUBSTANTIAL PERIOD AWAITING PRODUCTION AND DELIVERY OF A REPLACEMENT PART.

IN THE FIELD THE USER NORMALLY ABSORBS THE BURDEN OF THESE COSTS EXCEPT IN INSTANCES WHERE THE MANUFACTURER WARRANTS THE EQUIPMENT. IN EITHER CASE, SUCH COSTS CAN BE SUBSTANTIAL IF THE MANUFACTURER MUST SEND A FIELD ENGINEER TO A USER FACILITY TO EFFECT A REPAIR.

FOR THE USER, EQUIPMENT FAILURES RESULTING FROM ESD CAN REQUIRE INCREASED MAN-LOADING TO KEEP THE EQUIPMENT OPERATIONAL, INCREASED SPARES USAGE, GREATER BURDEN ON THE SUPPLY SYSTEM, AND OTHER LOGISTICS SUPPORT COST INCREASES.

AN INCREASE IN THE NUMBER OF FAILURES MEANS A DECREASE IN EQUIPMENT REALIBILITY, INCREASED DOWNTIME FOR MAINTENANCE AND INCREASED

PROBABILITY OF WAITING FOR A SPARE PART THAT IS NOT ON HAND. THIS DECREASE IN RELIABILITY AND INCREASE IN DOWNTIME MEANS LOWER AVAILABILITY OF THAT EQUIPMENT.

ALL OF THE ABOVE RELATE TO HIGHER LIFE CYCLE COSTS FOR AN EQUIPMENT WHETHER THEIR COSTS BE BORNE BY THE MANUFACTURER OR USER. FOR MILTIARY EQUIPMENT CRITICAL TO COMBAT SITUATIONS THE DECREASED RELIABILITY AND INCREASED DOWNTIME RELATES TO DECREASED MILITARY READINESS AND EFFECTIVENESS.

II. PRINCIPLES OF STATIC ELECTRICITY

A. BACKGROUND

STATIC ELECTRICITY IS THE OLDEST KNOWN FORM OF ELECTRICITY. THE GREEKS WERE ACQUAINTED WITH ELECTRIFICATION OF SUBSTANCES BY FRICTION. IN FACT, THE WORD "ELECTRON" WAS DERIVED FROM THE GREEK WORD "ELEKTRON" THE NAME FOR AMBER. THE TRUE SCIENTIFIC STUDY OF ELECTRICITY BEGAN IN THE SIXTEENTH CENTURY BY WILLIAM GILBERT OF COLCHESTER, ENGLAND, WHO MADE THE FIRST DETAILED STUDY OF THE PROPERTY WHICH SUBSTANCES ACQUIRE AFTER BEING RUBBED WITH SILK, FLANNEL OR FUR (I.E., THE ATTRACTION OF LIGHT OBJECTS). FURTHER STUDIES OF FRICTIONAL ELECTRICITY WERE PERFORMED IN THE EIGHTEENTH CENTURY BY SCIENTISTS IN ENGLAND, GERMANY AND FRANCE WHO ESTABLISHED THAT ALL SUBSTANCES COULD BE ELECTRIFIED BY RUBBING, BUT THAT SOME SUBSTANCES HAD THE POWER OF CONDUCTION AND COULD DIFFUSE THE ELECTRIC CHARGES OVER THEIR SURFACE. DURING THIS PERIOD ELECTRIC MACHINES WERE DESIGNED EMPLOYING SULPHUR OR GLASS BALLS ROTATED BY HAND AND RUBBED ON ANOTHER SUBSTANCE SUCH AS SILK, FLANNEL OR RUBBER. THESE MACHINES WERE CAPABLE OF PRODUCING FAIRLY INTENSE SPARKS. LATER STUDIES BY BENJAMIN FRANKLIN REFERRED TO BODIES AS NEGATIVELY OR POSITIVELY ELECTRIFIED AS THEY EXERTED A FORCE OR REPULSION ON A GLASS ROD RUBBED WITH SILK OR A RESIN STICK RUBBED WITH FLANNEL.

B. TRIBOELECTRIC EFFECT

THE PRIME METHOD OF GENERATING STATIC ELECTRICITY IS BY RUBBING OR SEPARATING MATERIALS, ALSO KNOWN AS TRIBOELECTRIC CHARGING. INVESTIGATIONS HAVE SHOWN THAT MATERIALS CAN BE RANKED IN ACCORDANCE WITH THEIR ABILITY TO BECOME POSITIVELY CHARGED WITH RESPECT TO OTHER MATERIALS DURING TRIBOELECTRIC CHARGING. THIS RANKING IS KNOWN AS A TRIBOELECTRIC SERIES.

A MATERIAL UPPERMOST IN THE SERIES BECOMES POSITIVELY CHARGED WHEN RUBBED WITH A MATERIAL LOWER IN THE SERIES; THE MATERIAL LOWER IN THE SERIES BECOMES NEGATIVELY CHARGED. ONE OF THE MANY VERSIONS OF THE SERIES IS SHOWN IN TABLE II-A. CONDITIONS SUCH AS CLEANLINESS, VARIATION IN CHEMICAL COMPOSITION AND PROCESSES, HUMIDITY AND THE MECHANICS OF RUBBING OR SEPARATION (E.G., SPEED, CONTACT PRESSURE) AFFECT THE SERIES TO A GREAT EXTENT. THUS THE RANKING OF ELEMENTS OR COMPOUNDS IN THE SERIES WILL NOT ALWAYS BE REPRODUCIBLE.

TRIBOELECTRIC GENERATION OF STATIC IS COMMONLY ENCOUNTERED BY PEOPLE WALKING ACROSS A VINYL CARPETED, FINISHED WOOD, SEALED OR PAINTED CONCRETE FLOOR, ESPECIALLY WHEN WEARING SHOES WITH SYNTHETIC SOLES. WAX COMMONLY USED ON WOOD OR VINYL FLOORS NORMALLY ADDS SIGNIFICANTLY TO THIS GENERATION OF STATIC ELECTRICITY. THE CONTACT AND SEPARATION OF THE SHOES FROM THE FLOOR GENERATES THE CHARGE ON THE BOTTOM OF THE SHOES WHICH IN TURN INDUCES A CHARGE ON THE PERSON'S BODY. THE CONTACT, SEPARATION AND RUBBING OF PEOPLE'S CLOTHING AS THEY MOVE THEIR ARMS OR LEGS AND THE SEPARATION OF A PERSON'S CLOTHING FROM A CHAIR SEAT MADE OF SYNTHETIC MATERIALS (E.G., VINYL OR FINISHED WOOD) CAN ALSO GENERATE SUBSTANTIAL ELECTROSTATIC CHARGES ON PERSONNEL. IN GENERAL, ALMOST ALL MOVEMENTS OF PERSONNEL RESULT IN SOME RELATIVE MOTION OF SUBSTANCES IN THE FORM OF RUBBING OR SEPARATION CREATING VARYING LEVELS OF ELECTROSTATIC CHARGE ON THAT PERSON.

TRIBOELECTRIC GENERATION OF STATIC ELECTRICITY IS NOT LIMITED TO PERSONNEL MOVEMENTS. ALL MACHINERY WITH MOVING PARTS, OR EQUIPMENT OPERATION WITH FLOW OF LIQUIDS OR GASES (E.G., PAINT SPRAYERS, FLOW SOLDER MACHINES, DE-GREASERS) CAN ALSO GENERATE SUBSTANTIAL ELECTROSTATIC CHARGES.

ONCE ELECTROSTATIC CHARGES ARE GENERATED BY TRIBOELECTRIC EFFECT OR ANY OTHER CHARGE MECHANISM, AN ELECTROSTATIC FORCE FIELD IS CREATED

TABLE II-A

SAMPLE TRIBOELECTRIC SERIES

POSITIVE	AIR
+	HUMAN HANDS
	ASBESTOS
	RABBIT FUR
	GLASS
	MICA
	HUMAN HAIR
	NYLON
	WOOL
	FUR
	LEAD
	SILK
	ALUMINUM
	PAPER
	COTTON
	STEEL
	WOOD
	AMBER
	SEALING WAX
	HARD RUBBER
	NICKEL, COPPER
	BRASS, COPPER
	GOLD, PLATINUM
	SULFUR
	ACETATE RAYON
	POLYESTER
	CELLULOID
	ORLON
	POLYURETHANE
	POLYETHYLENE
	POLYPROPYLENE
	PVC (VINYL)
	KEL F
NEGATIVE	SILICON
-	TEFLON

BETWEEN THE CHARGED SUBSTANCE AND THE CLOSEST MASS OR GROUND, AND/OR AN OPPOSITELY CHARGED OBJECT. OBJECTS ENTERING THIS ELECTROSTATIC FORCE FIELD WILL BE POLARIZED WITH EQUAL AND OPPOSITE CHARGES ATTRACTED TO THE SURFACES CLOSEST TO THE CHARGED SOURCE AND TERMINATION OF THE FIELD VECTOR (MASS OR GROUND OR ANOTHER OPPOSITELY CHARGED OBJECT IN CLOSE PROXIMITY).

THE ELECTROSTATIC FIELD WILL REMAIN INTACT UNTIL THE CHARGED OBJECT CREATING THE FIELD IS NEUTRALIZED BY SOME FORM OF ESD. THIS ESD CAN OCCUR BY DIRECT DISCHARGE VIA CONTACT WITH AN OPPOSITELY CHARGED OBJECT, BY CONTACT OF THE CHARGED OBJECT WITH A CONDUCTIVE OBJECT OR A GROUND, OR BY SUBJECTING THE CHARGED OBJECT TO IONIZED FLUID FLOW (E.G., FLOW FROM AN AIR IONIZER). THE DISCHARGE BY DIRECT CONTACT CAN BE A SLOW LOW CURRENT DISCHARGE AS OCCURS WHEN THE CHARGED OBJECT COMES IN CONTACT WITH AN OPPOSITELY CHARGED OBJECT, CONDUCTVE MASS OR GROUND HAVING A HIGH CONTACT RESISTANCE THROUGH WHICH THE CHARGES ARE NEUTRALIZED. THE DISCHARGE CAN ALSO BE IN THE FORM OF A HIGH CURRENT SPARK WHICH OCCURS WHEN THE CHARGE DIFFERENTIAL IS SUFFICIENT ENOUGH TO BREAK DOWN THE DIELECTRIC OF THE AIR GAP BETWEEN A CHARGED OBJECT AND A CONDUCTIVE MASS OR A GROUND. ALTERNATELY, A CORONA DISCHARGE COULD OCCUR WHEN THE CHARGE DIFFERENTIAL BETWEEN THE OPPOSITELY CHARGED OBJECTS, OR THE CHARGED OBJECT AND GROUND, IS SUFFICIENT TO IONIZE THE SURROUNDING AIR BUT IS NOT HIGH ENOUGH TO CAUSE DIELECTRIC BREAKDOWN OF THE AIR SPACE.

C. MATHEMATICAL FORMULATION OF ELECTROSTATIC FIELD ANALYSIS

TO HELP AVOID CONDITIONS OR SITUATIONS THAT ARE STATIC GENERATIVE, IT IS IMPORTANT THAT THE CONCEPT OF STATIC ELECTRICITY BE UNDERSTOOD. ONE WAY OF ACHIEVING THIS IS TO START BY DEFINING CERTAIN BASIC CONCEPTS AND MATHEMATICAL RELATIONSHIPS. THESE INVOLVE SUCH QUANTITIES AS THE

ELECTROSTATIC FORCES BETWEEN CHARGED BODIES, THE FIELD STRENGTHS PRODUCED BY CHARGED OBJECTS, ELECTROSTATIC POTENTIAL, CAPACITANCE, "RELAXATION TIME" (THE TIME FOR CHARGES TO BE DISSIPATED), AND THE ELECTRICAL ENERGY OF A SYSTEM COMPRISED OF OPPOSITELY CHARGED OBJECTS, OR A CHARGED OBJECT AND GROUND.

(1) COULOMB'S LAW

THE FORCE OF ATTRACTION OR REPULSION BETWEEN TWO POINT CHARGES IS PROPORTIONAL TO THE MAGNITUDE OF EACH OF THE CHARGES, INVERSELY PROPORTIONAL TO THE SQUARE OF THE DISTANCE BETWEEN THE CHARGES, AND HAS A DIRECTION ALONG THE LINE JOINING THE TWO CHARGES. THE CONSTANT OF PROPORTIONALITY IS BASED UPON THE MEDIUM IN WHICH THE CHARGED OBJECTS ARE CONTAINED. IN TERMS OF A MATHEMATICAL EQUATION AND CONSIDERING THE MEDIUM TO BE AIR, THIS CAN BE EXPRESSED AS:

$$F = K \left(\frac{Q_1 Q_2}{R^2}\right) \quad \text{..... (1)}$$

WHERE:

F = FORCE (NEWTONS)

Q_1 AND Q_2 = MAGNITUDES OF THE CHARGES (COULOMB)

R = DISTANCE BETWEEN CHARGES (METERS)

$K = \frac{1}{4\pi\epsilon_o}$ = THE PROPORTIONALITY CONSTANT 9×10^9 FOR VACUUM (SOMETIMES USED FOR AIR) (METERS/FARADS)

ϵ_o = THE PERMITIVITY OF FREE SPACE (PERFECT VACUUM)

EXAMPLE (A): CONSIDER TWO CHARGED BODIES (FIGURE 2.1) HAVING CHARGES $Q_1 = 5 \times 10^{-5}$ COULOMB AND $Q_2 = 10^{-5}$ COULOMB AND SEPARATED BY A DISTANCE OF 3 METERS. IT IS REQUIRED TO FIND THE FORCE OF REPULSION BETWEEN THE TWO

CHARGED BODIES.

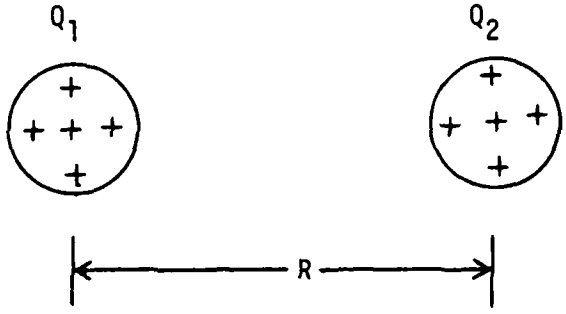


FIGURE 2.1: CHARGED OBJECTS Q_1 AND Q_2 SEPARATED BY A DISTANCE R

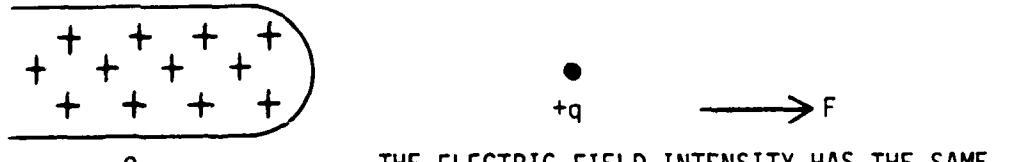
USING RATIONALIZED MKS UNITS IN EQUATION (1), WE HAVE:

$$F = \frac{9 \times 10^9 \times (5 \times 10^{-5})(10^{-5})}{3^2}$$

$$= .5 \text{ NEWTON}$$

(2) ELECTRIC FIELD INTENSITY

AN ELECTRIC FIELD IS SAID TO EXIST AT A POINT IF A FORCE OF ELECTRICAL ORIGIN IS EXERTED ON A CHARGED BODY (+q) PLACED AT THAT POINT (FIGURE 2.2). THE FIELD INTENSITY IS A VECTOR QUANTITY E HAVING BOTH DIRECTION AND MAGNITUDE IN TERMS OF FORCE PER UNIT CHARGE. THUS THE ELECTRIC INTENSITY IN AIR DUE TO CHARGE Q IS GIVEN AS:



THE ELECTRIC FIELD INTENSITY HAS THE SAME DIRECTION AS THE FORCE F ACTING ON A SMALL POSITIVE CHARGE +q

FIGURE 2.2: CALCULATION OF FIELD INTENSITY

$$E = \frac{F}{q} = \frac{1}{4\pi\epsilon_o} \times \frac{Q}{R^2} = \frac{1}{4\pi \times 8.85 \times 10^{-12} \frac{\text{FARAD}}{\text{METER}}} \times \frac{Q \text{ COULOMB}}{R^2 \text{ (METER)}^2}$$

$$= 9 \times 10^9 \frac{Q}{R^2}\left(\frac{\text{COULOMB}}{\text{FARAD . METER}}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

IN PRACTICAL APPLICATIONS, ELECTRIC FIELDS ARE USUALLY PRODUCED BY CHARGES DISTRIBUTED OVER A SURFACE RATHER THAN A POINT SOURCE; HENCE THE VECTOR SUM OF THE CHARGE IS USED TO EXPRESS THE ELECTRIC FIELD.

$$E = K \int A_R \frac{dQ}{R^2}, \text{ A VECTOR SUM} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

WHERE:

R = DISTANCE BETWEEN THE POINT OF INTEREST AND CHARGE (METERS)

A_R = UNIT VECTOR IN THE DIRECTION OF THE FIELD

FOR MANY POINT CHARGES:

$$E = \sum_{i=1}^{n} (K Q_i / R^2) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

E IN A GIVEN DIRECTION X IS:

$$E_X = \sum_{i=1}^{n} (K Q_i / R^2) \cos \theta \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

WHERE:

θ IS THE ANGLE BETWEEN THE ELECTRIC FIELD INTENSITY VECTOR AND THE X DIRECTION.

EXAMPLE (B): IN FIGURE 2.3 LET A AND B REPRESENT THE LOCATION OF TWO CHARGED OBJECTS (E.G., SOLDER IRON, CHARGED BAGS, CHARGED CHAIR, TOTE BOX, ETC.) HAVING CHARGES +5 MICROCOULOMBS (μC) AND -5μC RESPECTIVELY. IT IS REQUIRED TO FIND THE ELECTRIC INTENSITY AT POINT X. THE POINT X COULD BE THE LOCATION OF AN ELECTRONIC PART SENSITIVE TO ELECTROSTATIC FIELD.

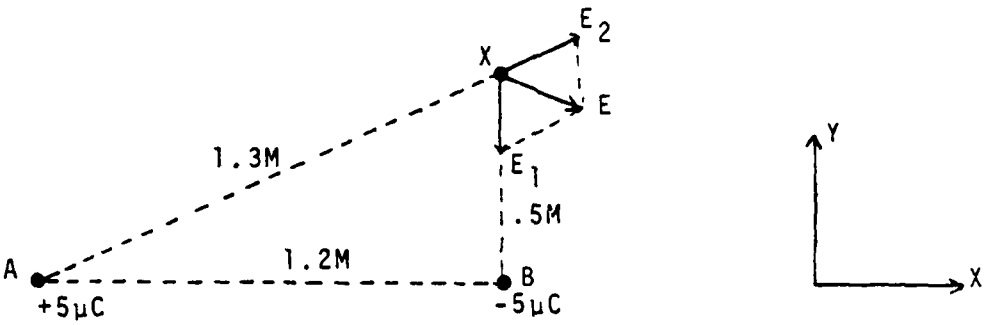


FIGURE 2.3. CALCULATION OF ELECTRIC INTENSITY

USING EQUATION (2), THE ELECTRIC INTENSITY AT X DUE TO -5μ, E_1

$$= \frac{9 \times 10^9 \times 5 \times 10^{-6}}{(.5)^2}$$

$$= 180 \times 10^3 \text{ NEWTON/COULOMB}$$

THE ELECTRIC INTENSITY AT X DUE TO +5μC, E_2

$$= \frac{9 \times 10^9 \times 5 \times 10^{-6}}{(1.3)^2}$$

$$= 27 \times 10^3 \text{ NEWTON/COULOMB}$$

THE COMPONENTS OF THESE VECTORS IN X AND Y DIRECTION ARE AS FOLLOWS:

$$E_{1X} = 180 \times 10^3 \cos 90^\circ$$

$$= 0$$

EXAMPLE (B) (CONTINUED)

$$E_{1Y} = -180 \times 10^3 \text{ SIN } 90^o$$

$$= -180 \times 10^3 \text{ NEWTON/COULOMB}$$

$$E_{2X} = 27 \times 10^3 \text{ COS } (\text{COS}^{-1} \frac{1.2}{1.2})$$

$$= 24.92 \times 10^3 \text{ NEWTON/COULOMB}$$

$$E_{2Y} = 27 \times 10^3 \text{ SIN } (\text{COS}^{-1} \frac{1.2}{1.3})$$

$$= 10.37 \times 10^3 \text{ NEWTON/COULOMB}$$

USING EQUATION (5), THE NET ELECTRIC INTENSITY IN THE X DIRECTION, E_X IS:

$$E_X = E_{1X} + E_{2X} \qquad \text{AND}$$

$$E_{1X} + E_{2X} = 0 + 24.92 \times 10^3$$

$$= 24.92 \times 10^3 \text{ NEWTON/COULOMB}$$

NET ELECTRIC INTENSITY IN THE Y DIRECTION,

$$E_Y = E_{1Y} + E_{2Y} = -180 \times 10^3 + 10.37 \times 10^3$$

$$= -169.63 \times 10^3 \text{ NEWTON/COULOMB}$$

THUS THE RESULTANT ELECTRIC FIELD INTENSITY AT X, E:

$$= \sqrt{E_X^2 + E_Y^2}$$

$$= 171.45 \times 10^3 \text{ NEWTON/COULOMB AT AN ANGLE OF } 8.35^o$$

So what does have to do with "voltage" or power" to damage - need to relate to V/cm - OK as discussed on page

ELECTRIC FIELD BETWEEN OPPOSITELY CHARGED OBJECTS (TWO PLATES OF A CAPACITOR) IS OFTEN EXPRESSED IN TERMS OF POTENTIAL DIFFERENCE BETWEEN THE TWO OBJECTS DIVIDED BY THE DISTANCE BETWEEN THEM.

PARTS SENSITIVE TO ELECTRIC FIELDS CAN BE DAMAGED IF SUBJECTED TO A HIGH ENOUGH ELECTRIC FIELD INTENSITY. MOS PARTS ARE SUCH PARTS BECAUSE OF THEIR VERY THIN (600-1000A^{o}) INSULATING OXIDE (COMMONLY SiO_2) LAYERS. SINCE THE BREAKDOWN VOLTAGE OF SiO_2 IS 6 X 10^6V/CM, A VOLTAGE OF ONLY 60 VOLTS ACROSS 1000A^{o} SiO_2 LAYER OF A MOS PART CAN CAUSE BREAKDOWN AND PART FAILURE.

THE PROTECTION OF ELECTRONIC PARTS FROM ELECTRIC FIELD CAN BE ACHIEVED BY USING A CONDUCTIVE BAG DURING STORAGE, TRANSPORTATION AND HANDLING. THE PRINCIPLE OF THIS TYPE OF PROTECTION CAN BE UNDERSTOOD FROM FIGURE 2.4 WHICH SHOWS A CROSS-SECTION OF A CONDUCTING BAG AND AN INSULATING BAG PLACED IN A UNIFORM ELECTRIC FIELD. NOTE THAT THE ELECTRIC FIELD PASSES THROUGH THE INSULATOR BUT TERMINATES ON THE SURFACE OF THE CONDUCTOR. THIS SHOWS THAT A PART WITHIN AN INSULATOR IS DEFINITELY NOT SHIELDED FROM AN ELECTRIC FIELD, SUCH AS IS GENERATED FROM A CHARGED PERSON. SINCE MANY MATERIALS ARE NOT PURELY CONDUCTIVE (I.E., ZERO RESISTANCE) OR PERFECT INSULATORS (I.E., INFINITE RESISTANCE) MATERIALS PROVIDE PARTIAL SHIELDING FROM ELECTROSTATIC FIELDS DEPENDING UPON THE CONDUCTIVITY OF THE MATERIAL.

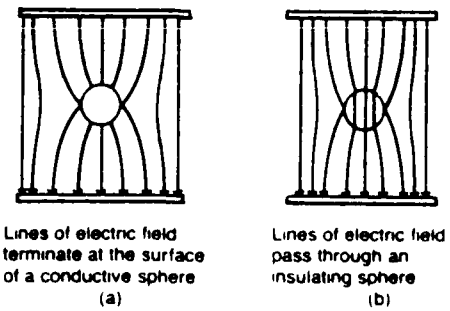


FIGURE 2.4: (A) CONDUCTOR AND (B) INSULATOR IN A UNIFORM ELECTRIC FIELD

(3) ELECTROSTATIC POTENTIAL

IN A REGION IN WHICH THERE IS AN ELECTRIC FIELD, AN ELECTRIC CHARGE EXPERIENCES A FORCE. IF THE CHARGE MOVES FROM ONE POINT (A) TO ANOTHER POINT (B), (FIGURE 2.5), EITHER THE FIELD DOES WORK ON THE CHARGE OR OUTSIDE ENERGY IS REQUIRED TO OVERCOME THE ELECTRICAL FORCES AND TO EFFECT THE MOTION. THE MAGNITUDE OF THIS WORK IS INDEPENDENT OF THE PATH TAKEN FROM A TO B. THUS THE ELECTROSTATIC POTENTIAL BETWEEN A AND B, IN VOLTS, IS A SCALAR QUANTITY DEFINED AS THE WORK IN JOULES PER COULOMB DONE BY THE ELECTRICAL FORCES WHEN A SMALL POSITIVE TEST CHARGE IS MOVED FROM A TO B.

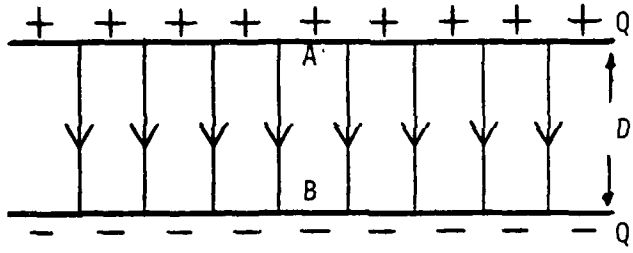


FIGURE 2.5: FIELD BETWEEN TWO CHARGED PLATES

IF A IS AT A HIGHER POTENTIAL THAN B, THE WORK IS POSITIVE AND THE FORCES EXERTED BY THE ELECTRIC FIELD PUSH THE POSITIVE CHARGE DOWN THE POTENTIAL HILL FROM A TO B. IF, ON THE OTHER HAND, THIS WORK IS NEGATIVE, INDICATING THAT OUTSIDE ENERGY MUST BE SUPPLIED TO OVERCOME THE FORCES OF THE ELECTRIC FIELD, A IS SAID TO BE AT A LOWER POTENTIAL THAN B. NOTE THAT DIFFERENCE OF POTENTIAL IS DEFINED IN TERMS OF WORK DONE ON A POSITIVE CHARGE.

CONSIDER THE DIFFERENCE OF POTENTIAL FOR TWO CHARGED PLATES BETWEEN WHICH THERE IS A UNIFORM ELECTRIC FIELD AS SHOWN IN FIGURE 2.5. AT ANY POINT BETWEEN THE PLATES, A SMALL TEST CHARGE +q EXPERIENCES A DOWNWARD ELECTROSTATIC FORCE:

$$F = qE$$

IN THE MOTION FROM A TO B, THIS FORCE DOES WORK:

$$W_{A \rightarrow B} = F.X = qE.X \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

$$= qE.X$$

THE WORK DONE PER COULOMB OF CHARGE IS:

$$W_{A \rightarrow B}/q = E.X$$

WHERE E IS IN NEWTON/COULOMB AND X IS IN METERS, THIS IS EQUIVALENT TO JOULES/COULOMB WHICH, BY DEFINITION, IS THE DIFFERENCE OF POTENTIAL BETWEEN A AND B IN VOLTS. THIS DIFFERENCE OF POTENTIAL IS USUALLY DENOTED BY $V_A - V_B$. THEREFORE,

$$V_A - V_B = EX \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (7)$$

SINCE:

$$1 \text{ VOLT} - 1 \frac{\text{JOULE}}{\text{COULOMB}} = 1 \frac{\text{NEWTON . METER}}{\text{COULOMB}}$$

$$1 \frac{\text{VOLT}}{\text{METER}} = 1 \frac{\text{NEWTON}}{\text{COULOMB}}$$

WHERE VOLT/METER IS USUALLY USED AS THE UNIT OF ELECTRIC INTENSITY AND IS FREQUENTLY CALLED POTENTIAL GRADIENT; OR THE POTENTIAL PER UNIT OF DISTANCE.

(4) MAXIMUM POTENTIAL

IF THE CHARGE ON A BODY WERE ABLE TO BUILD UP INDEFINITELY, THEN THE POTENTIAL WOULD HAVE NO UPPER LIMIT. FORTUNATELY, THIS IS NOT TRUE.

THE MAXIMUM CHARGE THAT CAN BE RETAINED BY AN OBJECT IN AIR IS LIMITED BY THE FACT THAT THE AIR ITSELF BECOMES CONDUCTIVE AT AN ELECTRIC FIELD OF ABOUT 3×10^6 V/M. FOR EXAMPLE, THE MAXIMUM POTENTIAL THAT A METALLIC SPHERICAL BODY IN AIR CAN ACHIEVE IS:

$$V_{MAX} = R\, E_{MAX} \text{ (VOLTS)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (8)$$

$$= R\,(3 \times 10^6) \text{ (VOLTS)}$$

WHERE:

V_{MAX} = MAXIMUM POTENTIAL (VOLTS)

E_{MAX} = MAXIMUM ELECTRIC FIELD (VOLTS/METERS)

R = RADIUS OF THE SPHERE (METER)

EXAMPLE (C): FOR A SPHERE OF 5 CM RADIUS:

$$V_{MAX} = (.05)\,(3 \times 10^6)$$

$$= 150{,}000 \text{ VOLTS}$$

(5) CAPACITANCE

IF TWO CONDUCTIVE PLATES ARE SEPARATED FROM EACH OTHER BY AN INSULATING (DIELECTRIC) MATERIAL, A CAPACITANCE WILL EXIST BETWEEN THEM. ANY OPPOSITE STATIC CHARGE THAT BUILDS UP ON THESE PLATES WILL CHARGE THIS CAPACITOR. A CAPACITOR CAN BE CHARGED BY: (1) ELECTRICALLY SHORTING AND PLACING THESE PLATES IN AN ELECTROSTATIC FIELD (WITH THE PLATES PERPENDICULAR TO THE ELECTRIC FIELD INTENSITY VECTOR) AND REMOVING THE SHORT PRIOR TO

REMOVING THESE PLATES FROM THE ELECTROSTATIC FIELD, (2) BY CHARGING THE PLATES DIRECTLY WITH EQUAL AND OPPOSITE CHARGES, OR (3) BY CHARGING ONE PLATE AND GROUNDING THE OTHER. THE VOLTAGE LEVEL TO WHICH THIS CAPACITOR WILL BE CHARGED IS EQUAL TO:

$$V = \frac{Q}{C} \quad \text{..... (9)}$$

WHERE:

V = VOLTAGE (VOLTS)

Q = CHARGE (COULOMBS)

C = CAPACITANCE (FARADS)

IT CAN BE SEEN THAT THE VOLTAGE ACROSS A CAPACITOR IS DIRECTLY PROPORTIONAL TO ITS STORED CHARGE AND INVERSELY PROPORTIONAL TO ITS CAPACITANCE. THE CAPACITANCE (C) OF THE TWO CHARGED PLATES OF OVERLAPPING AREA (A) (SQUARE METERS) SEPARATED BY A DIELECTRIC OF THICKNESS (D) IN METERS IS EQUAL TO:

$$C = \varepsilon_o \varepsilon_r \frac{A}{D} \text{ (FARADS)} \quad \text{..... (10)}$$

$$= 8.85 \varepsilon_r \frac{A}{D} 10^{-12} \text{ (FARADS)}$$

WHERE:

ε_r IS THE RELATIVE PERMITIVITY OF THE DIELECTRIC

ε_o IS THE PERMITIVITY OF FREE SPACE = $1/(36\pi \times 10^9)$ FARADS/METERS (RATIONALIZED MKS UNITS)

EXAMPLE (D): LET THE TWO PLATES OF A MOS CAPACITOR BE SEPARATED BY A DISTANCE OF 1000Å OF SiO_2 (ε_r = 10) WITH 5 MILLIMETERS^2 AS THE AREA OF THE SMALLER ONE. IT IS REQUIRED TO FIND THE CAPACITANCE OF THIS MOS PART AND THE CHARGE ON EITHER PLATE WHEN THE DIFFERENCE OF POTENTIAL BETWEEN THE PLATES IS 100V. USING EQUATION (10), THE CAPACITANCE (C) IS:

$$C = 8.85\ (10)\ \frac{5 \times 10^{-6}}{10^{3} \times 10^{-10}} \times 10^{-12}\ \text{FARAD}$$

$$= 4425\ \mu\mu f$$

USING EQUATION (9), THE CHARGE ON EACH PLATE Q IS:

$$Q = VC$$

$$= 100 \times 4425 \times 10^{-12}\ \text{COULOMB}$$

$$= .4425\ \mu C$$

(6) *DIELECTRIC STRENGTH*

THE REASON FOR USING A DIELECTRIC BETWEEN THE PLATES IS NOT SOLELY FOR MECHANICAL CONVENIENCE. A DIELECTRIC IMPROVES THE CAPACITOR ELECTRICALLY IN TWO WAYS: (1) IT INCREASES THE CAPACITANCE, AND (2) IT PERMITS THE USE OF HIGHER VOLTAGES WITHOUT DANGER OF BREAKDOWN OR FLASHOVER BETWEEN THE CAPACITOR PLATES. BREAKDOWN IS RELATED TO A PROPERTY OF A DIELECTRIC CALLED DIELECTRIC STRENGTH. THE DIELECTRIC STRENGTH OF A MATERIAL IS THE MAXIMUM POTENTIAL GRADIENT (VOLTS/METERS) THAT THE MATERIAL CAN WITHSTAND WITHOUT RUPTURE. DIELECTRIC STRENGTH MUST NOT BE CONFUSED WITH DIELECTRIC CONSTANT. THE DIELECTRIC CONSTANT OF A MATERIAL IS THE RATIO OF

THE CAPACITANCE OF A CAPACITOR WITH A GIVEN DIELECTRIC MATERIAL BETWEEN THE PLATES TO THE CAPACITANCE OF A CAPACITOR WITH VACUUM BETWEEN THE PLATES. THE DIELECTRIC CONSTANT DETERMINES HOW MUCH CHARGE A GIVEN CAPACITOR WILL STORE WITH A GIVEN POTENTIAL DIFFERENCE; DIELECTRIC STRENGTH DETERMINES HOW MUCH VOLTAGE THIS CAPACITOR WILL STAND WITHOUT BREAKING DOWN.

EXAMPLE (E): THE DIELECTRIC STRENGTH OF THERMAL SiO_2 IS IN THE RANGE OF 5-8 X 10^6V/CM. IF WE ASSUME THE DIELECTRIC STRENGTH OF THE SiO_2 USED IN THE MOS DEVICE OF EXAMPLE (C) TO BE 6 X 10^6V/CM, THEN A 1000$\mathring{A}$ LAYER WILL FAIL AT A VOLTAGE OF ONLY 60 VOLTS AS CALCULATED BELOW:

$$\text{MAXIMUM VOLTAGE TO BREAKDOWN} = 6 \times 10^6 \frac{V}{CM} \times 1000 \times 10^{-8} \text{ CM}$$

$$\approx 60V$$

THUS FOR A 5 MILLIMETER^2 CAPACITOR (SEE EXAMPLE (D), A Q OF .4425 μC ON EITHER PLATE CORRESPONDING TO THE POTENTIAL DIFFERENCE BETWEEN THE PLATES OF 100 VOLTS WILL DAMAGE THE DEVICE VIA DIELECTRIC BREAKDOWN.

(7) TYPICAL EXAMPLES OF A CAPACITOR

TYPICAL EXAMPLES OF CAPACITORS ENCOUNTERED IN THE FIELD OF ELECTRONICS ARE HUMANS, TOTE BOXES (AND OTHER CONTAINERS, TRAYS, ETC.) AND ELECTRONIC PARTS.

(a) HUMAN CAPACITANCE

THE HUMAN CAPACITANCE C_H IS DIVIDED INTO TWO MAJOR PARTS: THE PARALLEL PLATE CAPACITANCE OF THE SOLES OF THE FEET TO GROUND, AND CAPACITANCE OF THE BODY BULK TO GROUND. THE CAPACITANCE OF A PERSON IS

A FUNCTION OF HIS PROXIMITY TO OTHER OBJECTS. THIS CAPACITANCE CAN CHANGE SIGNIFICANTLY DURING SIMPLE MOVEMENTS SUCH AS LEANING FORWARD IN A CHAIR, PICKING UP ONE OR BOTH FEET FROM THE FLOOR, OR STANDING UP, AS IS SHOWN IN TABLE II-B. HUMAN CAPACITANCE CAN VARY FROM 50 TO SEVERAL THOUSAND PICO-FARADS (PF).

TABLE II-B (REFERENCE 6)

CAPACITANCE CHANGES IN PERSONNEL IN A WORK AREA

DESCRIPTION OF MOVEMENT	% CHANGE IN CAPACITANCE DUE TO MOVEMENT		
	INITIAL CAPACITANCE	FINAL CAPACITANCE	% CHANGE
PERSON SEATED, RAISING ONE FOOT	192	163	15% DECREASE
PERSON SEATED, PICKING UP BOTH FEET AND PLACING THEM ON THE FOOT REST	192	129	33% DECREASE
PERSON SEATED, LEANING FORWARDS IN CHAIR (DESK TYPE CHAIR WITH BACK)	192	184	4% DECREASE
STANDING PERSON RAISING ONE FOOT	167	141	16% DECREASE
SEATED PERSON STANDING UP	192	167	13% DECREASE

(b) CONDUCTIVE TOTE BOX CAPACITANCE

CONDUCTIVE TOTE BOXES HAVE BEEN FOUND TO VARY IN CAPACITANCE FROM 35-300 PF DEPENDING ON THEIR SIZE AND SHAPE. A TYPICAL VALUE OF THE CAPACITANCE OF A TOTE BOX TO GROUND PLANE (17 CM WIDE, 24 CM LONG AND 15 CM HIGH) IS 138 PF. THE EFFECT OF THIS CAPACITANCE TO THE DISCHARGE OF CONDUCTIVE TOTE BOX TO GROUND IS DISCUSSED IN REFERENCE 6.

(c) MOS CAPACITOR

THE CAPACITANCE BETWEEN THE METAL GATE AND SEMICONDUCTOR

OF A MOS FIELD EFFECT TRANSISTOR (FET) WITH SiO_2 AS THE DIELECTRIC FORMS ANOTHER TYPE OF CAPACITOR COMMON IN MANY INTEGRATED CIRCUITS.

(d) REVERSE BIASED P-N JUNCTION

THE DEPLETION LAYER OF THE REVERSE BIASED P-N JUNCTION DIODE CONSTITUTES A VOLTAGE DEPENDENT CAPACITOR, POPULARLY KNOWN AS A VARACTOR.

(8) ENERGY STORAGE

ASSUME THE SYSTEM WHERE THE CAPACITANCE (C) IS UNCHARGED AND HENCE HAS ZERO POTENTIAL DIFFERENCE BETWEEN ITS PLATES. LET US ALSO ASSUME THAT THERE IS NO DISSIPATIVE ELEMENTS IN THE STORAGE SYSTEM AND THAT THE STORED ENERGY W IS A FUNCTION OF SOME POSITION VARIABLE (E.G., PLATE SEPARATION X) AND THE CHARGE Q. SINCE THE CAPACITOR IS INITIALLY UNCHARGED, AND SINCE NO ELECTRICAL FORCES ARE INVOLVED IN PUTTING IT TOGETHER MECHANICALLY, THE CHANGE IN ENERGY dW AS CHARGE IS MOVED FROM ONE PLATE TO THE OTHER IS:

$$dW = VdQ \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (11)$$

WHERE V (VOLTS) IS THE POTENTIAL THROUGH WHICH THE CHARGE dQ MOVES IN BEING CARRIED FROM ONE PLATE TO THE OTHER. IF WE BEGIN WITH THE UNCHARGED SYSTEM AND CHARGE IT TO A POTENTIAL V BY TRANSFERRING A CHARGE Q (COULOMBS), AN EXTERNAL SOURCE MUST ADD W (JOULES) ENERGY TO THE SYSTEM WHERE:

$$W = \int_0^Q V \, dQ \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (12)$$

BUT AS BEFORE V = Q/C, WHICH MEANS THAT:

$$W = \int_0^Q \frac{Q\,dQ}{C} = \frac{1}{2}\frac{Q^2}{C} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (13)$$

FOR THE ENERGY STORED IN THE CAPACITOR. EXPRESSING ENERGY FUNCTION IN TERMS OF POTENTIAL (V) IN VOLTS AND (C) IN FARADS:

$$W = \frac{1}{2}\ CV^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (14)$$

EXAMPLE (F): CONSIDER A PERSON TOUCHING A CHARGED OBJECT THAT HAS A POTENTIAL OF (V) VOLTS AND ENOUGH CHARGE (Q) TO FULLY CHARGE THAT PERSON'S CAPACITANCE (C_H). THE AMOUNT OF CHARGE WOULD BE:

$$Q = C_H V \text{ COULOMBS}$$

$$= 100 \times 10^{-12} V \text{ (COULOMB)}, \text{ FOR C = 100 PF}$$

IF THAT CHARGE SOURCE IS OF 1000 VOLTS, THE TOTAL ENERGY (E) ABSORBED BY THAT PERSON WOULD BE:

$$W = \frac{1}{2}\ CV^2 \text{ JOULES}$$

$$= (.5)\ (100 \times 10^{-12}) \times (10^3)^2$$

$$= 50 \quad \text{JOULES}$$

SINCE:

$$CV = Q$$

$$W = \frac{1}{2}\ QV$$

IF THAT PERSON'S CAPACITANCE IS HALVED (AS BY LIFTING ONE FOOT OFF THE GROUND AFTER BEING CHARGED (CHARGE REMAINING CONSTANT), THE VOLTAGE AND THE ENERGY

WOULD BE DOUBLED. THIS SAME LINEAR RELATIONSHIP EXISTS FOR OTHER INCREASE IN VOLTAGES WITH A CORRESPONDING DECREASE IN CAPACITANCE (I.E., CONSTANT Q).

VARIOUS STUDIES HAVE SHOWN THAT SEMICONDUCTOR PARTS CAN BE DEGRADED BY A SINGLE VERY SHORT LOW ENERGY PULSE CHARACTERISTIC OF AN ELECTROSTATIC DISCHARGE. ESPECIALLY MOS INTEGRATED CIRCUITS, BIPOLAR INTEGRATED CIRCUITS WITH EXTREMELY SMALL GEOMETRIES AND MINIATURE FILM RESISTORS OF HIGH SHEET RESISTIVITY CAN BE DAMAGED BY AS LITTLE AS 3 PICOJOULES OF STATIC ENERGY.

III. CHARGING AND DISCHARGING

A. INTRODUCTION

THERE ARE MANY WAYS TO DEVELOP A STATIC CHARGE. CONTACT CHARGING, TRIBOELECTRIC CHARGING (A FORM OF CONTACT CHARGING), INDUCTION CHARGING, CHARGING BY FREEZING, ION AND ELECTRON BEAM CHARGING, AND SPRAY CHARGING ARE A FEW OF THE MOST COMMON METHODS AND MOST APPLICABLE TO ESD. IN THE ELECTRONICS INDUSTRY, STATIC CHARGING CAN POSE A SERIOUS PROBLEM IN MANY AREAS. IF THE MECHANISMS OF CHARGING ARE UNDERSTOOD, ONE IS BETTER EQUIPPED TO AVOID SITUATIONS WHICH ARE SUSCEPTIBLE TO THE HAZARDS OF STATIC CHARGES. ALSO, THE ASSEMBLY, REPAIR AND OTHER PERSONNEL WHO HANDLE ESDS ITEMS WILL BECOME MORE AWARE OF THE METHODS TO CONTROL STATIC TO SAFE LEVELS. IN THE NEXT FEW SECTIONS THESE COMMON MECHANISMS OF CHARGING ARE DISCUSSED IN DETAIL.

ALSO DISCUSSED ARE THE MECHANISMS OF "BLEEDING-OFF" STATIC CHARGES. CHARGED SUBSTANCES ACT AS CAPACITORS WITH THE CHARGED SURFACE OF THE CHARGED OBJECT ACTING AS ONE PLATE OF THE CAPACITOR, AIR OR OTHER INSULATORS AS THE DIELECTRIC AND A NEARBY CONDUCTIVE MASS OR GROUND ACTING AS THE SECOND CAPACITOR PLATE. FOR EXAMPLE, A CHARGED PERSON HAS A CAPACITANCE RELATIVE TO GROUND WITH THE DIELECTRIC BEING THE PERSON'S SHOE SOLES AND PERHAPS THE FLOOR. THE GROUND FORMS THE SECOND CAPACITOR PLATE. THEREFORE, THE PHENOMENA OF ELECTROSTATIC DISCHARGE IS SIMILAR TO THE DISCHARGE OF A CAPACITOR CHARGED TO SOME ELECTROSTATIC VOLTAGE POTENTIAL, USUALLY DISCHARGED THROUGH A RESISTANCE SUCH AS THE HUMAN BODY BULK AND SKIN CONTACT RESISTANCE, WORK TABLE TOP RESISTANCE, AND/OR THE RESISTANCE OF AN ELECTRONIC PART. THE TIME CONSTANT OF THIS RESISTANCE-CAPACITANCE (RC) CIRCUIT IS OF PRIME IMPORTANCE IN DETERMINING THE DECAY RATE OF THE DISCHARGE. A MATHEMATICAL

FORMULATION OF THIS SITUATION ALONG WITH A NUMBER OF NUMERICAL EXAMPLES ARE CITED AT THE END OF THIS SECTION.

(1) CONTACT CHARGING

THE CONCEPT OF CONTACT CHARGING WILL BE BETTER UNDERSTOOD IF WE START WITH THE ENERGY-LEVEL DIAGRAM REPRESENTATION OF A MATERIAL. AN ENERGY-LEVEL DIAGRAM FOR THE ELECTRONS IN A METAL INDICATES THE ENERGY STATES OF THE ELECTRONS WITH RESPECT TO A REFERENCE LEVEL OUTSIDE THE METAL (THE "VACUUM" ENERGY LEVEL). A TYPICAL ENERGY-LEVEL DIAGRAM FOR A METAL IS SHOWN IN FIGURE 3.1. E_C AND E_V ARE THE EDGES OF THE CONDUCTION BAND AND VALENCE BAND RESPECTIVELY WHERE ELECTRONS AND HOLES (ABSENCE OF ELECTRONS) CAN MOVE IN A CRYSTAL STRUCTURE.

(a) VALENCE BAND

THE OUTERMOST ELECTRONS ORBITING AROUND THE NUCLEUS OF AN ATOM ARE CALLED VALENCE ELECTRONS. ALSO EACH ELECTRON HAS ITS OWN ENERGY STATE DIFFERENT FROM THAT OF ANOTHER ELECTRON (PAULI EXCLUSION PRINCIPLE). THUS THE VALENCE ELECTRONS OCCUPY A BAND OF ENERGY LEVELS, INSTEAD OF A SINGLE ENERGY LEVEL (STATE). THIS ENERGY BAND IS CALLED THE VALENCE BAND.

(b) CONDUCTION BAND

THE CONDUCTION BAND IS A PARTIALLY FILLED ENERGY BAND IN WHICH ELECTRONS MOVE FREELY ALLOWING AN ELECTRIC CURRENT TO FLOW THROUGH THE MATERIAL.

THE VALENCE BAND AND THE CONDUCTION BAND ARE NORMALLY SEPARATED BY A FORBIDDEN ENERGY GAP (E_G) (FIGURE 3.1) WHERE ELECTRONS DO NOT EXIST. THE CONDUCTIVITY OF A MATERIAL DEPENDS ON THE NUMBER OF ELECTRONS IN THE CONDUCTION BAND AND THE NUMBER OF HOLES IN THE VALENCE BAND. FOR A VALENCE ELECTRON TO BECOME A CONDUCTION ELECTRON, A MINIMUM ENERGY EQUAL TO

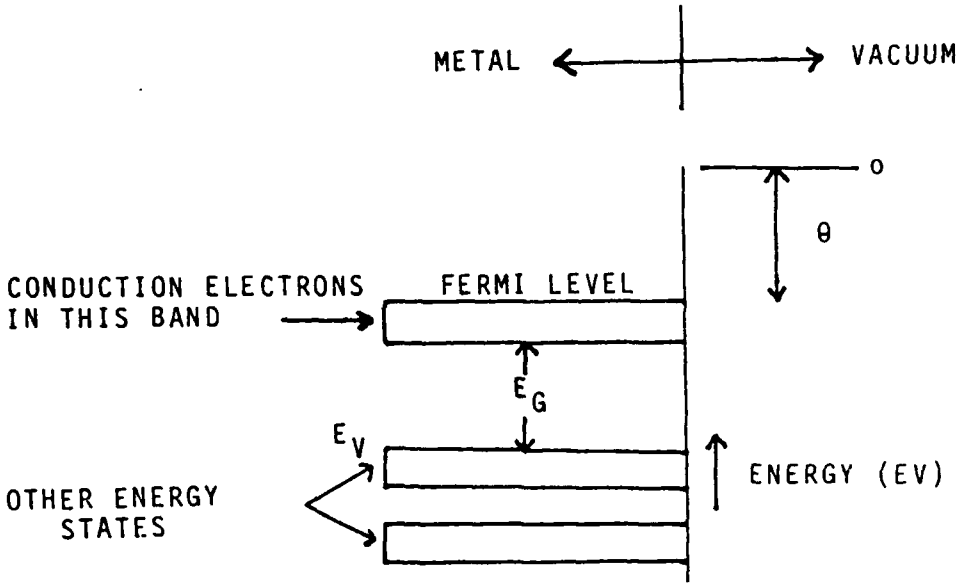


FIGURE 3.1: TYPICAL ENERGY-LEVEL DIAGRAM FOR A METAL
(REFERENCE 7)

THE FORBIDDEN GAP ENERGY HAS TO BE SUPPLIED TO THAT ELECTRON.

THE FERMI LEVEL INDICATED IN FIGURE 3.1 IS INSIDF THE CONDUCTION BAND. THIS CONCEPT IS TRUE ONLY FOR METALS AND HEAVILY DOPED SEMICONDUCTORS. IN MODERATELY DOPED AND UNDOPED (INTRINISIC) SEMICONDUCTORS THE FERMI LEVEL IS WITHIN THE BAND GAP OF THE MATERIAL REPRESENTED BY E_G OF FIGURE 3.1. THE CONCEPT OF FERMI-LEVEL CAN BE ILLUSTRATED FROM THE FERMI-DIRAC DISTRIBUTION FUNCTION, F(E), WHICH IS ACTUALLY THE ENERGY DISTRIBUTION FUNCTION FOR THE ELECTRONS. THE FERMI-DIRAC DISTRIBUTION FUNCTION IS WRITTEN AS FOLLOWS:

$$F(E) = \frac{1}{1 + EXP\ (E-E_F)/KT} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (15)$$

WHERE:

E = ENERGY OF DESIRED ENERGY LEVEL

E_F = THE FERMI ENERGY, THE ENERGY AT WHICH $F(E) = \frac{1}{2}$

F(E) = THE PROBABILITY THAT AN ENERGY STATE, E, IS OCCUPIED BY AN ELECTRON

K = THE BOLTZMANN CONSTANT

T = TEMPERATURE (^{O}K)

AS INDICATED IN FIGURE 3.1, IT IS NECESSARY TO GIVE THE ELECTRONS IN A METAL AN AMOUNT OF ENERGY EQUAL TO θ, THE WORK FUNCTION:

$$\theta \text{ (ELECTRON-VOLT)} = e \text{ (ELECTRON CHARGE)} \bullet V \text{ (VOLTS)} \quad \ldots\ldots\ldots \quad (16)$$

IN ORDER FOR THEM TO ESCAPE FROM THE METAL WITH NO KINETIC ENERGY. THIS CAN BE DONE BY HEATING THEM (THERMIONIC EMISSION), BY INTRODUCING A STRONG ELECTRIC FIELD (FIELD EMISSION), BY IMPACT WITH OTHER ELECTRONS (SECONDARY EMISSION), OR BY OTHER MEANS.

IF TWO DISSIMILAR METALS COME IN CONTACT THERE WILL BE A TRANSFER OF ELECTRONS FROM ONE MATERIAL TO THE OTHER UNTIL THE POTENTIALS OF THE MATERIALS ARE SUCH THAT THE FERMI LEVELS ARE ALIGNED AS INDICATED IN FIGURE 3.2. IN THIS CASE, ELECTRONS HAVE BEEN TRANSFERRED FROM MATERIAL A TO MATERIAL B TO ALIGN THE FERMI LEVELS. THE POTENTIAL DIFFERENCE (V_{A-B}) BETWEEN THE TWO MATERIALS FOR THE TRANSFERRED CHARGE IS EQUAL TO THE DIFFERENCE IN THE WORK FUNCTIONS ($\theta_A - \theta_B = e \bullet V_{A-B}$). THUS, MATERIAL B HAS BECOME NEGATIVELY CHARGED AND THE MATERIAL A HAS BECOME POSITIVELY CHARGED.

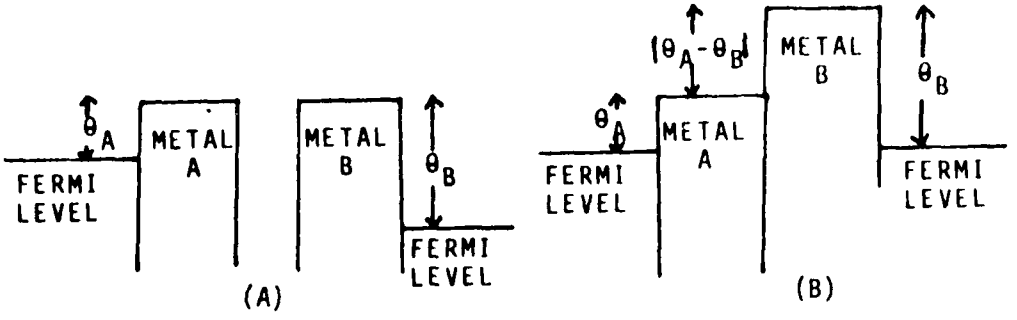


FIGURE 3.2: (A) METALS ARE SEPARATED; (B) METALS ARE IN CONTACT (REFERENCE 7)

THE SAME BASIC TYPE OF BEHAVIOR CAN BE POSTULATED FOR INSULATING SURFACES IN CONTACT, ALTHOUGH THE DETAILS ARE NOT GENERALLY UNDERSTOOD SINCE THE ENERGY LEVELS ARE NOT WELL DEFINED IN MANY INSULATING MATERIALS (PARTICULARLY THOSE WHICH ARE AMORPHOUS). IT IS VERY LIKELY THAT ONLY ELECTRONS VERY NEAR THE CONTACTING SURFACES TAKE PART IN THE CHARGING OF HIGHLY INSULATING MATERIALS. IF ANY TWO MATERIALS (A AND B) WHICH HAVE CONDUCTIVITIES AND PERMITIVITIES σ_A, σ_B, ε_A, AND ε_B, RESPECTIVELY, ARE BROUGHT INTO CONTACT, WE WOULD EXPECT THE CHARGING OF THOSE SURFACES AWAY FROM THE CONTACT AREA TO DEPEND ON THE RELAXATION TIME CONSTANTS $\tau_A = \varepsilon_A/\sigma_A$ AND $\tau_B = \varepsilon_B/\sigma_B$. THESE ARE THE TIME CONSTANTS FOR CHARGE TRANSFER IN THE MATERIALS, AND THEY GIVE A REASONABLE ESTIMATE OF THE TIME NECESSARY FOR REMOTE PORTIONS OF THE CONTACTING BODIES TO REACT ELECTRICALLY IN TERMS OF CHARGE DENSITY AFTER CONTACT WITH A CHARGED OBJECT HAS BEEN MADE. THE NET CHARGE SEPARATION OF THESE CONTACTS WILL DEPEND ON THE ELECTRONIC BULK AND SURFACE PROPERTIES OF THE MATERIALS IN CONTACT.

(2) TRIBOELECTRIC CHARGING

ANOTHER TYPE OF CHARGING, PERHAPS THE MOST COMMON METHOD OF CHARGING AS PREVIOUSLY DISCUSSED, IS TRIBOELECTRIC CHARGING, CAUSED BY RUBBING BETWEEN TWO SURFACES. HOWEVER, IT IS VERY DIFFICULT TO SEPARATE THE PHENOMENA OF CONTACT CHARGING FROM TRIBOELECTRIC (OR CHARGING BY RUBBING).

ALTHOUGH IDEALLY, TRIBOELECTRIC CHARGING REFERS TO CHARGE TRANSFER BY RUBBING (FRICTION) EFFECTS ONLY, COMMON USAGE OF THE TERM TRIBOELECTRIC CHARGING LUMPS CONTACT CHARGING AND FRICTIONAL CHARGING OF TWO MATERIALS TOGETHER. TRIBOELECTRIFICATION IS THE RESULT OF MECHANICAL EXPOSURE OF SURFACES THAT ARE MOVING RELATIVE TO ONE ANOTHER CHARGED BY COMING INTO CONTACT. IT IS BELIEVED THIS IS A COMBINATION OF CONTACT CHARGING AIDED BY THE THERMIONIC EMISSION CAUSED BY THE HEAT DUE TO FRICTION.

(3) INDUCTION CHARGING

ELECTROSTATIC CHARGES CAN BE INDUCED DUE TO THE PROXIMITY OF A CHARGED OBJECT. THE BASIC DIFFERENCE BETWEEN CONTACT AND INDUCTION CHARGING IS THAT THE CONTACT METHOD REQUIRES ACTUAL PHYSICAL CONTACT BETWEEN TWO OBJECTS WHILE THE INDUCTION METHOD DOES NOT. A BETTER UNDERSTANDING OF THE INDUCTION METHOD IS PROVIDED BY RECOGNIZING THE EXISTENCE OF A STATIC ELECTRIC FORCE FIELD EMINATING FROM A CHARGED BODY. THIS FIELD IS COMPRISED OF LINES OF FORCE WHEREIN OBJECTS OF SIMILAR CHARGE POLARITY REPEL EACH OTHER AND OBJECTS OF UNLIKE CHARGE POLARITY ARE ATTRACTED TO EACH OTHER.

WHEN A CHARGED BODY (X) IS BROUGHT CLOSE TO A NEUTRAL BODY (Y), THE NEUTRAL BODY (Y) IS SUBJECTED TO THE ELECTRIC FIELD OF THE CHARGED BODY (X). IF THE BODY (X) CARRIES A NEGATIVE CHARGE (I.E., CONTAINS AN EXCESS OF FREE ELECTRONS), THE FORCE FIELD OF THAT CHARGE WILL REPEL THE FREE ELECTRONS IN BODY (Y) FORCING THEM AWAY FROM THE CHARGE. BODY (Y) IS NOW POLARIZED WITH THE POSITIVELY CHARGED SURFACE LOCATED NEAREST (X), THE "CHARGING" BODY, AND THE NEGATIVELY CHARGED SURFACE LOCATED FARTHEST FROM BODY (X), THE NET CHARGE ON BODY (Y), EVEN THOUGH POLARIZED, IS STILL ZERO. IF BODY (Y) IS REMOVED FROM THE INFLUENCE OF THE STATIC FIELD CAUSED BY BODY (X) THE CHARGE ON BODY (Y) WILL REDISTRIBUTE ITSELF AND BODY (Y) WILL RETURN TO A STATE OF UNPOLARIZED NEUTRAL (ZERO) CHARGE. INSTEAD OF REMOVING BODY (Y) FROM THE INFLUENCE OF BODY (X)'S STATIC FIELD, IF THE SURFACE OF BODY (Y) (POLARIZED NEGATIVELY) IS TOUCHED TO GROUND, ELECTRONS WILL FLOW TO GROUND AND BODY (Y) WILL HAVE A NET POSITIVE CHARGE. AFTER REMOVING BODY (Y) FROM THE FIELD OF BODY (X), THIS POSITIVE CHARGE WILL BE DISTRIBUTED OVER BODY (Y). BODY (Y) WILL THEN HAVE BEEN CHARGED POSITIVELY BY INDUCTION. THIS PRINCIPLE IS ILLUSTRATED IN THE FOLLOWING DIAGRAM (FIGURE 3.3).

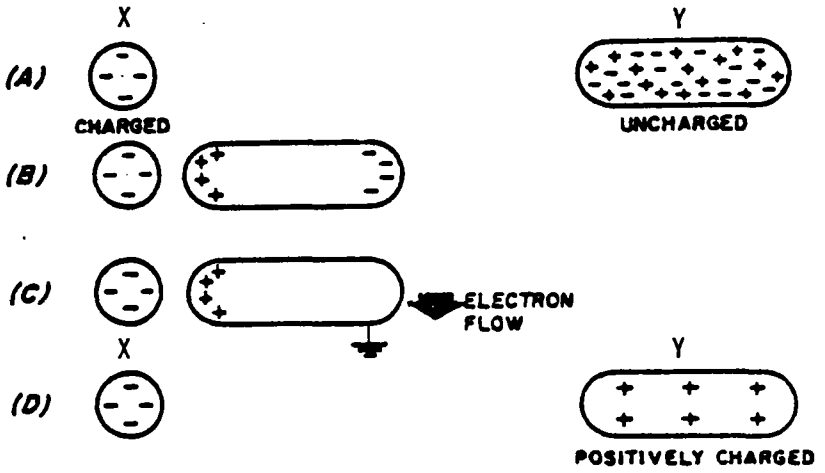


FIGURE 3.3: INDUCTION CHARGING

THE ELECTROSTATIC INDUCTION PHENOMENA CAN BE RESPONSIBLE FOR POLARIZING AN UNGROUNDED OBJECT OR CHARGING A GROUNDED OBJECT AS IS FREQUENTLY EXPERIENCED DURING THE PASSAGE OF A CHARGED CLOUD OVER AN OBJECT. PERSONNEL CAN ALSO INDUCE CHARGES ON NEARBY OBJECTS IN PROPORTION TO THE CHARGES THAT HAVE ACCUMULATED ON THEIR BODIES.

(4) CHARGING BY FREEZING

A NUMBER OF OBSERVERS HAVE FOUND LARGE POTENTIAL DIFFERENCES BETWEEN ICE AND WATER PHASES EXIST DURING THE FREEZING OF WATER. IT IS POSTULATED THAT AS A WATER DROP FREEZES, SMALL "SPLINTERS" ARE EJECTED FROM THE FREEZING DROP AND THE SPLINTERS ARE CHARGED OPPOSITELY TO THE REMAINING SOLID ICE PARTICLES. THIS MECHANISM CAUSES CLOUD ELECTRIFICATION DURING THUNDERSTORMS.

(5) ION AND ELECTRON BEAM CHARGING

IN A NUMBER OF INSTANCES IT HAS BEEN CONVENIENT TO CHARGE PARTICLES BY BOMBARDING THEM WITH IONS, ELECTRONS, OTHER ATOMIC PARTICLES

(E.G., ALPHA PARTICLES), OR X-RAYS. LET US ASSUME THAT THE PARTICLE IS CHARGED BY THE COLLECTION OF IONS OR ELECTRONS. CONSIDER A CHARGE PARTICLE BEAM IN WHICH THE PARTICLES CARRY A CHARGE "Q" AND HAVE A MASS "M" (FIGURE 3.4). LET THE BEAM CURRENT DENSITY BE J (AMPS/M^2); THE PARTICLE RADIUS BE "r"; AND THE BEAM RADIUS BE "R". IF THE PARTICLE FALLS THROUGH THE DIAMETER OF THE BEAM WITH A VELOCITY V (M/SEC), IT WILL BE IN THE BEAM A TIME:

$$t = \frac{2R}{V} \text{ (SEC)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (17)$$

DURING THAT TIME THERE WILL BE A CURRENT OF:

$$I = \pi r^2 J \text{ AMPERE} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (18)$$

IMPINGING ON THE PARTICLE. THE TOTAL CHARGE TRANSFERRED TO THE PARTICLE SURFACE WILL BE EQUAL TO tI OR:

$$Q = \frac{2\pi r^2 JR}{V} \text{ (COULOMB)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (19)$$

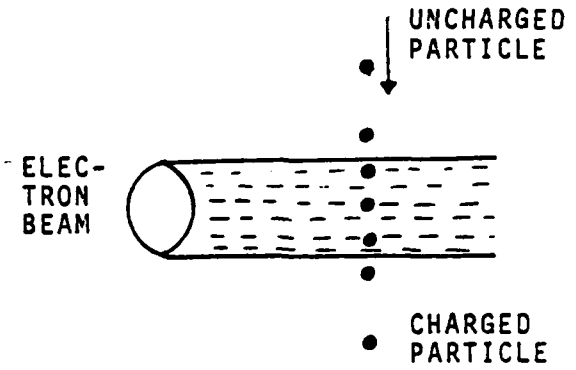


FIGURE 3.4: THE BEAM METHOD OF CHARGING PARTICLES

EXAMPLE (G): LET US USE SOME TYPICAL NUMBERS FOR THE VARIOUS PARAMETERS AND CALCULATE THE MAXIMUM CHARGE ON THE FALLING PARTICLE:

$r = 10^{-5}$ METER, $R = 10^{-3}$ METER, J = 0.1 AMPERE/$METER^2$

AND V = 1.0 METER/SEC

THE CHARGE Q FOR THE PARTICLE AFTER IT TRAVERSES THE ION BEAM IS CALCULATED AS FOLLOWS:

$$Q = \frac{2\pi r^2 JR}{V} \text{ (COULOMB) (EQUATION 19)}$$

$$= \frac{2\pi (10^{-5})^2 (1.1)(10^{-3})}{(1.0)} \text{ (COULOMB)}$$

$$= 1.97 \times 10^{-13} \text{ (COULOMB)}$$

THE AMOUNT OF CHARGING OF THE PARTICLE FALLING THROUGH THE BEAM ALSO DEPENDS ON THE ENERGY OF THE ELECTRONS OR IONS. INITIALLY THE PARTICLE HAS NO CHARGE ON ITS SURFACE; HENCE THE INCOMING IONS (ELECTRONS) FIND NO RETARDING FIELDS TO KEEP THEM FROM THE SURFACE. AS THE PARTICLE BECOMES MORE HIGHLY CHARGED WITH ELECTRONS, THE ELECTRONS AND IONS IN THE BEAM ARE ACTED ON BY THE FIELD PRODUCED BY THE CHARGED PARTICLE. IF THE BEAM ELECTRONS OR IONS HAVE AN ENERGY LEVEL THAT IS HIGH COMPARED WITH THAT OF THE FALLING PARTICLE, THEY WILL REACH THE SURFACE OF THE FALLING PARTICLE DURING THE ENTIRE TIME PERIOD THAT THE PARTICLE IS IN THE BEAM. ON THE OTHER HAND, IF THE POTENTIAL OF THE FALLING PARTICLE BECOMES COMPARABLE TO THE BEAM ENERGY WHILE IT IS STILL IN THE BEAM, THE IONS (ELECTRONS) IN THE BEAM WILL BE REPELLED AND CHARGING WILL CEASE OR THE RATE OF CHARGE WILL BE MARKEDLY REDUCED.

MANY AIR IONIZERS USE ALPHA PARTICLE EMISSION FOR CHARGING PARTICLES IN THE AIR. THE ALPHA PARTICLES COLLIDING WITH ATOMS IN THE AIR CREATE POSITIVELY CHARGED AIR MOLECULES AND FREE ELECTRONS WHICH ALSO COMBINE WITH AIR MOLECULES FORMING BOTH POSITIVELY CHARGED AND NEGATIVELY CHARGED IONS.

(6) SPRAY CHARGING

THE PHENOMENON OF THE FORMATION OF CHARGED DROPS IN A CLOUD OR FOG PRODUCED BY AN ATOMIZED SPRAY OF A LIQUID IS COMMONLY DESCRIBED AS THE BALLOELECTRIC EFFECT. THIS EFFECT IS EXPLAINED AS THE ELECTRIFICATION OF DROPS DURING MECHANICAL ATOMIZATION OF THE LIQUID OCCURS BECAUSE THE DROPS CARRY EXCESS CHARGE OF ONE OR THE OTHER POLAIRY AND THAT THESE CHARGES FORM IN THE VOLUME OF THE DROP AS A RESULT OF FLUCTUATIONS IN THE ION DISTRIBUTION IN THE LIQUID. SOME OTHER RESEARCH WORKERS EXPLAIN THE PHENOMENA ON THE BASIS OF A DOUBLE LAYER OF CHARGE AT THE SURFACE OF THE LIQUID.

IN THE DOUBLE LAYER THEORY, A LAYER OF ORIENTED DIPOLES IS FOUND AT THE LIQUID-GAS INTERFACE. DEPENDING ON THE LIQUID, THE DIPOLES MAY BE ORIENTED WITH NEGATIVE POLES OUTWARD AND POSITIVE POLES INWARD. IN THIS CASE, THE INWARD ENDS OF THE DIPOLES ATTRACT AND IN SOME CASES BIND VERY TIGHTLY SOME OF THE NEGATIVE IONS PRESENT IN THE LIQUID. THE IONS OF POSITIVE SIGN IN THE LIQUID ARE LESS STRONGLY HELD TO THEIR POSITIVE COUNTERPARTS, AND THEY THEREFORE MOVE RANDOMLY IN THE LIQUID WITH MORE EASE.

THUS, THE DOUBLE LAYER AND ITS ATTACHED NEGATIVE IONS CONSTITUTE A CHARGED LAYER WHICH, WHEN SPRAYED OR OTHERWISE DISRUPTED TO FORM SMALLER DROPLETS, WILL LEAD TO NET NEGATIVE CHARGES ON THE DROPLETS. THE POSITIVE CHARGES TEND TO REMAIN ON THE SPRAY CONTAINER. THE PRESENCE OR ADDITION OF IMPURITIES OR SALTS OF VARIOUS KINDS AND IN VARIOUS AMOUNTS CAN ALTER QUITE DRASTICALLY THE SPRAY CHARGING PROCESS.

IT IS TO BE NOTED THAT THE TIME CONSTANTS FOR CHARGE AND MASS TRANSFER OF VARIOUS LIQUIDS PLAY A VERY IMPORTANT ROLE IN ANY OF THESE PHENOMENA. THESE TIME CONSTANTS ARE DEPENDENT UPON THE CONDUCTIVITY OF THE LIQUID AND THE MASS TRANSFER OF THE DROPLETS. IF THE NEGATIVE CHARGES

ARE MECHANICALLY REMOVED FASTER THAN THE NEGATIVE CHARGES CAN BE TRANSFERRED BACK THROUGH THE LIQUID, THE CHARGE PER UNIT MASS OF THE DROPLET WILL BEGIN TO FALL. A HIGHLY INSULATING LIQUID MAY REACH THE POINT WHERE A NET CHARGE IS NOT POSSIBLE, AND CAN GO FROM AN ASYMMETRICAL CHARGING SITUATION TO A SYMMETRICAL SITUATION WHERE EACH DROPLET MAY BE SLIGHTLY CHARGED, ALTHOUGH THE NET CHARGE (AVERAGED OVER ALL DROPLETS SPRAYED) WILL BE ZERO. IT SHOULD BE POINTED OUT THAT ANY LOCAL FIELDS AT THE LIQUID SURFACE WILL AFFECT THE RESULTS DRASTICALLY AND WILL LEAD TO INCORRECT INTERPRETATION OF ANY DATA OBTAINED UNLESS THEIR PRESENCE IS TAKEN INTO ACCOUNT.

(7) OTHER METHODS OF CHARGING

OTHER LESS KNOWN METHODS OF ELECTROSTATIC CHARGING ALSO PERTINENT TO ESD AND ESD CONTROL ARE AS FOLLOWS:

(a) CHARGING BY THERMIONIC EMISSION

IN SOME INSTANCES, PARTICLES ARE RAISED TO TEMPERATURES HIGH ENOUGH TO PERMIT THERMIONIC EMISSION OF ELECTRONS TO TAKE PLACE AS OCCURS IN THE FILAMENT OF AN ELECTRON TUBE. IF SOME OF THESE ELECTRONS ARE REMOVED BY AN EXTERNAL FIELD OR BY A NEAR ENCOUNTER WITH ANOTHER SURFACE, THE PARTICLE COULD END UP WITH A POSITIVE CHARGE.

(b) PHOTOELECTRIC CHARGING

IF LIGHT FALLS ON THE SURFACE OF A PARTICLE, THE LIGHT QUANTA CAN IMPART SUFFICIENT ENERGY TO ELECTRONS ON THE SURFACE TO EJECT THEM FROM THE PARTICLE LEAVING THE PARTICLE POSITIVELY CHARGED. THIS PHENOMENA IS KNOWN AS PHOTOELECTRIC CHARGING.

(c) FIELD EMISSION CHARGING

IF AN UNCHARGED PARTICLE (LIQUID OR SOLID) ENTERS A REGION IN WHICH THERE IS AN ELECTRIC FIELD, THE PARTICLE WILL BE POLARIZED.

THAT IS, THERE WILL BE A TRANSFER OF CHARGE WITHIN THE PARTICLE SO THAT ONE END OF THE PARTICLE BECOMES NEGATIVELY AND THE OTHER END POSITIVELY CHARGED. IF THE FIELD INTENSITY, E, IS HIGH ENOUGH, ELECTRONS MAY BE EXTRACTED BY THE HIGH FIELD FROM THE NEGATIVE END (ELECTRON FIELD EMISSION) AND/OR POSITIVE IONS MAY BE EXTRACTED FROM THE POSITIVE END (POSITIVE ION) FIELD EMISSION. IF ELECTRONS LEAVE THE PARTICLE, THE PARTICLE BECOMES POSITIVELY CHARGED AND EXPERIENCES A FORCE IN THE DIRECTION OF THE ELECTRIC FIELD.

(d) CORONA CHARGING

IF A PARTICLE IS CAUSED TO TRAVEL THROUGH A REGION OF IONIZED GAS IN WHICH THE CHARGE IS PREDOMINANTLY OF ONE POLARITY OR THE OTHER, THE PARTICLE ACQUIRES A NET NON-ZERO CHARGE. IN REALITY, THE SITUATION IS MORE COMPLEX BECAUSE IN ANY IONIZED GAS THERE ARE IONS OF BOTH POLARITIES (OR POSITIVE IONS AND ELECTRONS OR NEGATIVE IONS) PRESENT, EVEN THOUGH IONS OF ONE POLARITY MAY PREDOMINATE. IN THE LATTER CASE, THE PARTICLE WILL CHARGE TO THE POLARITY OF THE MOST PREDOMINANT IONS. THE PARTICLE WILL BE CHARGED TO A VALUE DEPENDING ON THE TEMPERATURE OF THE IONS AND ELECTRONS IN THE GAS AND ON THEIR MASSES. THE IONIZED GAS COULD BE FORMED DUE TO CORONA DISCHARGE OF A SHARP POINTED OBJECT, CHARGED TO A HIGH VOLTAGE.

(e) SURFACE CHARGING BY DEFORMATION AND CLEAVAGE

DEFORMATION OF A SOLID BODY CAN GIVE RISE TO SURFACE CHARGES. THIS OCCURS BY THE REORIENTATION OF POLAR MOLECULES OR DISPLACEMENT OF IONS UNDER THE ACTION OF AN EXTERNAL PRESSURE, AND THE GENERATION AND MIGRATION OF DISLOCATIONS. THE FIRST MECHANISM REQUIRES A PARTICULAR CRYSTAL SYMMETRY.

B. PARAMETERS INFLUENCING THE MAGNITUDE OF STATIC CHARGE GENERATION

(1) CONDUCTIVITY

THE ABILITY OF A MATERIAL TO SURRENDER ITS ELECTRONS OR ABSORB EXCESS ELECTRONS IS A FUNCTION OF THE CONDUCITIVITY OF THE MATERIAL. FOR EXAMPLE, IN A GOOD CONDUCTOR, SUCH AS COPPER, ELECTRONS MOVE ABOUT FREELY, AND RAPIDLY. IF GROUNDED A CONDUCTIVE MATERIAL WOULD GIVE THE CHARGE UP TO GROUND AND BECOME NEUTRAL.

FOR HIGHLY NON-CONDUCTIVE (INSULATIVE) MATERIALS, SUCH AS PLASTICS, IT IS EXTREMELY EASY TO DISRUPT THE MOLECULAR STRUCTURE AND CAUSE THE MATERIAL TO CHARGE WITH THE SLIGHTEST FRICTION, HEAT OR PRESSURE. HOWEVER, IF THE CONDUCTIVITY OF THE INSULATIVE MATERIAL CAN BE INCREASED, THEN, PREVENTING STATIC ELECTRICITY BECOMES RELATIVELY EASY SINCE THE CHARGE WILL BE DISPERSED OVER THE SURFACE OF THE MATERIAL, AND IF GROUNDED WILL FLOW TO GROUND.

FOR EXAMPLE, ADDING CONDUCTIVITY TO PLASTICS (E.G., ANTISTATS WHICH CREATE A CONDUCTIVE LAYER, OR IMPREGNATING THE PLASTIC WITH A CONDUCTIVE SUBSTANCE) WILL MOVE THESE MATERIALS HIGHER INTO THE CONDUCTIVITY RANGE AND REDUCE THE BUILDUP OF STATIC ELECTRICITY DUE TO ANY CHARGING MECHANISM. SOME ANTISTATS, IMPREGNATED WITHIN THE PLASTICS, BLEED TO THE SURFACE AND REACT WITH THE HUMIDITY IN THE AIR TO FORM A CONDUCTIVE SWEAT LAYER. TOPICAL ANTISTATIC SPRAYS USED TO PROVIDE A SLIGHTLY CONDUCTIVE COATING ARE TYPICALLY MADE UP FROM A DETERGENT BASED MATERIAL THAT HAS BEEN DILUTED IN A SOLVENT, SUCH AS A MILD ALCOHOL. A FIRE RETARDANT IS ADDED TO COMBAT THE FLAMMABILITY OF THE SOLVENT, FREONS ARE ADDED TO PROVIDE SPRAY PRESSURE, ENDING UP WITH THE FINAL PRODUCT COMMONLY KNOWN AS AN AEROSOL ANTI-STATIC SPRAY. AS THIS SPRAY LEAVES THE NOZZLE OF THE AEROSOL CAN, THE FREONS

NORMALLY EVAPORATE IMMEDIATELY. A SHORT TIME AFTER CONTACT WITH THE MATERIAL TO BE COATED, THE FIRE RETARDANT AND SOLVENTS EVAPORATE, LEAVING A DETERGENT OR SLIGHTLY CONDUCTIVE COATING ON THE SURFACE OF THE MATERIAL. THE PLASTIC HAS NOW BECOME MORE CONDUCTIVE AND AS LONG AS THIS COATING IS NOT DISTURBED, IT WILL HELP RETARD THE GENERATION OF STATIC ELECTRICITY ON THIS MATERIAL.

(2) HUMIDITY

HUMID AIR HELPS TO DISSIPATE GENERATED ELECTROSTATIC CHARGES BY KEEPING SURFACES MOIST WITH A CONDUCTIVE SWEAT LAYER OF WATER AND DUST PARTICLES. ELECTROSTATIC VOLTAGE LEVELS GENERATED CAN INCREASE SUBSTANTIALLY WITH A DECREASE IN RELATIVE HUMIDITY WHERE THE SWEAT LAYER IS DEPLETED AS SHOWN IN TABLE III-A. HOWEVER, IT IS ALSO EVIDENT FROM TABLE III-A THAT RELATIVELY HIGH ELECTROSTATIC VOLTAGES CAN STILL BE GENERATED WITH RELATIVE HUMIDITY AS HIGH AS 90%. RELATIVE HUMIDITY LEVELS IN ESD PROTECTIVE AREAS SHOULD BE MAINTAINED IN THE RANGE OF 40 TO 60% OR HIGHER AS LONG AS IT DOES NOT RESULT IN ACCELERATING RUST FORMATION OR RESULT IN OTHER DETRIMENTAL EFFECTS. WHERE HIGH RELATIVE HUMIDITY LEVELS CANNOT BE MAINTAINED THE USE OF IONIZED AIR CAN BE USED TO AID IN DISSIPATING ELECTROSTATIC CHARGES ON INSULATORS.

C. MATHEMATICAL EXPRESSIONS FOR ELECTROSTATIC DISCHARGE (ESD)

WHAT TYPICALLY HAPPENS DURING AN ELECTROSTATIC DISCHARGE CAN BE SIMULATED BY A CAPACITOR CHARGED TO SOME POTENTIAL AND THEN DISCHARGED THROUGH A RESISTOR. CONSIDER THE CIRCUIT IN FIGURE 3.5. IT IS ASSUMED THAT CAPACITOR C HAS BEEN CHARGED TO A VOLTAGE $V = Q_o/C$ PRIOR TO $t = o$. THE CHARGE Q_o MIGHT HAVE BEEN PRESENT AT THE PLATES OF THE CAPACITOR FOR SOME PERIOD OF TIME PRIOR TO THE CLOSING OF SWITCH(S) SINCE A PERFECT DIELECTRIC

TABLE III-A

TYPICAL MEASURED ELECTROSTATIC VOLTAGES (REFERENCE 8)

MEANS OF STATIC GENERATION	RELATIVE HUMIDITY	
	LOW - 10-20%	HIGH - 65-90%
WALKING ACROSS CARPET	35,000	1,500
WALKING OVER VINYL FLOOR	12,000	250
WORKER AT BENCH	6,000	100
VINYL ENVELOPES FOR WORK INSTRUCTIONS	7,000	600
COMMON POLY BAG PICKED UP FROM BENCH	20,000	1,200
WORK CHAIR PADDED WITH URETHANE FOAM	18,000	1,500

MATERIAL IS ASSUMED. ACTUALLY THE DIELECTRIC LEAKAGE, Rg AND THE CHARGE BLEEDING OFF INTO THE AIR, Ra (FIGURE 3.6) WILL CAUSE THE CHARGE TO GRADUALLY DIMINISH TO ZERO. WITH VALUES OF Ra/Rg ON THE ORDER OF 10^{13} OHMS, THE TIME CONSTANT WOULD BE RC = $10^{13} \times 10^{-10} = 10^{3}$ SECONDS OR 17 MINUTES WITH THE DISCHARGE CURRENT BEING QUITE LOW. THIS TIME IS REFERRED TO AS RELAXATION TIME IN ELECTROSTATICS. THIS IS A PARAMETER OF PRIME IMPORTANCE WHEN CONSIDERING THE ESD HAZARD TO SEMICONDUCTORS. RELAXATION TIME IS A MEASURE OF THE TIME REQUIRED FOR A CHARGE TO DISSIPATE BY LEAKAGE. IT IS EQUAL TO:

$$\tau = \varepsilon_r \varepsilon_o / \gamma \quad \text{......} \quad (20)$$

$$\tau = RC \quad \text{......} \quad (21)$$

WHERE:

ε_o IS THE ABSOLUTE DIELECTRIC CONSTANT FOR FREE SPACE (8.85×10^{-14} SEC/OHM CM).

ε_r = RELATIVE DIELECTRIC CONSTANT, DIMENSIONLESS

γ = SPECIFIC CONDUCTIVITY (OHM - CM)$^{-1}$

R = EFFECTIVE RESISTANCE TO GROUND CONSIDERING ALL PARALLEL PATHS (OHMS)

C = CAPACITANCE OF THE CHARGED OBJECT (FARADS)

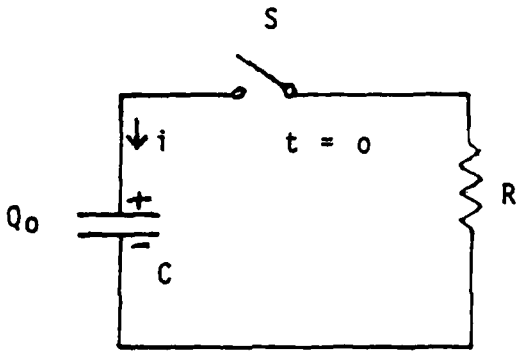


FIGURE 3.5: CAPACITOR DISCHARGING THROUGH A RESISTANCE

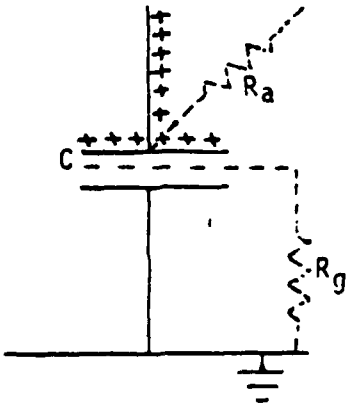


FIGURE 3.6: CHARGE STORED AND LEAKAGE PATHS

THE CAPACITOR DISCHARGE PHENOMENA (FIGURE 3.5), AT AND AFTER t = o IS DESCRIBED BY THE FOLLOWING DIFFERENTIAL EQUATION:

$$Ri + \frac{q}{C} = o \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (22)$$

SUBJECT TO THE CONDITION THAT $q = Q_o$ AT $t = o$, THE CHARGE, q, IN EQUATION (22), IS:

$$q = Q_o \pm \int_o^t di\, dt \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (23)$$

WHERE:

$\pm \int_o^t i\, dt$ IS THE CHARGE TRANSFERRED TO (CHARGING) OR FROM (DISCHARGING) THE CAPACITOR PLATES AS A RESULT OF CURRENT FLOW. EQUATION (22) CAN BE WRITTEN IN TERMS OF q AS:

$$R \frac{dq}{dt} + \frac{q}{C} = o \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (24)$$

A SOLUTION OF THE ABOVE EQUATION FOR q AS A FUNCTION OF TIME IS:

$$q = A\, e^{\alpha t} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (25)$$

SINCE:

$$R\ (A\alpha e^{\alpha t}) + \frac{A}{C} \alpha t = Ae^{\alpha t} (R\alpha + \frac{1}{C}) = 0$$

PROVIDED THAT:

$$(R\alpha + \frac{1}{C}) = o \qquad \text{or} \qquad \alpha = -\frac{1}{RC}$$

USING INITIAL CONDITION ($q = Q_o$ AT $t = o$) ON EQUATION (25):

$A = Q_o$, THEREFORE:

$$q = Q_o\, e^{-t/RC} \quad \text{..... (26)}$$

$$= VC\, e^{-t/RC}$$

AND THE CIRCUIT CURRENT:

$$i = \frac{dq}{dt} = -\frac{Q_o}{RC}\, e^{-t/RC} \quad \text{..... (27)}$$

EQUATION (26) SHOWS THAT THE CHARGE AT THE PLATES OF THE CAPACITOR SUBSIDES FROM ITS INITIAL VALUE OF Q_o AT A TIME RATE WHICH IS GOVERNED BY THE RC PRODUCT. EQUATION (27) SHOWS THAT THE CURRENT AT $t = o$, IS:

$$I_o = -\frac{Q_o}{RC} = -\frac{V}{R} \quad \text{..... (28)}$$

$$i(t) = I_o\, e^{-t/RC}$$

$$= I_o\, e^{-t/\tau}$$

THE LENGTH OF TIME REQUIRED FOR q (OR i) TO LOSE 63.2% OF ITS TOTAL CHARGE IS $\tau = RC$, SINCE IT IS THIS VALUE OF TIME WHICH, WHEN ENTERED INTO EQUATION (27), REDUCES THE CHARGE q TO .368 Q_o. IN 5τ THE CHARGE WILL BE REDUCED TO APPROXIMATELY 99% OF Q_o. THE CHARGE q CHANGES FROM Q_o, AT $t = o$, TO ZERO VALUE ONLY AT $t = \infty$. THE PRODUCT $RC = \tau$ IS CALLED THE TIME CONSTANT OF THE CIRCUIT.

EXAMPLE (H): CONSIDER A CHARGED HUMAN WITH THE FOLLOWING VALUES FOR THE DISCHARGE PARAMETERS:

C = 100 PF, R = 1,500 OHM, AND V = 10,000 VOLTS

THE PEAK CURRENT $I_o = \frac{V_o}{R} = \frac{10,000}{1,500} = 6.66$ AMPERES

THE INSTANTANEOUS POWER DISSIPATED IN THE RESISTOR IS:

$$P_i = i_i^2 R = R I_o^2 e^{-2t/\tau}$$

WHERE:

$= RC = 150$ NSEC

THE AVERAGE POWER OVER FIVE TIME CONSTANTS IS:

$$P_{AV} = \frac{1}{5\tau} \int_0^{5\tau} R I_o^2 e^{-2t/\tau} dt$$

$$P_{AV} = \frac{R I_o^2}{10} (1 - e^{-10})$$

$$= \frac{R I_o^2}{10}$$

$= 6653$ WATTS

THE AVERAGE POWER DISSIPATED IN THE RESISTOR OVER 5 RC (=750 N SEC) TIME PERIOD IS THEN CALCULATED TO BE 6653 WATTS. THE ENERGY IS 6653 X 750 X 10^{-9} = 5 X 10^{-3} JOULES. IN THIS EXAMPLE MOST OF THE ENERGY IN THE CAPACITOR IS DISSIPATED IN THE RESISTOR IN A VERY SHORT PERIOD OF TIME (750 N SEC). CONSEQUENTLY, THE POWER IS QUITE HIGH. IN REALITY, PART RESISTANCE ADDS CONSIDERABLE RESISTANCE WHEN DISCHARGING THROUGH A PART WHICH REDUCES THE POWER LEVEL, LENGTHENS THE DISCHARGE PULSE AND RESULTS IN MOST OF THE STORED ENERGY BEING DISSIPATED IN THE PART ITSELF.

EXAMPLE (I): EXPERIENCE HAS SHOWN THAT PERSONNEL IN A MANUFACTURING ENVIRONMENT COMMONLY ATTAIN POTENTIALS OF 10,000 VOLTS OR MORE JUST WALKING ACROSS THE FLOOR, ESPECIALLY UNDER CONDITIONS OF LOW HUMIDITY. FOR AN ANTI-STATIC TABLE MAT, AN ANTI-STATIC FLOOR MAT OR A WRIST STRAP TO BE EFFECTIVE IT SHOULD HAVE A RESISTANCE TO GROUND TO ALLOW DISCHARGE FROM 10,000 VOLTS DOWN TO A SAFE LIMIT (FOR EXAMPLE 100 VOLT) IN APPROXIMATELY ONE MILLISECOND. THE MAXIMUM RESISTANCE TO GROUND FOR THE EFFECTIVE DISSIPATION OF SUCH POTENTIALS IS CALCULATED AS FOLLOWS:

$$V = V_o \, e^{-\frac{t}{RC}}$$

WHERE:

V = 100 VOLTS (ASSUMED SAFE LEVEL)

V_o = 10,000 VOLTS (INITIAL VOLTAGE OF OBJECT OR PERSON)

t = 1 MILLISECOND (ALLOWABLE TIME FOR DISCHARGE TO V)

C = 100 PF

R = MAXIMUM ALLOWABLE RESISTANCE TO GROUND IN OHMS

$$100 = 10{,}000 \; EXP \left(- \frac{10^{-3}}{100 \times 10^{-12} R}\right)$$

$$R = \frac{1}{\ell n \; 100 \times 10^{-7}}$$

$$= 2.17 \times 10^{6} = 2.17 \text{ MEGOHMS}$$

NOTE: THIS IS AN ILLUSTRATIVE MATHEMATICAL CALCULATION TO FIND THE MAXIMUM RESISTANCE TO GROUND FOR THE EFFECTIVE DISSIPATION OF STATIC VOLTAGE TO A SAFE LEVEL. THE SAFE LEVEL VOLTAGE AND THE TIME TO REACH THE VALUE SHOULD NOT BE CONSIDERED AS ACCEPTED VALUES.

EXAMPLE (I) (CONTINUED): THUS, A RESISTANCE OF 2×10^6 OHMS TO GROUND THROUGH EITHER A TABLE MAT OR FLOOR MAT OR WRIST STRAP OR ANY OF THE COMBINATIONS, ASSURES THAT DISCHARGE TO A SAFE LIMIT (100 VOLTS) WILL OCCUR WITHIN ONE MILLISECOND. THIS, FOR ALL PRACTICAL PURPOSES, MINIMIZES THE CHANCE THAT A STATIC SENSITIVE ELECTRONIC COMPONENT CAN BE EXPOSED TO A STATIC CAUSED ELECTRICAL OVERSTRESS.

IV. PRIME STATIC GENERATORS

A. TYPICAL CHARGE GENERATORS

TYPICAL PRIME CHARGE SOURCES COMMONLY ENCOUNTERED IN A MANUFACTURING FACILITY ARE SHOWN IN TABLE IV-A. THESE SOURCES INCLUDE THE WORLD AROUND US. THEY CONSIST OF OUR BUILDING FLOOR AND WALLS, CHAIRS, WORK SURFACES, CLOTHING, PACKAGING, TOOLS, TEST AND PROCESSING EQUIPMENT. THESE PRIME SOURCES ARE COMMONLY NON-CONDUCTORS AND TYPICALLY SYNTHETIC NON-CONDUCTIVE TYPE MATERIALS. ELECTROSTATIC VOLTAGE LEVELS GENERATED BY NON-CONDUCTORS CAN BE EXTREMELY HIGH AND ARE SUSTAINED FOR LONG PERIODS OF TIME SINCE CHARGES ARE IMMOBILE, ARE NOT DISSIPATED OVER THE SURFACE OF THE SUBSTANCE, OR READILY CONDUCTED TO ANOTHER CONTACTING SUBSTANCE. HOWEVER, IONS IN THE AIR AND LOW LEAKAGE CURRENT BASED UPON THE RESISTIVITY OF THE MATERIAL WILL SLOWLY DISSIPATE THE CHARGE TO A NEARBY MASS OR GROUND. THE MORE MOISTURE IN THE AIR THE FASTER A CHARGE WILL DISSIPATE. THIS IS DUE TO THE MOISTURIZING OF SURROUNDING MATERIALS WHICH USUALLY MAKES THEM MORE CONDUCTIVE (SEE SECTION III). THE GENERATION OF 15,000 VOLTS FROM PRIME SOURCES IN A TYPICAL MANUFACTURING FACILITY WITHOUT ESD PROTECTIVE CONTROLS IS NOT UNUSUAL.

B. MANUFACTURING PROCESSES GENERATING STATIC ELECTRICITY

MANY OF THE PROCESSES INVOLVED IN THE MANUFACTURE OF ELECTRONIC EQUIPMENT CAN GENERATE VARYING LEVELS OF STATIC VOLTAGES. SOME EXAMPLES OF THESE PROCESSES ARE AS FOLLOWS:

(1) CRYOGENIC COOLANTS

CRYOGENIC COOLANTS ARE COMMONLY USED FOR TROUBLE-SHOOTING AND ENVIRONMENTAL TESTING. FACTORY TEST TECHNICIANS, IN ORDER TO ISOLATE A

TABLE IV-A

TYPICAL PRIME CHARGE SOURCES

- WORK SURFACES
  - WAXED, PAINTED OR VARNISHED SURFACES
  - COMMON VINYL OR PLASTICS
- FLOORS
  - SEALED CONCRETE
  - WAXED, FINISHED WOOD
  - COMMON VINYL TILE OR SHEETING
- CLOTHES
  - COMMON CLEAN ROOM SMOCKS
  - COMMON SYNTHETIC PERSONNEL GARMENTS
  - NON-CONDUCTIVE SHOES
  - VIRGIN COTTON*
- CHAIRS
  - FINISHED WOOD
  - VINYL
  - FIBERGLASS
- PACKAGING AND HANDLING
  - COMMON PLASTIC - BAGS, WRAPS, ENVELOPES
  - COMMON BUBBLE PACK, FOAM
  - COMMON PLASTIC TRAYS, PLASTIC TOTE BOXES, VIALS, PARTS BINS
- ASSEMBLY, CLEANING, TEST AND REPAIR AREAS
  - SPRAY CLEANERS
  - COMMON PLASTIC SOLDER SUCKERS
  - SOLDER IRONS WITH UNGROUNDED TIPS
  - SOLVENT BRUSHES (SYNTHETIC BRISTLES)
  - CLEANING OR DRYING BY FLUID OR EVAPORATION
  - TEMPERATURE CHAMBERS
  - CRYOGENIC SPRAYS
  - HEAT GUNS AND BLOWERS
  - SAND BLASTING
  - ELECTROSTATIC COPIERS

*VIRGIN COTTON CAN BE A STATIC SOURCE AT LOW RELATIVE HUMIDITIES SUCH AS BELOW 30%.

DEFECTIVE INTEGRATED CIRCUIT, OFTEN USE A CANNED CRYOGENIC SUCH AS KOOL-ZIT,® QUICK FREEZE,® OR OTHER BRAND NAMES TO COOL A SMALL ZONE ON AN ASSEMBLY BOARD. LIQUID NITROGEN (LN_2) IS ALSO USED FOR THIS PURPOSE. STATIC CHARGE GENERATION IS USUALLY DEVELOPED DURING THIS PROCESS BY THE FOLLOWING METHODS:

(a) GAS EXPANSION INTO THE ATMOSPHERE OF DIFFERENT GASSES PRODUCES FRICTION BETWEEN THE MOLECULES OF THE GASSES. THIS PHENOMENON OCCURS AT THE EXPANSION POINT OF AN AEROSOL SPRAY CAN NOZZLE.

(b) AS THE CRYOGENIC LIQUID CONTACTS THE SURFACE OF THE ASSEMBLY BOARD, THE LOWERED TEMPERATURE CAUSES THE HUMIDITY (WATER) IN THE AIR TO CONDENSATE ON THE SURFACE. AT THE INTERFACE BETWEEN THE ASSEMBLY'S SURFACE AND THE WATER CONDENSATE A STATIC POTENTIAL DIFFERENCE IS PRODUCED.

(2) ULTRA-VIOLET (UV) LIGHT

ULTRA-VIOLET LIGHT OFTEN USED FOR VISUAL INSPECTION CAUSES NEGATIVELY CHARGED MATERIALS TO LOSE THEIR CHARGE. ALSO, IF THE MATERIAL IS UNCHARGED, THAT MATERIAL WILL ACQUIRE A POSITIVE CHARGE AS A RESULT OF THE ILLUMINATION.

THE CHARGE GENERATION REQUIRES APPROXIMATELY THIRTY MINUTES TO AN HOUR TO DEVELOP A CHARGE HIGH ENOUGH TO CAUSE A PROBLEM, DEPENDENT UPON THE TYPE OF MATERIAL THAT IS BEING ILLUMINATED. NORMAL UV LIGHT INSPECTION TIME SHOULD NOT CAUSE ANY PROBLEM. PROLONGED EXPOSURE COULD RESULT IN VOLTAGE LEVELS THAT COULD DAMAGE PARTS HIGHLY SENSITIVE TO ESD. THEREFORE, ASSEMBLIES WITH ESDS PARTS SHOULD NOT BE PLACED NEAR A UV LIGHT SOURCE FOR LONG PERIODS OF TIME.

(3) FLUID FLOW

MACHINES INCORPORATING FLUID FLOW OR EVAPORATION SUCH AS FLOW SOLDER MACHINES AND VAPOR DE-GREASERS ARE SOURCES OF STATIC CHARGE. THE

VAPOR DE-GREASING PROCESS REQUIRES THAT THE ASSEMBLIES OR PARTS BE CLEANED IN A LIQUID REGION AND THEN BE HELD IN THE VAPOR REGION FOR A PERIOD OF TIME.

THE LIQUID PORTION OF THE FREON (TF, TE, ETC.) IS CONDUCTIVE AND WILL NOT GENERATE A CHARGE. HOWEVER, THE VAPOR REGION IS NON-CONDUCTIVE. AS THE VAPOR CONDENSES ON THE SURFACE OF THE ASSEMBLY OR COMPONENTS, A CHARGE OF UP TO 400 VOLTS CAN BE GENERATED. AS THE CONDENSATE FALLS FROM THE ASSEMBLY, THE CHARGE IS CARRIED AWAY AND NO RESIDUAL CHARGE REMAINS. HOWEVER, BY THIS TIME THE STATIC CHARGE COULD HAVE CAUSED A FAILURE OF A SENSITIVE PART ON THAT ASSEMBLY.

(4) CONFORMAL COATING

CONFORMAL COATING OF PRINTED WIRING BOARD ASSEMBLIES INVOLVES VARIOUS FORMS OF THE FOLLOWING STEPS:

- TAPING
- SPRAY OR DIP COATING OF POLYURETHANE OR OTHER COATING MATERIAL
- CURING IN AMBIENT ROOM TEMPERATURE
- CURING IN LAMINAR AIR FLOW OVENS WHILE MOUNTED IN METAL FRAME CARD-EDGE HOLDERS OR ON POLYPROPYLENE HOLDING TRAYS

(a) THE AMOUNT OF STATIC CHARGE GENERATED BY REMOVING INSULATING TAPE SUCH AS CELLOPHANE, PLASTIC, KAPTON, OR TEFLON COULD BE AS HIGH AS 8 KV. THIS CHARGE CAN BE GENERATED WHILE THE TAPE IS BEING PULLED FROM EITHER THE TAPE ROLL OR FROM THE ASSEMBLY. MOREOVER, SINCE THESE TAPES ARE NORMALLY INSULATIVE, CHARGES WILL NOT BLEED OFF BY CONTACT WITH A GROUNDED PERSON TOUCHING THE TAPE. TO PROTECT ELECTROSENSITIVE ASSEMBLIES (PRIOR TO CONFORMAL COATING) FROM THE CHARGE GENERATED BY THE TAPES, AN IONIZING BLOWER

CAN BE USED. AN IONIZER WILL NEUTRALIZE THE CHARGE BY BLOWING IONIZED AIR ACROSS THE WORK SURFACE AREA WHILE THE TAPES ARE APPLIED AND REMOVED. ALSO, THE TAPE SHOULD BE REMOVED SLOWLY.

(b) SPRAYING OF CONFORMAL COATING CAN CREATE SUBSTANTIAL STATIC CHARGES DUE TO THE "SPRAY CHARGING" PROCESS.

(c) NON-OVEN DRYING OF ASSEMBLIES CAN DEVELOP A STATIC CHARGE ON THE SURFACE OF THE ASSEMBLIES AS THEY SIT IN THE AMBIENT ROOM ENVIRONMENTS. THIS CHARGE IS GENERATED BY THE CONDENSATION OF WATER AND THE FORMATION OF A WATER-SOLID INTERFACE AT THE SURFACE OF THE ASSEMBLY. THE CONDENSATION OF WATER OCCURS DUE TO THE EVAPORATION OF SOLVENTS FROM THE POLYURETHENE COATED SURFACE, PRODUCING A LOW TEMPERATURE AT THE SURFACE OF THE ASSEMBLY.

(d) OVEN DRYING OF ASSEMBLIES USING METAL FRAME CARD-EDGE HOLDERS DOESN'T PRESENT CHARGE ACCUMULATION BECAUSE THE CHARGE WILL BLEED OFF TO THE CARD HOLDER AND IF THE OVEN SURFACES ARE CONDUCTIVE, TO THE OVEN GROUND. WHEN THE ASSEMBLIES ARE PLACED IN THE OVEN ON A POLYPROPYLENE TRAY, HOWEVER, CHARGES CAN ACCUMULATE ON BOTH THE TRAY AND ASSEMBLY AS A RESULT OF THE FLOW OF HOT AIR ACROSS THEIR SURFACES. THIS CHARGING WILL BE IN ADDITION TO THE CHARGES ALREADY PRESENT ON THE ASSEMBLY AND THE TRAY DUE TO NORMAL HANDLING OPERATIONS SUCH AS TOUCHING, SLIDING, OR LIFTING THE TRAY PRIOR TO PLACING IT IN THE OVEN.

(5) REMOVAL OF CONFORMAL COATING

GIDEP ALERT REPORT NUMBER R4-F-78-01 (REFERENCE NO. 9) REPORTED THE FOLLOWING FAILURE EXPERIENCE DUE TO ELECTROSTATIC DISCHARGE: ATTEMPTS TO REMOVE CONFORMAL COATINGS, PARTICULARLY VAPOR-DEPOSITED PARYLENE

FROM ELECTRONIC ASSEMBLIES DAMAGED STATIC-SENSITIVE ELECTRONIC PARTS. REPLACEMENT OF A FAILED PART ON A CONFORMALLY COATED ELECTRONIC ASSEMBLY REQUIRED THAT THE CONFORMAL COATING BE REMOVED LOCALLY. TESTS WITH A MICRO-BLASTER USING SODIUM BICARBONATE OR CALCIUM CARBONATE AS THE ABRASIVE SHOWED STATIC CHARGE BUILD-UP OF 1000 VOLTS. ABRASIVE BLASTING TO REMOVE CONFORMAL COATINGS FROM ELECTRONIC MODULES CONTAINING STATIC-SENSITIVE PARTS SHOULD BE AVOIDED.

(6) HYBRID FACILITY

TYPICALLY HYBRID CIRCUITS ARE HANDLED AND PROCESSED IN GLASS PETRIE DISHES, AND THE INDIVIDUAL DICE ARE CARRIED IN MULTI-CELL FLUROWARE DISHES. ALSO, THE COVERS USED FOR THE FLUROWARE DISHES ARE MADE OF HIGH DIELECTRIC MATERIALS THAT HOLD LARGE CHARGE POTENTIALS ON THEIR SURFACE. THE PRINCIPAL CHARACTERS INFLUENCING THE CHARGE GENERATION IN THE HYBRID LABORATORIES ARE: DRY NITROGEN, HUMAN HANDS, RUBBER FINGER COTS, AND COTTON GLOVES IN CONJUNCTION WITH THE GLASS AND PLASTIC FLUROWARE DISHES.

(7) OTHER PROCESSES CREATING STATIC CHARGES

TESTING IN TEMPERATURE CHAMBERS WHERE AIR FLOW IS CIRCULATED OVER PARTS OR ASSEMBLIES CAN CREATE SUBSTANTIAL ELECTROSTATIC CHARGES. ANY SPRAYING ACTION SUCH AS SPRAY CLEANERS, SPRAY PAINTING, SPRAY COATING, SAND BLASTING, OR THE USE OF LAMINAR FLOW CHAMBERS FOR "CLEAN" ASSEMBLY CAN ALSO RESULT IN THE GENERATION OF HIGH CHARGES OF STATIC ELECTRICITY. ALL PROCESSING EQUIPMENT USED IN THE MANUFACTURING, ASSEMBLY OR TEST OF ELECTRONIC PARTS AND EQUIPMENT SHOULD BE MONITORED FOR THE GENERATION OF STATIC ELECTRICITY. IONIZING AND GROUNDING TECHNIQUES SHOULD BE IMPLEMENTED FOR THIS PROCESS MACHINERY TO REDUCE THE GENERATION OF STATIC ELECTRICITY TO SAFE LEVELS.

V. STATIC ELECTRIFICATION OF ELECTRICAL AND ELECTRONIC PARTS

A. GENERAL

STATIC VOLTAGES AS HIGH AS 10,000 TO 15,000 VOLTS CAN EASILY BE GENERATED BY SOMEONE WALKING ACROSS A ROOM. THESE VOLTAGE LEVELS CAN DESTROY MANY TYPES OF ELECTRONIC PARTS SUCH AS INTEGRATED CIRCUITS (ICs), DISCRETE SEMICONDUCTOR DEVICES, THICK AND THIN FILM DEVICES AND CRYSTALS.

EVEN IF ELECTRONIC PARTS WITHIN EQUIPMENT ARE PROTECTED FROM EXPOSURE TO THE DIRECT APPLICATION OF A STATIC DISCHARGE VOLTAGE BY PROTECTIVE CIRCUITRY, A NEARBY ELECTROSTATIC DISCHARGE IN THE FORM OF A SPARK CAN STILL CAUSE SUBTLE PROBLEMS. FOR EXAMPLE, THE DISCHARGE OF A STEEP WAVEFRONT HIGH CURRENT PULSE TO AN EQUIPMENT FRAME AND GROUND BUS CAN GENERATE A BROAD SPECTRUM OF ELECTROMAGNETIC INTERFERENCE (EMI). ICs AND OTHER SEMICONDUCTOR COMPONENTS HAVE BEEN KNOWN TO MALFUNCTION AND HAVE EVEN BEEN PERMANENTLY DAMAGED DURING SUCH DISCHARGES.

WHILE CATASTROPHIC FAILURES OF ICs ARE A MAJOR PROBLEM, THEY BECOME OBVIOUS RATHER QUICKLY TO THE EQUIPMENT USER. DAMAGE COULD ALSO RESULT IN PART DEGRADATION NOT DETECTABLE AT THE HIGHER ASSEMBLY LEVELS, OR LATENT DEFECTS NOT DISCERNIBLE AT THE PART LEVEL. SUCH DAMAGE COULD GO UNDETECTED UNTIL THE EQUIPMENT IS IN THE FIELD. ANOTHER EFFECT OF ESD AT THE EQUIPMENT LEVEL CAN RESULT FROM A SPARK DISCHARGE INDUCED EMI. THIS EMI CAN CAUSE TRANSIENT UPSET IN DIGITAL EQUIPMENT, BOMBING PROGRAMS, ERASING MEMORY, OR CAUSING PROCESSING ERRORS WHICH CAN BE VERY DIFFICULT TO DIAGNOSE. THE EMI FROM HIGH VOLTAGE SPARK DISCHARGES HAS ALSO BEEN KNOWN TO CAUSE HARD PART FAILURE.

SEMICONDUCTORS, MICROELECTRONIC AND HYBRID CIRCUITS ARE COMPOSED OF CONSTITUENTS SOME OF WHICH ARE PARTICULARLY SUSCEPTIBLE TO ELECTRICAL OVERSTRESS DUE TO ESD.

B. FAILURE MECHANISMS

ESD RELATED CATASTROPHIC FAILURE MECHANSISMS TYPICALLY INCLUDE:

- SECOND BREAKDOWN (THERMAL)
- METALLIZATION MELT
- DIELECTRIC BREAKDOWN
- METALLIZATION TO METALLIZATION ARC OVER
- SURFACE BREAKDOWN
- BULK BREAKDOWN
- SURFACE INVERSION

(1) SECOND BREAKDOWN (THERMAL)

SECOND BREAKDOWN IS ALSO KNOWN AS AVALANCHE DEGRADATION. SINCE THERMAL TIME CONSTANTS OF SEMICONDUCTOR MATERIALS ARE GENERALLY LARGE COMPARED WITH TRANSIENT TIMES ASSOCIATED WITH ESD PULSES, THERE IS LITTLE DIFFUSION OF HEAT FROM THE AREAS OF POWER DISSIPATION AND LARGE TEMPERATURE GRADIENTS CAN FORM IN THE PARTS. LOCALIZED PART JUNCTION TEMPERATURES CAN APPROACH MATERIAL MELT TEMPERATURE, RESULTING IN DEVELOPMENT OF "HOT SPOTS" AND SUBSEQUENT JUNCTION SHORTS DUE TO MELTING. THIS PHENOMENON IS TERMED "THERMAL SECOND BREAKDOWN." THE EMITTER-BASE JUNCTION FAILURE OF A BIPOLAR PART DUE TO AN ESD PULSE IS AN EXAMPLE OF THIS TYPE OF BREAKDOWN.

(2) METALLIZATION MELT

FAILURE CAN ALSO OCCUR WHEN ESD TRANSIENTS INCREASE PART TEMPERATURE TO MELT METAL, ESPECIALLY WHERE THE METAL STRIPS ARE OF REDUCED CROSS-SECTIONS AS THEY CROSS OXIDE STEPS. FILM RESISTORS SHOW SHIFTS IN RESISTANCE WHEN SUBJECTED TO ESD DUE TO LOCALIZED FUSING/MELTING OF THE FILM CRYSTALS. THIS RESULTS IN THE CREATION OF SMALL INTERNAL SHUNTS OF NEARBY CRYSTALS WITHIN THE RESISTOR.

(3) DIELECTRIC BREAKDOWN

WHEN A POTENTIAL DIFFERENCE IS APPLIED ACROSS A DIELECTRIC REGION IN EXCESS OF THE REGION'S INHERENT BREAKDOWN CHARACTERISTICS, A PUNCTURE OF THE DIELECTRIC OCCURS. THIS FORM OF FAILURE COULD RESULT IN EITHER TOTAL OR LIMITED DEGRADATION OF THE PART DEPENDING ON THE PULSE ENERGY. FOR EXAMPLE THE PART COULD EXPERIENCE A PUNCH THROUGH THE DIELECTRIC CARRYING METAL (SHORTING THROUGH) OR THE PART DIELECTRIC COULD HEAL FROM A VOLTAGE PUNCH THROUGH IF THE ENERGY IN THE PULSE IS INSUFFICIENT TO CARRY METAL THROUGH THE PUNCTURE. IN THE LATTER CASE, HOWEVER, THE PART WILL USUALLY EXHIBIT LOWER BREAKDOWN VOLTAGE OR INCREASED LEAKAGE CURRENT AFTER SUCH AN EVENT, BUT NOT TOTAL PART FAILURE. THIS TYPE OF FAILURE COULD RESULT IN A LATENT DEFECT WHERE TOTAL FAILURE OCCURS WITH CONTINUED USE, AS METAL MIGRATES THROUGH THE PUNCTURE. THE BREAKDOWN VOLTAGE OF AN INSULATING LAYER IS A FUNCTION OF THE PULSE WIDTH TIME SINCE TIME IS REQUIRED FOR AVALANCHING OF THE INSULATING MATERIAL.

(4) METALLIZATION TO METALLIZATION ARC-OVER

IN MICROCIRCUIT METALLIZATION, SPACINGS ARE TYPICALLY DESIGNED TO WITHSTAND VOLTAGES WELL BEYOND THE RATINGS OF THE SEMICONDUCTOR JUNCTIONS. HOWEVER, METALLIZATION DEFECTS SUCH AS DISPLACEMENT OF IRREGULARITIES CAN RESULT IN SITUATIONS WHERE METALLIZATION SPACING IS MINIMAL, AND THE POSSIBILITY FOR ARC-OVER IS PRESENT WHEN SUBJECTED TO AN ESD. THE ARC OVER FAILURE MODE IS NOT COMMON, SINCE THE SEMICONDUCTOR JUNCTIONS WILL USUALLY FAIL AT MUCH LOWER VOLTAGE THRESHOLDS THAN THAT NEEDED FOR ARC-OVER.

(5) SURFACE BREAKDOWN

FOR PERPENDICULAR JUNCTIONS THE SURFACE BREAKDOWN IS EXPLAINED AS A LOCALIZED AVALANCHE MULTIPLICATION PROCESS CAUSED BY NARROWING

OF THE JUNCTION SPACE CHARGE LAYER AT THE SURFACE. THE SURFACE BREAKDOWN RESULTS IN A HIGH LEAKAGE PATH AROUND THE JUNCTION, THUS NULLIFYING THE JUNCTION ACTION. ANOTHER MODE OF SURFACE FAILURE IS THE OCCURRENCE OF AN ARC AROUND THE INSULATING MATERIAL WHICH IS SIMILAR TO METALLIZATION TO METALLIZATION ARC-OVER EXCEPT IN THIS CASE ARC-OVER IS BETWEEN METALLIZATION AND SEMICONDUCTOR.

(6) BULK BREAKDOWN

BULK BREAKDOWN RESULTS FROM CHANGES IN JUNCTION PARAMETERS DUE TO HIGH LOCAL TEMPERATURES WITHIN THE JUNCTION AREA. SUCH HIGH TEMPERATURES RESULT IN METALLIZATION ALLOYING OR IMPURITY DIFFUSION RESULTING IN DRASTIC CHANGES IN JUNCTION PARAMETERS. THE USUAL RESULT IS THE FORMATION OF A RESISTANCE PATH ACROSS THE JUNCTION. THIS EFFECT IS USUALLY PRECEDED BY SECOND BREAKDOWN.

(7) SURFACE INVERSION

ESD CAN CAUSE FAILURES OF ENCAPSULATED MOS LSI CHIPS IN HERMETIC PACKAGES WITH NON-CONDUCTIVE LIDS. FAILURES ARE INDUCED BY STATIC CHARGES OR FIELDS SUCH AS ARE CREATED BY RUBBING OR FREEZE SPRAYING THE LID OF THE PACKAGE WITH A CANNED COOLANT. THE INDUCED CHARGES IN THE CHANNEL CAUSE THE FORMATION OF INVERSION LAYER LEAKAGE PATHS. THE FORMATION OF LOCAL LEAKAGE PATHS GIVES RISE TO THE ISOLATED CIRCUIT FAILURES. THIS TYPE OF FAILURE IS ALSO SIMULATED BY RUBBING THE TOP OF THE LID WITH TISSUE PAPER OR BY APPLYING A HIGH ELECTROSTATIC VOLTAGE TO THE LID. THIS FAILURE MODE CAN BE REVERSED UNDER STRONG ULTRAVIOLET EXPOSURE (FOR LIDS TRANSPARENT TO UV) OR BY DEIONIZED WATER RINSE. FAILURE CAN BE PREVENTED BY GROUNDING THE BOTTOM SURFACE OF THE LID OVER THE DIE OR BY NOT SUBJECTING THE PART TO FREEZE SPRAY OR OTHER CHARGING MECHANISMS.

C. LATENT/DEGRADATION DAMAGE FAILURE MECHANISMS

ESD CAN INDUCE LATENT OR DEGRADATION FAILURE MECHANISMS IN BOTH MOS STRUCTURES AND BIPOLAR JUNCTIONS OF DISCRETE PARTS AND MICROCIRCUITS. THESE FAILURE MECHANISMS RESULT IN MINIMAL DAMAGE AND SUBTLE PERFORMANCE DEGRADATION OF THE PART WHICH WEAKENS THE PART, EVENTUALLY LEADING TO A CATASTROPHIC FAILURE. THE ESD OVERSTRESS CAN PRODUCE A DIELECTRIC BREAKDOWN OF A SELF-HEALING NATURE WHEN THE CURRENT IS NOT LIMITED AS DISCUSSED UNDER THE DIELECTRIC BREAKDOWN FAILURE MECHANISM. WHEN THIS OCCURS, THE PART MAY RETEST GOOD BUT CONTAIN A HOLE IN THE GATE OXIDE. WITH USE, METAL WILL EVENTUALLY MIGRATE THROUGH THE PUNCTURE RESULTING IN A SHORTING THROUGH THIS OXIDE LAYER. THIS TYPE OF FAILURE MECHANISM IS ALSO REPORTED ON BIPOLAR INTEGRATED CIRCUITS WHERE V_{CC} METALLIZATION AND LOW RESISTANCE DIFFUSION CROSSOVERS SEPARATED BY THIN OXIDE FORM A MOS STRUCTURE WITH LITTLE OR NO CURRENT LIMITING.

A LATENT DEFECT DUE TO ESD CAN RESULT IN A ROUND-OFF OF THE KNEE OF THE BREAKDOWN CURVE OR AN INCREASE IN LEAKAGE IN A P-N JUNCTION. THIS CAN RESULT IN A LOWERED DAMAGE THRESHOLD WHERE A SUBSEQUENT, LOWER VOLTAGE ESD CAN RESULT IN FURTHER DEGRADATION OR A CATASTROPHIC FAILURE.

THESE FAILURE MECHANISMS ALONG WITH LATENT FAILURES ARE DISCUSSED IN MORE DETAIL IN THE DOD HANDBOOK ON ESD CONTROL PROGRAM (REFERENCE 10). SOME TYPICAL FAILURE MODES AND MECHANISMS RESULTING FROM ELECTROSTATIC DISCHARGE ARE ILLUSTRATED BELOW. THE EXAMPLES INCLUDE ESD DAMAGE OF J-FET, TTL, HYBRID, ECL, OPERATIONAL AMPLIFIER AND MOS LSI CIRCUITS.

D. EXAMPLES OF ESD FAILURES

(1) J-FET DEVICES

FREEMAN AND BEALL (REFERENCE 11) REPORTED THE FAILURE OF A 2N3970 N-CHANNEL J-FET WHICH HAS A TYPICAL GATE TO DRAIN AND GATE-TO-SOURCE

BREAKDOWN OF 80 TO 100 V AND A TYPICAL LEAKAGE CURRENT OF 100 pAMP AT 40 V. THE FET WAS SUBJECTED TO A SINGLE ELECTROSTATIC DISCHARGE FROM AN RC CIRCUIT OF C_H = 150 PF; R_H = 2KΩ WITH C_H CHARGED TO A POTENTIAL OF 6000 V. THE DISCHARGE CURRENT WAS APPLIED BETWEEN THE GATE AND THE SOURCE, PLACING THE JUNCTION IN REVERSE BREAKDOWN. THE RESULTING DAMAGE CAUSED A DEGRADATION IN THE REVERSE BREAKDOWN VOLTAGE FROM 83 TO 28 V. THIS CHANGED THE PART CHARACTERISTICS SUCH THAT THE JUNCTION BREAKDOWN NOW OCCURRED BELOW THE LEAKAGE TEST VOLTAGE OF 40 VOLTS. THIS SIGNIFICANT DECREASE IN JUNCTION BREAKDOWN VOLTAGE WOULD PRODUCE A CATASTROPHIC HARDWARE FAILURE IN MOST APPLICATIONS. THE SIZE AND VISIBILITY OF THE FAILURE SITE FROM PART TO PART IS DEPENDENT ON THE RATE OF ENERGY DISCHARGE (CURRENT DISSIPATED AT THE FAILURE POINT), QUANTITY OF CHARGE DISSIPATED AT THAT FAILURE POINT (RELATIVE TO THE SIZE OF THE CAPACITOR IN THE TEST CIRCUIT), LENGTH OF THE BREAKDOWN PATH, AND THE BREAKDOWN CHARACTERISTIC OF THE SPECIFIC PART.

THE CHANGE IN BREAKDOWN CHARACTERISTIC WAS DUE TO MICRODIFFUSION AT THE SILICON/SiO_2 INTERFACE AS SHOWN IN FIGURE 5.1.

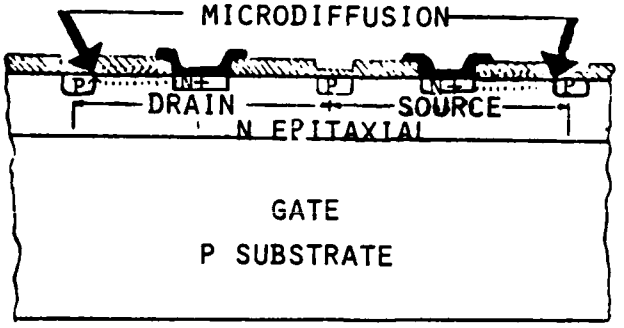


FIGURE 5.1: N-CHANNEL J-FET CROSS SECTIONAL DIAGRAM

(2) LOW POWER TTL CKT

ANOTHER EXAMPLE REPORTED BY THE SAME AUTHOR (REFERENCE 11) IS A 54L04 HEX INVERTER, LOW POWER TTL CIRCUIT. THIS FAILURE MODE OCCURRED IN A HYBRID CIRCUIT APPLICATION IN A DIGITAL COMMAND CONTROL CIRCUIT OF A PHOTO SENSOR ARRAY THIN FILM HYBRID. THIS HYBRID CIRCUIT WAS AN INTEGRAL PART OF THE ELECTRONICS FOR THE VIKING '75 LANDER CAMERA. THE PACKAGE WAS 2 INCHES IN DIAMETER AND WEIGHED A TOTAL OF 2 OZ. IT CONTAINED 100 ELECTRONIC CHIPS, 40 DISCRETE COMPONENTS, AND APPROXIMATELY 900 WIRE BONDS PER PACKAGE.

THE REPORTED FAILURE WAS A LACK OF RESPONSE TO A DIGITAL COMMAND SIGNAL. THE CIRCUIT OUTPUT WOULD NOT SWITCH TO LOW. ALL CIRCUIT NODE VOLTAGES APPEARED TO RESPOND NORMALLY TO AN INPUT DIGITAL SIGNAL EXCEPT THE COLLECTOR OF ONE TRANSISTOR IN ONE OF THE INVERTER STAGES OF A LOW-POWER TTL HEX INVERTER (FIGURE 5.2). THE Q_2 COLLECTOR REMAINED HIGH ($\approx$ 5V), AND EXHIBITED THE APPEARANCE OF AN OPEN COLLECTOR CONTACT. THE IN-CIRCUIT Q_2 BETA WAS NOTED TO BE APPROXIMATELY 2 (COMPARED TO 15-20 FOR A GOOD TRANSISTOR OF THIS TYPE) AT A COLLECTOR CURRENT OF 150 μAMP. THE TRANSISTOR WAS ISOLATED FROM THE CIRCUITRY AND THE EMITTER-BASE LEAKAGE TESTED AT 2 μAMP AT 5V AS COMPARED TO LESS THAN 6 NAMP AT 5V FOR THE OTHER FIVE INVERTERS. IN ADDITION, THE BREAKDOWN VOLTAGE KNEE FOR THE FAILED EMITTER-BASE JUNCTION WAS VERY SOFT.

AN ELECTROSTATIC DISCHARGE SUSCEPTIBILITY TEST WAS CONDUCTED WITH A NEW PART AND THE FAILURE MECHANISM WAS REPRODUCED IN INVERTER CIRCUITS AT CHARGES OF 2500 TO 3000 V. THE DISCHARGE CURRENT WAS INTRODUCED BETWEEN THE INPUT (NEGATIVE) AND GROUND. IT WAS CONCLUDED THAT THE DAMAGE WAS DUE TO MICRODIFFUSION IN THE EMITTER-BASE JUNCTION AT THE Si/SiO_2 INTERFACE (FIGURE 5.3).

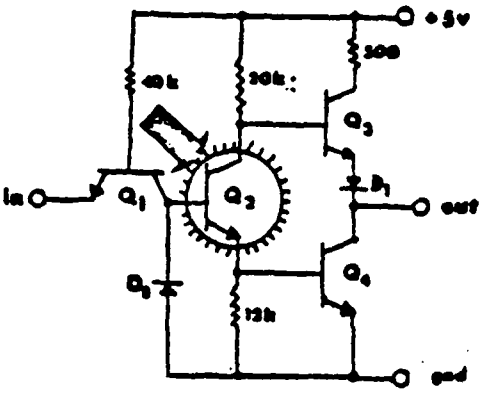


FIGURE 5.2: 54L04 TTL GATE SCHEMATIC

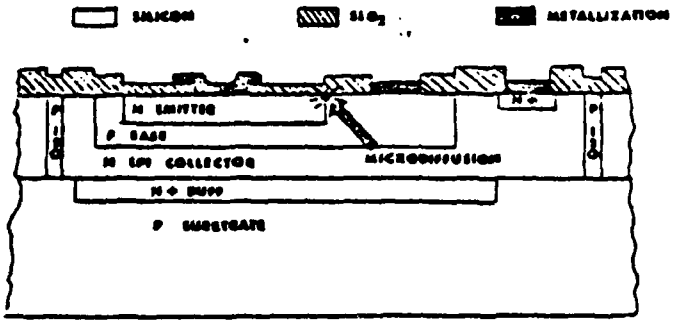


FIGURE 5.3: CROSS SECTIONAL DIAGRAM OF Q_2

(3) BIPOLAR, HYBRID AND ECL DEVICES

McATEER (REFERENCE 12) STUDIED THE ELECTROSTATIC DAMAGE TO HYBRID ASSEMBLIES INCLUDING BIPOLAR DEVICES, THIN FILM SUBSTRATES, ECL AND CMOS DEVICES. EXAMPLES DISCUSSED HEREIN WILL ILLUSTRATE CERTAIN SUBTLE ASPECTS ASSOCIATED WITH THESE ESD FAILURES.

(a) ESD EFFECTS ON BIPOLAR DEVICES

THE MOST FREQUENT FAILURE MODE OF BIPOLAR OPERATIONAL AMPLIFIER CHIPS INTENDED FOR HYBRID USAGE WAS DAMAGE TO THE INPUT TRANSISTOR PAIR. IN THE MOST SEVERE CASES, THE BASE-EMITTER JUNCTION WAS DEGRADED TO A LOW RESISTANCE SHORT OR THE REVERSE CHARACTERISTIC CURVE WAS SHIFTED BY SEVERAL TENTHS OF A VOLT. THE ESD DAMAGE WAS SIMULATED BY A PERSON SEATED AT THE WORK BENCH GETTING UP FROM THE LAB STOOL AND TOUCHING THE 14 PIN DIP PACKAGE LID WHILE IN A STANDING POSITION. THIS MOTION HAD BUILT UP A SUFFICIENT STATIC VOLTAGE ON THE PERSON'S BODY TO DESTROY THIS DEVICE. THE PATH OF THE TRANSIENT WAS FROM THE CHARGED PERSON'S FINGER TO THE PACKAGE LID WHICH IS ELECTRICALLY TIED TO THE PACKAGE BOTTOM AND TO THE CHIP SUBSTRATE. FROM THE SUBSTRATE THE PATH WAS THROUGH A P-N JUNCTION TO THE COLLECTOR OF THE N-P-N CURRENT SOURCE TRANSISTOR (Q14) TO THE EMITTER AND THEN THE BASE OF THE INPUT TRANSISTOR (Q1 OR Q2) (FIGURE 5.4). DETAILED PHYSICAL ANALYSIS INDICATED THE ESD FAILURE MECHANISM WAS DUE TO ALUMINUM TRANSPORT WHICH OCCURRED AT THE Si/SiO_2 INTERFACE, AND THERMAL CRACKING OF THE LOW TEMPERATURE GROWN SiO_2 OVERCOAT.

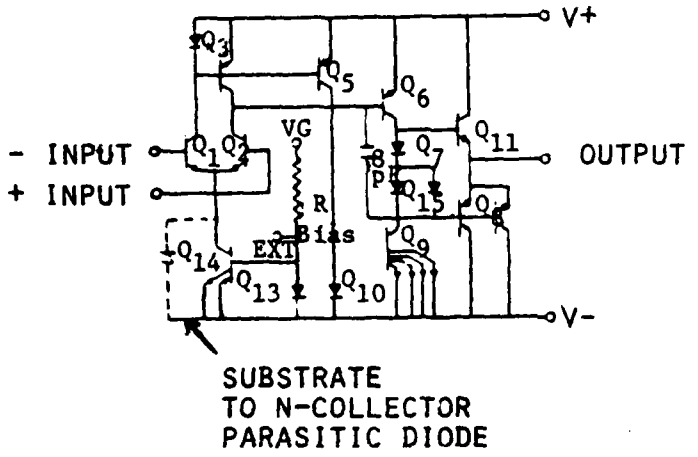


FIGURE 5.4: BIPOLAR OPERATIONAL AMPLIFIER CIRCUIT DIAGRAM

(b) SHORTED SUBSTRATES (HYBRIDS)

AN ESD SHORTING PROBLEM WAS REPORTED IN HYBRID UNITS CONTAINING COMPLEX CMOS CHIPS MOUNTED ON SAPPHIRE THIN FILM SUBSTRATES WITH TWO METALLIZATION INTRACONNECTING LAYERS. IN EACH CASE THE SHORTS WERE ISOLATED TO SCRATCHED METALLIZATION CROSSOVERS ON THE SAPPHIRE SUBSTRATE. THE CMOS CHIPS ON THE FAILED SUBSTRATE WERE STILL FUNCTIONAL. HOWEVER, THE SCRATCHES AT THE CROSSOVERS MADE THE SUBSTRATES VERY SUSCEPTIBLE TO DAMAGE FROM LOW LEVEL STATIC VOLTAGES OR TRANSIENTS.

(c) STATIC DAMAGE TO ECL DEVICES

SIMILAR FAILURES WERE NOTICED ON EMITTER-COUPLED LOGIC (ECL) PARTS AT THE PRINTED CIRCUIT BOARD LEVEL. THE SYMPTOM WAS SEVERAL TENTHS OF A VOLT SHIFT IN ONE EMITTER (OR) OUTPUT OF A DUAL-FOUR-INPUT GATE DEVICE. CURVE TRACER MEASUREMENT INDICATED A 100Ω TO 500Ω RESISTIVE SHORT BETWEEN EMITTER OUTPUT AND V_{CC}. SINCE THE OUTPUT CAME TO AN EXTERNAL PRINTED CIRCUIT BOARD JACK, STATIC ELECTRICITY WAS THE PRIME SUSPECT. THIS FAILURE WAS SIMULATED WITH A 200 PF, 1KΩ RC TEST CIRCUIT CHARGED TO 500 V. DETAILED PHYSICAL ANALYSIS INDICATED THE DAMAGE WAS DUE TO PUNCTURE OF THE OXIDE OVER THE E-B JUNCTION NEAR ONE END OF EACH EMITTER CONTACT AREA.

(4) OPERATIONAL AMPLIFIERS

TRIGONIS (REFERENCE 13) REPORTED THE ESD FAILURE OF A HIGH PERFORMANCE OPERATIONAL AMPLIFIER EMPLOYING DIELECTRIC ISOLATION AND MOS CAPACITORS FOR INTERNAL COMPENSATION (FIGURE 5.5). A FUNCTIONAL TEST OF THE FAILED PART INDICATED THE OUTPUT VOLTAGE OF THE AMPLIFIER WOULD LATCH-UP AT SLIGHTLY BELOW THE POSITIVE SUPPLY VOLTAGE. CIRCUIT ANALYSIS COMBINED WITH INTERNAL ELECTRICAL PROBING AND CIRCUIT ISOLATION FOUND A 400Ω SHORT ACROSS THE C_2 MOS CAPACITOR. A SCANNING ELECTRON MICROSCOPE VIEW OF THE FAILED SITE INDICATED AN ESD PUNCH THROUGH IN THE C_2 AREA

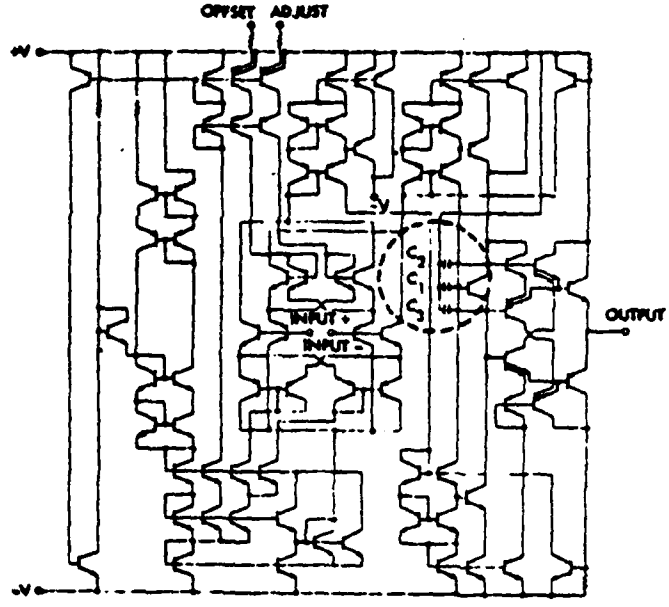


FIGURE 5.5: SCHEMATIC DIAGRAM OF A HIGH PERFORMANCE OPERATIONAL AMPLIFIER

A HIGH SLEW RATE OPERATIONAL AMPLIFIER, SHOWN IN FIGURE 5.6, EXHIBITED SIMILAR FAILURES. THIS AMPLIFIER HAS A SMALL C_2 MOS CAPACITOR CONNECTED BETWEEN THE BANDWIDTH CONTROL AND POSITIVE POWER SUPPLY TERMINALS. A RESISTIVE SHORT OF 50Ω WAS MEASURED ACROSS THIS CAPACITOR. HOWEVER, THE SURFACE DAMAGE WAS ONLY EVIDENT AFTER THE METALLIZATION WAS REMOVED.

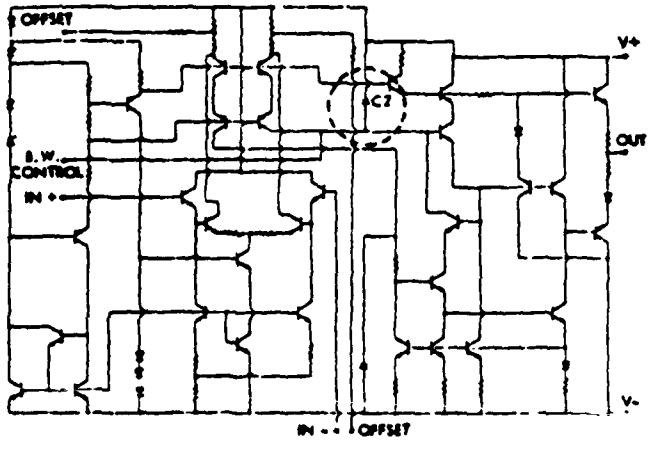


FIGURE 5.6: SCHEMATIC DIAGRAM OF A HIGH SLEW RATE OPERATIONAL AMPLIFIER

(5) MOS LSI CIRCUITS

ELECTROSTATIC DISCHARGE TEMPORARILY AFFECTS (UV RECOVERABLE) MOS LSI COMPONENTS IN HERMETIC PACKAGES WITH NON-CONDUCTIVE LIDS (REFERENCE 14). THIS FAILURE IS OBSERVED ON UV EPROMS (UV ERASABLE, ELECTRICALLY PROGRAMMABLE) WHERE FAILED PARTS EXHIBITED BOTH PROGRAMMED BITS THAT APPEARED UNPROGRAMMED AND UNPROGRAMMED BITS THAT APPEARED PROGRAMMED. FAILURE CAN BE INDUCED BY SPRAYING PACKAGE LIDS WITH CANNED COOLANT (E.G., FREON 12).

THE POSITIVE CHARGE FROM THE FREEZE SPRAY IMPINGING ON THE TOP OF THE LID INDUCES A POSITIVE CHARGE ON THE BOTTOM OF THE INSULATING PORTION OF THE LID. THE MECHANISM BY WHICH THE POSITIVE CHARGE IS INDUCED ON THE BOTTOM OF THE LID BY THE FREEZE SPRAY IS CONJECTURED TO BE THE COMBINATION OF COLD-INDUCED STRESS AND POSITIVE CHARGE FROM THE FREEZE SPRAY CAUSING THE LID TO BE POLARIZED. THE POSITIVE CHARGES ON THE BOTTOM OF THE LID PRODUCES A FIELD IN THE AIR GAP OF THE HERMETICALLY SEALED PACKAGE AND WHEN THE FIELD STRENGTH EXCEEDS THE BREAKDOWN STRENGTH OF AIR, LOCALIZED BREAKDOWN AND IONIZATION OCCURS. THIS CAUSES THE IONIZED STREAMERS (POSITIVE AND NEGATIVE CHARGES) TO FORM FROM THE DIE TO THE LID. THIS IS SHOWN IN FIGURE 5.7. THE POSITIVE CHARGES REACHING THE DIE SURFACE DUE TO THIS IONIZATION ATTRACTS THE NEGATIVE CHARGES FROM THE BULK SEMICONDUCTOR TOWARD THE LID. THESE POSITIVE CHARGES, IN TURN, CAUSE THE FORMATION OF INVERSION LAYER LEAKAGE PATHS. THE FORMATION OF LOCAL LEAKAGE PATHS GIVES RISE TO THE ISOLATED CIRCUIT FAILURES THAT HAVE BEEN OBSERVED.

THE FAILURE MODE DISCUSSED ABOVE CAN BE RECOVERED FOR UV TRANSPARENT LIDS UNDER STRONG UV EXPOSURE ($<2900A^{O}$). THE UV RECOVERY OF INVERSION LAYER LEAKAGE IN N-CHANNEL PARTS IS DUE TO PHOTOEXCITED ELECTRONS FROM THE P+ SILICON FIELD REGIONS RATHER THAN FROM N+ POLYSILICON LINES OR

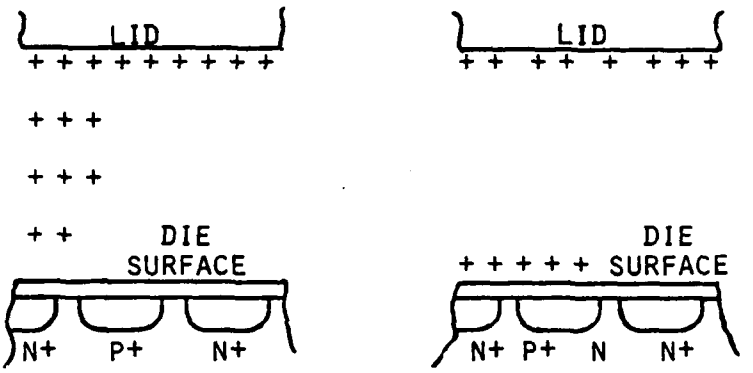


FIGURE 5.7: AIR GAP BREAKDOWN AND SURFACE CHARGING MODEL FOR FAILURES: (A) LOCALIZED AIR BREAKDOWN; (B) LOCALIZED SURFACE CHARGING

ALUMINUM METAL LINES. THESE PHOTOEXCITED ELECTRONS FROM THE SILICON ARE TRANSPORTED THROUGH THE OXIDE, PYROGLASS, AND PYROX LAYERS TO THE OUTER SURFACE OF THE DIE WHERE THEY NEUTRALIZE THE ATTRACTIVE POSITIVE IONS. FOR THE CASE OF THE P-CHANNEL UV EPROM CELL, MOST OF THE ELECTRONS, WHICH NEUTRALIZE THE POSITIVE SURFACE CHARGE ABOVE THE FLOATING GATE, ARE ACTUALLY PHOTOEXCITED FROM THE FLOATING GATE. THUS NEUTRALIZATION OCCURS AT THE EXPENSE OF DISCHARGING THE FLOATING GATE ON ALMOST A ONE-FOR-ONE BASIS. THEREFORE, THE NET CHARGE SEEN BY THE P-CHANNEL REGION OF THE MEMORY CELL CHANGES VERY LITTLE DUE TO UV EXPOSURE.

(6) THICK FILM RESISTOR

THE ELECTROSTATIC EFFECTS ON FILM RESISTORS IS DIRECTLY PROPORTIONAL TO THE SHEET RESISTIVITY AND INVERSELY PROPORTIONAL TO THE ASPECT RATIO (LENGTH/WIDTH) AND PHYSICAL SIZE (REFERENCE 15). STATIC ELECTRICITY HAS THE MOST PRONOUNCED EFFECT (AS MUCH AS 50% CHANGE IN RESISTANCE) ON THICK FILM RESISTORS THAT ARE SMALLER THAN 40 MILS SQUARE AND HAVING A SHEET RESISTIVITY OF SEVERAL THOUSAND OHMS. ENCAPSULATED THIN FILM RESISTORS APPEAR TO BE LESS AFFECTED DUE, PERHAPS, TO THEIR GENERALLY LOWER SHEET RESISTIVITY OR TO THE HOMOGENEITY OF THE METALLIC FILM.

FOR THE ELECTRICAL MODEL OF THE HETEROGENEOUS THICK FILM RESISTOR, IT IS DIFFICULT TO PINPOINT THE EXACT MECHANISM OF RESISTANCE CHANGE, BUT THERE IS SUFFICIENT EVIDENCE TO POSTULATE THAT THE CONDUCTION PATH OF THE THICK FILM RESISTOR IS ENHANCED.

AN ELECTROSTATIC FIELD INTRODUCES CHARGES IN THE MATERIAL OF THE RESISTOR. THESE CHARGES ARE NOT EVENLY DISTRIBUTED SINCE THE MATERIAL IS HETEROGENEOUS, AND POTENTIAL DIFFERENCE WILL VARY BETWEEN DIFFERENT AREAS. WHEN THIS POTENTIAL STRESS EXCEEDS THE DIELECTRIC BREAKDOWN VOLTAGE OF THE MATERIAL, THE DIELECTRIC WILL RUPTURE AND IF SUFFICIENT ENERGY IS PRESENT IN THE DISCHARGE, THE PARTICLES WILL FUSE (WELD) AND CREATE SHUNT PATHS. ALSO, IONIZATION OF THE RESISTOR MATERIAL CAUSED BY THE ELECTROSTATIC CHARGE WILL REDUCE THE RESISTANCE AT THE HIGH RESISTANCE JUNCTIONS.

THE NEWLY CREATED SHUNT PATHS ARE SHOWN AS HEAVY LINES IN FIGURE 5.8. FOR THICK FILM RESISTORS OF LESS THAN 600 OHMS PER SQUARE, ESD WILL CAUSE A SMALL INCREASE IN RESISTANCE. THIS IS PROBABLY DUE TO DESTRUCTION OF SOME OF THE MINUTE SHUNT PATHS. HOWEVER, RESISTORS ABOVE THIS RESISTIVITY CHANGE SIGNIFICANTLY; CHANGES IN SUCH CASES VARY IN DIRECT PROPORTION TO THE INCREASE IN SHEET RESISTANCE VALUE.

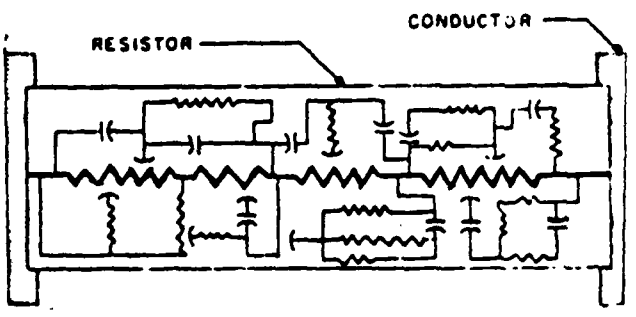


FIGURE 5.8: THICK FILM RESISTOR MATRIX REPRESENTATION BY DISCRETE SERIES-PARALLEL RESISTORS IN EQUIVALENT CIRCUIT

VI. ESD CONTROL PROGRAM

A. GENERAL

AN ESD CONTROL PROGRAM REQUIRES AN APPROACH TO ASSURE ALL PROGRAM ELEMENTS ARE INTEGRATED AS A SYSTEM, AND TO REDUCE THE ESD HAZARDS THROUGHOUT THE FACILITY, ESPECIALLY WHERE ESDS ITEMS ARE HANDLED OUTSIDE OF PROTECTIVE COVERING. THE PROGRAM SHOULD BE BOTH COST EFFECTIVE AND FUNCTIONAL. THE PROGRAM SHOULD CONSIDER EXISTING EQUIPMENT AND FACILITIES AND HOW THEY CAN BE EFFECTIVELY CONVERTED CONSISTENT WITH THE ESD CONTROL REQUIREMENTS FOR THE SENSITIVITY OF THE ESDS ITEMS INVOLVED. THE ESD CONTROLS SHOULD BE TAILORED TO THE PERSONNEL AND THE ESD FUNCTIONS THEY ARE TO PERFORM.

TRADEOFFS SHOULD BE PERFORMED TO DETERMINE A BALANCE BETWEEN THE COST OF CONSTRUCTING ESD PROTECTED AREAS AND ESD GROUNDED WORK BENCHES VERSUS THE DEGREE OF THE HANDLING PROCEDURES TO BE IMPLEMENTED TO ATTAIN THE REQUIRED CONTROLS. THE INITIAL COST OF THE PROGRAM WILL USUALLY DEPEND ON THE ELABORATENESS OF THE ESD PROTECTED AREAS. THIS COST MUST BE BALANCED AGAINST THE ESD RISKS WHICH COULD RESULT IN COSTLY REPLACEMENT OF DAMAGED ESDS PARTS AND ASSEMBLY REWORK COSTS WHERE PART DAMAGE OCCURS AT HIGHER ASSEMBLY LEVELS. FURTHER CONSIDERATIONS ARE WARRANTY COSTS AND THE COSTS RELATED TO THE DOWNTIME OF EQUIPMENT IN THE FIELD WHEN PARTS FAIL DUE TO ESD RELATED LATENT DEFECTS OR ESD DAMAGE OCCURRING DURING EQUIPMENT OPERATION OR MAINTENANCE.

B. PROGRAM REQUIREMENTS

AN ESD CONTROL PROGRAM SHOULD CONSIDER SUCH CIRCUMSTANCES IN WHICH ESDS ITEMS ARE: (1) PROCURED; (2) USED IN THE DESIGN OF HARDWARE; (3) TESTED; (4) ASSEMBLED INTO HIGHER ASSEMBLY LEVELS; (5) HANDLED AT ANY POINT IN THE FACILITY; (6) PACKAGED FOR DELIVERY; (7) STORED AT ANY POINT IN THE

FACILITY; (8) MAINTAINED OR REPAIRED IN THE FIELD OR NAVAL INTERMEDIATE OR DEPOT REPAIR FACILITIES. THIS PROGRAM SHOULD INCLUDE AS A MINIMUM, THE FOLLOWING:

(1) ESD IDENTIFICATION AND CLASSIFICATION

IDENTIFICATION OF ESDS ITEMS IS THE FIRST AND BASIC STEP IN AN ESD CONTROL PROGRAM. WITHOUT PROPER IDENTIFICATION OF ESDS ITEMS BEING USED, AN EFFECTIVE ESD CONTROL PROGRAM CANNOT BE IMPLEMENTED. THE CONTRACTOR SHOULD KNOW WHICH ITEMS HE HANDLES ARE ESDS AND THE LOWEST ESD VOLTAGE SENSITIVITY LEVEL OF THOSE ITEMS TO ESTABLISH DESIGN, HANDLING, PACKAGING, TRAINING AND PROGRAM MONITORING REQUIREMENTS, AND AS A BENCH MARK FOR DESIGNING THE ESD PROTECTED AREAS AND GROUNDED WORK BENCHES.

ESDS ITEMS SHOULD BE IDENTIFIED ON DOCUMENTATION, SUCH AS INTERNAL WORK INSTRUCTIONS. ADDITIONALLY THIS DOCUMENTATION SHOULD CONTAIN OR REFER TO AN ESD PRECAUTIONARY HANDLING PROCEDURE. THESE REQUIREMENTS NOTIFY AND REMIND THE PERSONNEL HANDLING THESE ITEMS TO DO SO IN ESD PROTECTED AREAS AND TO FOLLOW THE NECESSARY ESD PRECAUTIONS. DRAWINGS AND SPECIFICATIONS SHOULD BE SIMILARLY MARKED TO ALERT CONTRACTOR PERSONNEL IN-HOUSE DURING THE PRODUCTION PROCESS, FOR THE USER IN THE FIELD, FOR SPARES PROCUREMENT, AND FOR DEPOT ASSEMBLY REPAIR. THE TECHNICAL MANUAL SHOULD ALSO IDENTIFY THE ESDS ITEMS APPLICABLE TO THE EQUIPMENT AND PROVIDE THE NECESSARY ESD CAUTIONS AND RECOMMENDED ESD HANDLING PROCEDURES DURING EQUIPMENT MAINTENANCE. ESD EQUIPMENT TRAINING COURSE MATERIAL SHOULD PROVIDE SOME BASIC THEORY ON ESD; IDENTIFY THE ESDS ITEMS; AND LIST THE PRECAUTIONS TO BE FOLLOWED DURING MAINTENANCE, HANDLING AND PACKAGING.

SIMILARLY, MARKING OF ESDS ASSEMBLIES AND EQUIPMENT CLUE PERSONNEL TO FOLLOW ESD PRECAUTIONS DURING MAINTENANCE, HANDLING AND REPACKAGING OF FAILED ESDS ITEMS TO BE RETURNED FOR FAILURE ANALYSIS. MARKING

THE PACKAGING OF ESDS ITEMS ALERTS STOCK ROOM PERSONNEL NOT TO OPEN PACKAGING OF ESDS ITEMS AND MAINTENANCE PERSONNEL TO KEEP ESDS ITEMS IN THEIR ESD PROTECTIVE PACKAGING EXCEPT FOR REPAIRS AND FOR USE.

TO AID IN THE IDENTIFICATION OF ESDS ITEMS, DOD-STD-1686 (REFERENCE 1), AND DOD-HDBK-263 (REFERENCE 10) LIST ESDS PARTS BY TYPE AND THE GENERAL VOLTAGE RANGES AT WHICH THESE PART TYPES ARE SUSCEPTIBLE TO ESD.

(2) ESD DESIGN REQUIREMENTS

HIGHLY SENSITIVE ESDS ITEMS SHOULD CONTAIN PROTECTIVE CIRCUITRY TO REDUCE THEIR SENSITIVITY. PART MANUFACTURERS INCORPORATE PROTECTIVE CIRCUITRY ON SOME ESDS METAL OXIDE SEMICONDUCTORS, BUT OFTEN THIS PROTECTION REDUCES SENSITIVITY BY ONLY A FEW HUNDRED VOLTS. ADDITIONAL PROTECTIVE CIRCUITRY MAY BE REQUIRED AT THE ASSEMBLY AND EQUIPMENT LEVEL TO PROVIDE PROTECTION IN AREAS WHERE IT IS DIFFICULT TO MAINTAIN STATIC VOLTAGES TO LOW LEVELS. THIS PROTECTION CIRCUITRY MUST PROVIDE PROTECTION DOWN TO THE VOLTAGE LIMIT THAT CAN NORMALLY BE ACHIEVED DURING MAINTENANCE OF EQUIPMENT IN THE FIELD (E.G., 1000 VOLTS). EXTERNAL EQUIPMENT INTERFACES CONNECTED TO ESDS ITEMS SHOULD CONTAIN PROTECTION TO VOLTAGE LIMITS ACHIEVEABLE DURING EQUIPMENT HANDLING, INSTALLATION AND TEST (E.G., 4000 VOLTS). ESD PROTECTIVE CIRCUITRY IS OFTEN A TRADEOFF BETWEEN VOLTAGE PROTECTION LEVELS AFFORDED AND EQUIPMENT PERFORMANCE. MANY PROTECTIVE CIRCUITRY TECHNIQUES AFFECT THE SPEED OF THE PART OR CIRCUIT; THIS SPEED IS OFTEN CRITICAL TO EQUIPMENT PERFORMANCE.

THE DOD-STD-1686 (REFERENCE 1) DEFINES THREE BASIC DESIGN REQUIREMENTS: (1) TO RESTRICT THE USE OF HIGHLY SENSITIVE ESDS PARTS (I.E., THOSE SENSITIVE TO ELECTROSTATIC VOLTAGE LEVELS OF 1000 VOLTS OR LESS) WHERE LESS SENSITIVE ESDS PARTS ARE AVAILABLE AND CAN PERFORM THE NEEDED ELECTRICAL FUNCTION; (2) WHERE LESS SENSITIVE PARTS CANNOT BE USED,

PROTECTIVE CIRCUITRY IS REQUIRED AT THE LOWEST PRACTICABLE LEVEL OF ASSEMBLY TO PROVIDE PROTECTION TO ESDS VOLTAGE LEVELS OF 1000 VOLTS MINIMIM; AND (3) TO LIMIT THE SENSITIVITY OF EXTERNAL ELECTRICAL INTERFACES TO 4000 VOLTS.

THE 1000 VOLT REQUIREMENT IS MEANT TO PROVIDE PROTECTION TO REPLACEABLE ASSEMBLIES DURING EQUIPMENT LEVEL ASSEMBLY, TEST AND MAINTENANCE AT THE CONTRACTOR'S PLANT AND IN THE FIELD WHERE ELABORATE ESD PROTECTED AREAS (E.G., GROUNDED WORK BENCHES) CANNOT ALWAYS BE CONSTRUCTED OR IMPLEMENTED. EMPLOYING SUCH CONTROLS AS: PERSONNEL GROUNDING TECHNIQUES (PERSONNEL GROUND STRAPS OR GROUNDING BY CONTACT WITH EQUIPMENT CHASSIS); EFFECTIVE ESD HANDLING PROCEDURES, AND OTHER BASIC ESD CONTROLS SUCH AS AVOIDING THE PRESENCE OF PRIME STATIC GENERATORS, A LEVEL OF CONTROL TO 1000 VOLTS SHOULD BE READILY ACHIEVEABLE.

IT SHOULD BE NOTED THAT ADDING PROTECTIVE CIRCUITRY AT THE ASSEMBLY LEVEL DOES NOT NORMALLY PROVIDE COMPREHENSIVE PROTECTION OF ESDS PARTS. THE PARTS ARE STILL SUSCEPTIBLE TO ESD VALUES GREATER THAN THE DESIGNED-IN PROTECTION LEVEL. THESE PARTS ARE ALSO STILL VULNERABLE TO INDUCED ESD CAUSED BY SUBJECTING THE ASSEMBLY TO STRONG ELECTROSTATIC FIELDS (FOR WHICH THE PROTECTIVE CIRCUITRY IS INEFFECTIVE), OR DUE TO A CHARGED PERSON OR OBJECT TOUCHING THE ESDS PART, ELECTRICAL CONNECTIONS, OR PATHS OF A PRINTED CIRCUIT BOARD DOWN STREAM OF THE PROTECTIVE CIRCUITRY. HOWEVER, THE USE OF ESD HANDLING PRECAUTIONS AND THE USE OF ESD PROTECTIVE PACKAGING WHEN NOT WORKING ON ESDS ITEMS SHOULD PROVIDE PROTECTION AGAINST SUCH THREATS.

AS PREVIOUSLY MENTIONED, ESD SPARK DISCHARGES EMIT EMI WHICH CAN RESULT IN UPSET FAILURES OF DIGITAL EQUIPMENT. SUCH SPARK DISCHARGES ARE GENERALLY UNLIKELY TO PROVIDE HAZARDOUS EMI AT VOLTAGES BELOW 4,000 VOLTS. FOR PROTECTION IN OPERATING ENVIRONMENTS ABOVE 4,000 VOLTS THE TYPE OF EQUIPMENT MUST BE PROPERLY SHIELDED OR STEPS MUST BE

TAKEN TO LIMIT AREA STATIC VOLTAGES TO 4000 VOLTS OR LESS. THE DOD-HDBK-263 (REFERENCE 10) PROVIDES DESIGN RELATED ESD INFORMATION WITH RESPECT TO TYPES OF ESD FAILURES. ESD FAILURE MECHANISMS (INCLUDING LATENT FAILURE MECHANISMS), ESD DESIGN PRECAUTIONS AND INFORMATION ON SOME ESDS PROTECTION NETWORKS WHICH SHOULD BE HELPFUL IN HARDENING EQUIPMENT AGAINST ESD HAZARDS.

(3) ESD PROTECTED AREAS

THE DOD-STD-1686 (REFERENCE 1) REQUIREMENTS FOR THE ESD PROTECTED AREAS IS SIMPLY STATED AS FOLLOWS: "ELECTROSTATIC VOLTAGES IN AREAS WHERE CLASS 1 AND CLASS 2 ITEMS ARE HANDLED WITHOUT ESD PROTECTIVE COVERING SHALL BE LIMITED TO THE LOWEST VOLTAGE SENSITIVITY LEVEL OF THESE ITEMS AS A MINIMUM."

THIS REQUIREMENT LEAVES THE DESIGN AND CONSTRUCTION OF THE ESD PROTECTED AREA TO THE DISCRETION OF THE CONTRACTOR AS LONG AS THIS PROTECTED AREA PROVIDES THE NEEDED PROTECTION. THE DOD-STD-1686 APPENDIX A (REFERENCE 1) IDENTIFIES THE ESDS PARTS SENSITIVE TO A VOLTAGE LEVEL OF 4000 VOLTS OR LESS. THE CONTRACTOR HAVING IDENTIFIED THE ESDS PARTS PERTINENT TO A PROTECTED AREA THEN KNOWS HIS BASIC DESIGN REQUIREMENTS AND CAN PROCEED ACCORDINGLY.

THE DOD-HDBK-263 (REFERENCE 10) PROVIDES THE CONTRACTOR WITH GUIDANCE IN THE SELECTION OF ESD PROTECTIVE MATERIALS AND EQUIPMENT TO AID IN THE DESIGN OF THE ESD PROTECTED AREA. THE DOD-HDBK-263 (REFERENCE 10) ALSO PROVIDES THE CONTRACTOR WITH CONSIDERATIONS AND METHODS FOR EVALUATING THE PROPERTIES OF ESD PROTECTIVE MATERIALS AND ESD PROTECTIVE EQUIPMENT, PERSONNEL GROUNDING CONSIDERATIONS, AND THE DESIGN AND CONSTRUCTION CONSIDERATIONS FOR ESD PROTECTED AREAS.

(4) ESD HANDLING PROCEDURES

THE IMPLEMENTATION OF ESD PROTECTED AREAS ALONE DOES NOT PROVIDE THE ESD CONTROLS NEEDED TO PROTECT ESDS ITEMS FROM DAMAGE DURING THE PRODUCTION, TESTING, AND PACKAGING PROCESSES. PERSONNEL PERFORMING SUCH ACTIONS EVEN IN ESD PROTECTED AREAS SHOULD HAVE AN AWARENESS OF THE ESD PROBLEM AND IMPLEMENT THE NECESSARY ESD PRECAUTIONARY PROCEDURES. ESD PROTECTED AREAS CANNOT BE DESIGNED TO BE 100% FAIL SAFE; THE MISUSE OF ESD PROTECTIVE MATERIALS OR EQUIPMENT OR IMPROPER HANDLING PRECAUTIONS CAN STILL RESULT IN DAMAGE TO ESDS ITEMS.

THE MORE SENSITIVE THE ESDS ITEMS BEING HANDLED, THE MORE STRINGENT SHOULD BE THE HANDLING PROCEDURES. PERSONNEL ACTIONS WHICH ARE ACCEPTABLE FOR MODERATELY SENSITIVE ESDS ITEMS (E.G., CLASS 2) MIGHT PRODUCE STATIC LEVELS THAT COULD DESTROY HIGHLY SENSITIVE ESDS ITEMS (E.G., CLASS 1). THE ELABORATENESS OF THE PROTECTED AREA CAN HAVE A SIGNIFICANT EFFECT ON THE REQUIRED DETAIL OF THE ESD HANDLING PROCEDURES. FOR EXAMPLE, ESD PROTECTED AREAS IN THE FIELD COULD BE SO SIMPLIFIED IN CONSTRUCTION BECAUSE OF PHYSICAL CONSTRAINTS THAT HIGHLY DETAILED STEP-BY-STEP PROCEDURES AND PRECAUTIONS WOULD HAVE TO BE TAKEN TO LIMIT GENERATED VOLTAGES BELOW THE SUSCEPTIBILITY LEVELS OF THE ESDS ITEMS BEING HANDLED.

THE DEGREE OF ESD TRAINING ALSO IMPACTS THE LEVEL OF DETAIL NEEDED IN ESD HANDLING PROCEDURES. PERSONNEL WITH LESS TRAINING NEED THE PRECAUTIONARY MEASURES SPELLED OUT IN A MORE DETAILED STEP-BY-STEP MANNER.

THE TYPES OF ESD MATERIALS AND EQUIPMENT USED IN THE CONSTRUCTION OF AN ESD PROTECTED AREA CAN DICTATE THE PROCEDURES BY WHICH PERSONNEL HANDLE ESDS ITEMS. ALSO, THE SELECTION OF ESD PROTECTIVE MATERIALS CAN INFLUENCE THE SAFETY PRECAUTIONS PERSONNEL SHOULD OBSERVE DURING THE PROCESS OF ASSEMBLING AND TESTING ESDS ITEMS.

THE DOD-STD-1686 (REFERENCE 1) REQUIRES THAT A CONTRACTOR DEVELOP AND DOCUMENT HIS ESD PRECAUTIONARY PROCEDURES. IN SUMMARY, THE DETAIL AND EXTENT OF THESE PROCEDURES DEPENDS UPON FACTORS SUCH AS: THE SENSITIVITY OF THE ESDS ITEMS, THE ELABORATENESS OF THE ESD PROTECTED AREA, THE DEGREE OF TRAINING OF PERSONNEL, AND THE TYPES OF ESD PROTECTIVE MATERIALS AND EQUIPMENT USED.

THE DOD-HDBK-263 (REFERENCE 10) PROVIDES GENERAL GUIDELINES FOR HANDLING ESDS ITEMS AND A SAMPLE ESD OPERATING PROCEDURE FOR A FACILITY MANUFACTURING EQUIPMENT CONTAINING ESDS ITEMS. THIS SAMPLE PROCEDURE ALSO INCLUDES THE CONTRACTOR'S ORGANIZATIONS TYPICALLY AFFECTED BY AN ESD CONTROL PROGRAM, TYPICAL INTERFACING BETWEEN THESE ORGANIZATIONS AND THE BASIC DETAILED CONTROLS NEEDED TO IMPLEMENT AN EFFECTIVE ESD CONTROL PROGRAM IN STEP-BY-STEP FORMAT.

(5) ESD TRAINING

ESD AWARENESS SHOULD BE INCLUDED AS A PART OF TRAINING COURSES FOR CONTRACTOR PERSONNEL WHO DEAL WITH ESDS ITEMS, AND EQUIPMENT TRAINING COURSES FOR USER PERSONNEL. THE MOST ELABORATE ESD PROTECTED MANUFACTURING AREAS AND ESD PROTECTIVE HANDLING PROCEDURES WILL NOT PROVIDE THE PROTECTION NEEDED IF MANUFACTURING PERSONNEL ARE NOT PROPERLY TRAINED IN THEIR CORRECT USE. SUCH PERSONNEL SHOULD BE TRAINED TO EFFECTIVELY EMPLOY THE ESD PROTECTIVE MATERIALS AND EQUIPMENT IN A FACILITY AND TO UNDERSTAND THE THEORY BEHIND MANY OF THE ESD PRECAUTIONS INCLUDED IN ESD HANDLING PROCEDURES TO EFFECT THEIR USE. SINCE GROUNDING IS ONE OF THE PRIME METHODS OF CONTROLLING STATIC IN ESD PROTECTED AREAS, PERSONNEL SHOULD BE TRAINED IN GROUNDING SAFETY PRECAUTIONS. SUCH TRAINING SHOULD INCLUDE IDENTIFICATION OF ESDS ITEMS IN THE EQUIPMENT, SOME BASIC ESD THEORY, ESD HANDLING PRE-
[illegible] THE NEED FOR, USE OF AND TYPES OF ESD PROTECTIVE MATERIALS AND

EQUIPMENT, AND THE SAFETY ASPECTS INVOLVED WHERE GROUNDING IS A PART OF THE ESD HANDLING PROCEDURES.

THE DOD-STD-1686 (REFERENCE 1) REQUIRES THAT ESD AWARENESS AND PROPER HANDLING TRAINING BE GIVEN TO ALL PERSONNEL WHO SPECIFY, PROCURE, DESIGN, MANUFACTURE, ASSEMBLE, PROCESS, INSPECT, TEST, PACKAGE, REPAIR, RE-WORK, INSTALL OR MAINTAIN ESDS ITEMS. THE TRAINING SHOULD BE TAILORED TO COVER THE DEPTH AND BREADTH OF INFORMATION NECESSARY SO THAT THESE PERSONNEL CAN EFFECTIVELY PERFORM THEIR FUNCTION IN THE ESD CONTROL PROGRAM.

ESD TRAINING SHOULD BE GEARED TO THE JOB FUNCTIONS OF THE PERSONNEL BEING TRAINED. FOR EXAMPLE PROCUREMENT PERSONNEL DO NOT REQUIRE TRAINING IN AREAS WHICH DO NOT AFFECT THEIR JOB FUNCTION SUCH AS THE DESIGN AND CONSTRUCTION OF ESD PROTECTED AREAS, DESIGN CONSIDERATIONS FOR ESDS ITEMS, ESD FAILURE ANALYSIS TECHNIQUES, OR ESD HANDLING PRECAUTIONS AND PROCEDURES. THEY SHOULD, HOWEVER, HAVE AN AWARENESS TO THE EXTENT NECESSARY TO ADEQUATELY SPECIFY ESD REQUIREMENTS IN PROCUREMENTS.

THE SKILL LEVEL OF THE TRAINEES ALSO HAS A BEARING ON THE ESD TRAINING TO BE GIVEN. THE DEPTH OF THEORY ON STATIC ELECTRICITY SHOULD DEPEND ON THE TRAINEE'S ABILITY AND NEED TO COMPREHEND THE DEPTH OF INFORMATION PROVIDED. FOR EXAMPLE, ENGINEERS REQUIRE MORE THEORETICAL TRAINING FOR DE-SIGN OF PROTECTIVE CIRCUITRY THAN PACKAGING PERSONNEL NEED FOR PROTECTIVE PACKAGING OF ESDS ITEMS.

THE SENSITIVITY OF ESDS ITEMS BEING USED CAN ALSO AFFECT THE DEGREE OF TRAINING AS IT ALSO AFFECTS THE DETAIL OF THE ESD PRECAUTIONARY HANDLING PROCEDURES. SIMILARLY, ESD HANDLING PROCEDURES, DESIGN OF ESD PROTECTED AREAS AND TRAINING COMPLEMENT EACH OTHER AND CAN BE CONSIDERED IN TRADEOFFS.

ESD TRAINING PROGRAMS SHOULD ALSO BE ORIENTED TO THE CONTRACTOR'S FACILITIES AND THE TYPES OF ESD MATERIALS AND EQUIPMENT THAT HE HAS FOUND TO BE EFFECTIVE FOR HIS PARTICULAR APPLICATION.

THE DOD-HDBK-263 (REFERENCE 10) PROVIDES A SAMPLE COMPREHENSIVE ESD COURSE OUTLINE AND GUIDANCE IN TAILORING THE COURSE TO VARIOUS TYPES OF PERSONNEL. ALTHOUGH CERTIFICATION OF PERSONNEL THAT HAVE SATISFACTORILY COMPLETED THE COURSE IS NOT REQUIRED BY THE DOD-STD-1686 (REFERENCE 1), THIS IS A PREFERRED PRACTICE.

(6) ESD PROTECTIVE PACKAGING

ESDS ITEMS NOT PROPERLY PACKAGED WITH ESD PROTECTIVE MATERIAL CAN BE DAMAGED DURING TRANSPORTATION BY TRIBOELECTRIC GENERATION. FOR EXAMPLE, MOVEMENT OF THE ESDS ITEM RELATIVE TO THE PACKAGING MATERIAL AS OCCURS DURING TRANSPORTATION, VIBRATION AND SHOCK CAN RESULT IN TRIBOELECTRIC CHARGING. HANDLING OF SUCH PACKAGES BY CHARGED PERSONNEL, CONTACT WITH CHARGED OBJECTS OR SUBJECTION OF THE PACKAGE TO ELECTROSATIC FIELDS CAN ALSO DAMAGE THE ESDS ITEM WHERE ADEQUATE ESD PROTECTIVE PACKAGING IS NOT USED. SUCH PROBLEMS HAVE BEEN OBSERVED WHERE A SPARE PRINTED CIRCUIT ASSEMBLY, TESTED AND CERTIFIED WITHIN SPECIFICATION PRIOR TO LEAVING THE MANUFACTURER'S PLANT, IS IN A NON-OPERATIONAL STATE WHEN USED FOR OPERATION. AGAIN, THE IDENTIFICATION OF SUCH ITEMS AS ESDS IS PARAMOUNT. EVEN IF THE ESDS ITEM IS CORRECTLY PACKAGED, UNLESS THE PERSON RECOGNIZES THE REPLACEMENT ITEM AS ESDS HE MAY FAIL TO TAKE THE NECESSARY ESD PRECAUTIONS AS THE ESDS ITEM IS REMOVED FROM THE PACKAGING MATERIAL OR IS INSERTED IN THE EQUIPMENT, RESULTING IN ESD DAMAGE FOR THAT ITEM.

THE DOD-STD-1686 (REFERENCE 1) REQUIRES ESD PROTECTIVE COVERING AND PACKAGING. A FORM OF ESD PROTECTIVE COVERING IS REQUIRED

INTRAPLANT WHEN ESDS ITEMS ARE TRANSPORTED OUTSIDE OF AN ESD PROTECTED AREA. THIS PROTECTIVE PACKAGING MUST BE CAPABLE OF PROTECTING THE ESDS ITEMS FROM ESD DAMAGE DUE TO TRIBOELECTRIC GENERATION (GENERATION OF STATIC WITHIN THE PACKAGING BY SLIDING, VIBRATION OR OTHER MECHANICAL MOTIONS), DIRECT DISCHARGE FROM A CHARGED OBJECT OR PERSONNEL, OR ELECTROSTATIC FIELDS. THE SAME GENERAL ESD PACKAGING REQUIREMENTS WITH ADDITIONAL MARKING REQUIREMENTS ARE SPECIFIED FOR ESDS ITEMS DELIVERABLE UNDER A CONTRACT.

THE DOD-HDBK-263 (REFERENCE 10) PROVIDES APPLICATION INFORMATION ON DIFFERENT TYPES OF ESD PROTECTIVE MATERIALS INCLUDING THOSE USED FOR PACKAGING. SINCE LITTLE APPLICATION DATA RELATIVE TO PROTECTION LEVELS AFFORDED BY ESD PROTECTIVE MATERIALS ARE PROVIDED BY MATERIAL MANUFACTURERS, THIS IS ONE AREA IN WHICH THE USER SHOULD PERFORM TESTS TO IDENTIFY PACKAGING MATERIALS THAT WILL MEET THE SPECIFIED DOD-STD-1686 PACKAGING REQUIREMENTS. TECHNIQUES FOR EVALUATING CHARACTERISTICS OF ESD PROTECTIVE MATERIALS AS THEY RELATE TO TRIBOELECTRIC GENERATION, STATIC DECAY TIME AND RESISTIVITY MEASUREMENTS ARE PROVIDED IN THE DOD-HDBK-263 (REFERENCE 10).

(7) ESD CONTROL PROGRAM MONITORING

THE DOD-STD-1686 (REFERENCE 1) QUALITY ASSURANCE PROVISIONS REQUIRE THAT THE CONTRACTOR CERTIFY THE ESD PROTECTED AREAS PRIOR TO THEIR USE, AND PERFORM PERIODIC AUDITS TO ASSURE THEIR CONTINUED INTEGRITY. THE CONTRACTOR IS ALSO REQUIRED TO PERFORM AUDITS AND MONITOR THE ESD CONTROL PROGRAMS INVOKED ON SUBCONTRACTORS SUPPLYING ESDS ITEMS.

GOVERNMENT REVIEW OF THE CONTRACTOR'S ESD CONTROL PROGRAM INCLUDES FORMAL ESD DESIGN AND PROGRAM REVIEWS AND PERIODIC AUDITS.

DURING THE DESIGN PHASE, ESD DESIGN REVIEWS ARE REQUIRED AND SHOULD INCLUDE SUCH TOPICS AS: THE SELECTION AND IDENTIFICATION OF ESDS

ITEMS; ANALYSIS OF PROTECTIVE CIRCUITRY; AND THE ESD MARKING OF DOCUMENTATION AND HARDWARE.

PROGRAM REVIEWS ARE ALSO REQUIRED TO REVIEW ESD PROGRAM CONTROLS SUCH AS: THE ABILITY OF PROTECTED AREAS TO CONTROL STATIC VOLTAGE GENERATION; CONTRACTOR QUALITY CONFORMANCE PROCEDURES AS THEY RELATE TO THE ESD CONTROL PROGRAM; ESD PRECAUTIONARY PROCEDURES; CONTRACTOR ESD TRAINING PROGRAMS; AND THE PACKAGING AND LABELING OF ESDS ITEMS FOR DELIVERY.

GOVERNMENT PERSONNEL OR THEIR REPRESENTATIVES MAY PERIODICALLY MONITOR THE ESD PROTECTED AREAS, ESD HANDLING PROCEDURES, ESD DOCUMENTATION AND HARDWARE MARKING, AND ESD PROTECTIVE PACKAGING TO EVALUATE CONFORMANCE TO THE DOD-STD-1686 (REFERENCE 1).

C. TAILORING

THE DOD-STD-1686 (REFERENCE 1) ALLOWS FOR TAILORING OF THE ESD CONTROL PROGRAM ELEMENTS APPLICABLE TO A SPECIFIC TYPE OF ACQUISITION AS SHOWN IN TABLE VI-A. FOR EXAMPLE, MOST OF THE FUNCTIONS LISTED IN TABLE VI-A WOULD BE APPLICABLE, AND THE ASSOCIATED ESD CONTROL PROGRAM ELEMENTS WOULD HAVE TO BE IMPLEMENTED FOR AN ACQUISITION WHICH REQUIRES THE DEVELOPMENT, DESIGN, MANUFACTURE AND DELIVERY OF AN ENGINEERING DEVELOPMENT MODEL EQUIPMENT. LESSER ACQUISITIONS, SUCH AS PROCUREMENT OF ONLY SPARE PARTS, WOULD REQUIRE THE ESD CONTROL PROGRAM ELEMENTS APPLICABLE TO MANUFACTURING, INSPECTION AND TEST, PACKAGING, REWORK/REPAIR, AND FAILURE ANALYSIS AS APPLICABLE. THE EXTENT OF THE IMPLEMENTATION OF THESE REQUIREMENTS SHALL BE BASED, AS A MINIMUM, UPON THE VOLTAGE SENSITIVITY OF THE MOST SENSITIVE ESDS ITEMS APPLICABLE TO THE FUNCTION.

THE ACQUIRING ACTIVITY CAN MODIFY THE REQUIREMENTS OF TABLE VI-A BY SPECIFICALLY DELINEATING THE FUNCTIONS WHICH HE DEEMS APPLICABLE TO THE ACQUISTION OR CAN DELETE OR ADD ESD CONTROL PROGRAM ELEMENTS BY REFERENCE IN

TABLE VI-A

ESD CONTROL PROGRAM

FUNCTIONS APPLICABLE TO AN ACQUISITION	CONTROL PROGRAM ELEMENTS										
	IDENTIFICATION & CLASSIFICATION	DESIGN PROTECTION	PROTECTED AREAS	HANDLING PROCEDURES	PROTECTIVE COVERING	INSTALLATION SITE	TRAINING	MARKING DOCUMENTATION	MARKING HARDWARE	QA PROVISIONS, AUDITS & REVIEWS	PACKAGING FOR DELIVERY
DESIGN	X	X					X	X		X	
MANUFACTURING			X	X	X		X		X	X	
INSPECTION (EXAMINATION AND TEST)			X	X	X		X	X 1/	X	X	
PACKAGING			X	X	X 2/		X			X	X 3/
REWORK/REPAIR			X	X	X		X		X 1/	X	
FAILURE ANALYSIS			X	X	X		X			X	
TRAINING COURSES							X			X	
FIELD INSTALLATION						X 4/					
FIELD MAINTENANCE/TEST			X	X	X		X			X	

1/ IF NOT PREVIOUSLY PERFORMED;

2/ INTERNAL TO CONTRACTOR'S FACILITY;

3/ EXTERNAL TO CONTRACTOR'S FACILITY;

4/ FOR A SHIPBUILDING CONTRACT, UNLESS OTHERWISE SPECIFIED IN SUCH CONTRACT, THE INSTALLATION SITE ELEMENT IS THE ONLY ELEMENT OF THIS TABLE THAT APPLIES TO *SHIPS AND SHIPYARDS*.

THE CONTRACT. FOR EXAMPLE, FOR REPROCUREMENT OF EQUIPMENT WHICH HAS NOT PREVIOUSLY HAD THE BENEFITS OF AN ESD CONTROL PROGRAM, THE ADDITIONAL ESD REQUIREMENTS OF THE DOD-STD-1686 (REFERENCE 1) PARAGRAPHS 5.1 (IDENTIFICATION AND CLASSIFICATION OF ESDS ITEMS) AND 5.8.1 (MARKING OF DOCUMENTATION) SHOULD NORMALLY BE ADDED TO THE ESD PROGRAM ELEMENTS REQUIRED FOR MANUFACTURING, INSPECTION AND TEST, PACKAGING, REWORK/REPAIR, AND FAILURE ANALYSIS, TRAINING COURSES, FIELD INSTALLATION, AND FIELD MAINTENANCE/TEST AS APPLICABLE.

VII. ESD PROTECTIVE MATERIALS

A. GENERAL

THE PRIMARY PROTECTION AFFORDED TO ESD PARTS AND ASSEMBLIES DURING MANUFACTURE, TEST, PACKAGING AND MAINTENANCE IS PROVIDED BY ESD PROTECTED WORK AREAS AND ASSOCIATED ESD GROUNDED WORK BENCHES. THE SOPHISTICATION OF THE ESD PROTECTED AREA NEEDED DEPENDS UPON THE LEVEL OF ASSEMBLY, (E.G., PART, ASSEMBLY, OR EQUIPMENT) AND LEVEL OF MAINTENANCE (E.G., ORGANIZATIONAL, INTERMEDIATE OR DEPOT MAINTENANCE LEVELS); THE SENSITIVITY OF THE ESDS ITEMS TO BE HANDLED THEREIN AND THE PHYSICAL LIMITATIONS OF THE WORK AREA OR FACILITY. ALSO, TRADEOFFS BETWEEN THE HANDLING PROCEDURES AND PRECAUTIONS, SKILL LEVELS OF PERSONNEL AND PROTECTED AREA CONSTRUCTION SHOULD BE PERFORMED FOR AN EFFECTIVE AND EFFICIENT CONTROL PROGRAM.

OTHER THAN THE ELIMINATION OF PRIME ELECTROSTATIC GENERATORS IN WORK AREAS, THE USE OF ESD PROTECTIVE MATERIALS AND GROUNDING IS THE MOST POSITIVE METHOD OF ELIMINATING THE BUILDUP OF ELECTROSTATIC VOLTAGES. AREAS OF CONSIDERATION IN THE CONSTRUCTION OF ESD PROTECTIVE AREAS INCLUDE THE TYPES OF FLOORS, FLOOR POLISHES AND CLEANERS, BENCH TOP MATERIALS, PERSONNEL SHOES AND CLOTHING, CARTS AND ASSOCIATED WHEELS, TOOLS AND TEST EQUIPMENT, ANTISTATIC SPRAYS, HUMIDITY LEVEL, AND NUMEROUS OTHER ESD PROTECTIVE TECHNIQUES.

B. ESD PROTECTIVE MATERIALS

THERE ARE THREE BASIC TYPES OF ESD PROTECTIVE MATERIALS USED IN THE DESIGN OF ESD PROTECTED AREAS. THESE MATERIALS ARE REFERRED TO AS: CONDUCTIVE, STATIC DISSIPATIVE, AND ANTI-STATIC BASED UPON THEIR RESISTIVE PROPERTIES (REFERENCE 1).

CONDUCTIVE ESD PROTECTIVE MATERIALS ARE DEFINED AS MATERIALS HAVING SURFACE RESISTIVITIES OF 10^5 OHM PER SQUARE OR LESS. METALS, BULK CONDUCTIVE PLASTICS (CONTAINING CONDUCTIVE FILLERS OR IMPREGNATED WITH WIRES SUCH AS MIL-P-82646 (REFERENCE 16)) CAN BE CAPABLE OF MEETING THIS RESISTIVITY REQUIREMENT (EXCEPT FOR VERY THIN PIECES OF BULK CONDUCTIVE MATERIALS OR MATERIALS WITH SPARSELY WOVEN WIRES OR WIRE MESH THAT PROVIDE RESISTIVITIES OF $>10^5$ OHMS PER SQUARE).

STATIC DISSIPATIVE MATERIALS ARE DEFINED AS THOSE MATERIALS HAVING SURFACE RESISTIVITIES BETWEEN 10^5 AND 10^9 OHMS PER SQUARE. STATIC DISSIPATIVE MATERIALS COULD INCLUDE THE SAME MATERIALS AS CONDUCTIVE MATERIALS EXCEPT THAT THE THICKNESSES ARE LOWER, WIRE OR WIRE MESH INCLUDED THEREIN IS FINER OR MORE SPARSE THAN IN CONDUCTIVE MATERIALS OR VOLUME RESISTIVITIES ARE HIGHER.

ANTI-STATIC MATERIALS ARE DEFINED AS THOSE MATERIALS HAVING SURFACE RESISTIVITIES BETWEEN 10^9 AND 10^{14} OHMS PER SQUARE. THESE MATERIALS INCLUDE HYGROSCOPIC ANTI-STATIC MATERIALS (MIL-B-81705 TYPE II)(REFERENCE 17), SOME MEALMINE LAMINATES, HIGH RESISTANCE BULK CONDUCTIVE PLASTICS, VIRGIN COTTON, CELLULOSE BASED HARDBOARDS, WOOD AND PAPER PRODUCTS, AND STATIC DISSIPATIVE OR CONDUCTIVE MATERIALS HAVING VERY SMALL THICKNESSES.

MATERIALS WITH SURFACE RESISTIVITIES GREATER THAN 10^{14} OHMS PER SQUARE ARE CLASSIFIED AS INSULATIVE. TYPICALLY INSULATIVE MATERIALS ARE PRIME GENERATORS OF STATIC ELECTRICITY AND ARE RESISTIVE ENOUGH TO MAINTAIN CHARGES FOR LONG PERIODS OF TIME.

(1) MEASUREMENT OF RESISTIVE PROPERTIES OF MATERIALS

MEASUREMENT PARAMETERS COMMONLY USED IN DESCRIBING THE RESISTIVE PROPERTIES OF MATERIALS USED FOR PROTECTION AGAINST ESD ARE COMMONLY REFERRED TO AS:

VOLUME RESISTIVITY (OHMS-CM)

SURFACE RESISTIVITY (OHMS PER SQUARE)

DECAY TIME (SECONDS)

(a) VOLUME RESISTIVITY (ρ_V)

VOLUME RESISTIVITY, ALSO REFERRED TO AS BULK RESISTIVITY, IS A CONSTANT FOR A GIVEN HOMOGENEOUS MATERIAL AND IS MATHEMATICALLY DERIVED AS FOLLOWS:

FROM ELECTRICAL THEORY, THE RESISTANCE (R) OF A PIECE OF MATERIAL IS INVERSELY PROPORTIONAL TO THE CROSS-SECTIONAL AREA (A) PERPENDICULAR TO THE FLOW OF CURRENT AND DIRECTLY PROPORTIONAL TO THE LENGTH OF THE MATERIAL (L) PARALLEL TO THE FLOW OF THE CURRENT.

$$R \propto \frac{L}{A} \quad \ldots\ldots (29)$$

THEREFORE:

$$R = (\text{CONSTANT}) \frac{L}{A} \quad \ldots\ldots (30)$$

THIS CONSTANT, KNOWN AS VOLUME RESISTIVITY (ρ_V), IS PUBLISHED FOR VARIOUS HOMOGENEOUS MATERIALS, AND HAS DIMENSIONS OF OHM-CM^2/CM OR OHM-CM.

$$\rho_V = \frac{RA}{L} \quad \ldots\ldots (31)$$

THE RESISTIVITY OF A HOMOGENEOUS MATERIAL IS DETERMINED BY MEASURING THE RESISTANCE OF A PIECE OF THE MATERIAL WITH KNOWN DIMENSIONS (I.E., LENGTH (L), WIDTH (W) AND THICKNESS (t)) FOR A SQUARE PIECE OF MATERIAL "L" IS EQUAL TO "W" AND EQUATION (31) REDUCES TO:

$$\rho_V = Rt \quad \ldots\ldots (32)$$

IT IS EVIDENT FROM EQUATION (32) THAT THE RESISTANCE (R) OF A BULK CONDUCTIVE MATERIAL WITH A GIVEN ρ_V CAN BE VARIED BY VARYING THE THICKNESS OF THE MATERIAL (I.E., A BENCH TOP, TOTE BOX OR PARTS TRAY SHEET RESISTANCE CAN BE VARIED BY VARYING THE THICKNESS OF THE MATERIAL USED). ρ_V IS NORMALLY DETERMINED BY MEASURING THE RESISTANCE (R) OF A SQUARE OF MATERIAL AND MULTIPLYING THE RESISTANCE (R) BY THE THICKNESS (t) (EQUATION (32)).

(b) SURFACE RESISTIVITY

SURFACE RESISTIVITY (ρ_S) IS A MEASURE OF THE RESISTANCE (R) OF A SQUARE SECTION OF MATERIAL AND IS NORMALLY USED AS A RESISTIVITY MEASUREMENT OF A THIN CONDUCTIVE LAYER OF MATERIAL OVER A RELATIVELY INSULATIVE BASE MATERIAL. ρ_S HAS THE DIMENSIONS OF OHMS PER SQUARE AND IS MEASURED ACROSS THE SURFACE OF THE MATERIAL. ρ_S IS EQUIVALENT TO THE RESISTANCE MEASUREMENT (R) TAKEN FOR DETERMINING VOLUME RESISTIVITY FOR A SQUARE SECTION OF MATERIAL.

$\rho_S = R\,t$ (WHEN THE SURFACE AREA OF THE SPECIMEN IS SQUARE) .... (33)

OF THE TWO RESISTIVITY PARAMETERS, THE SURFACE RESISTIVITY IS THE MORE REPRESENTATIVE RESISTIVITY MEASUREMENT BECAUSE IT IS A MEASURE OF THE EFFECTIVE MATERIAL RESISTANCE FOR A GIVEN PIECE OF MATERIAL. HOWEVER, IT SHOULD BE NOTED THAT RESISTIVITY MEASUREMENTS ARE PERFORMED ON SQUARE PIECES OF MATERIAL USING THE ELECTRODES ALONG OPPOSITE SIDES OF THE MATERIAL SQUARE. MOST OBJECTS MADE OF ESD PROTECTIVE MATERIALS ARE NOT SQUARE AND NORMALLY THE ELECTRICAL POINTS OF CONTACT DO NOT ENCOMPASS THE COMPLETE OPPOSITE EDGES OF THE OBJECT. CONSEQUENTLY, SURFACE RESISTIVITY IS ONLY AN APPROXIMATION OF THE ACTUAL RESISTANCE OF THE PATH BETWEEN THE TWO ELECTRICAL CONTACT POINTS (E.G., A PERSON'S HAND OR FINGER AND A GROUND CONNECTION). THE ACTUAL RESISTANCE CAN BE CALCULATED USING EQUATION (31),

OR MEASURED WITH AN OHM OR MEGOHMMETER, USING REPRESENTATIVE ELECTRICAL CONTACT SIZES AND SHAPES TO SIMULATE THE CONTACT POINT AND THE GROUND POINT.

EXAMPLE (J): ASSUME A PERSON DISCHARGES HIMSELF BY TOUCHING A TABLE TOP HAVING A VOLUME RESISTIVITY OF 30×10^3 OHMS-CM. ASSUME THE CONTACT AREA OF THE DISCHARGE IS A PERSON'S FINGER EQUIVALENT TO A CIRCLE AND HAVING A DIAMETER OF 1 CM. THE DISTANCE FROM THE POINT OF DISCHARGE TO THE GROUND POINT OF THE TABLE TOP (CONNECTED TO A BOLT OF 1 CM DIAMETER) IS 50 CM. THE THICKNESS OF THE TABLE TOP MATERIAL IS .065 CM. FIND THE RESISTANCE TO THE GROUND POINT. FROM EQUATION (30):

$$R = \frac{\rho_V L}{A}$$

$$= \frac{(30 \times 10^3)\ (50)}{1 \times .065}$$

$$= 23 \times 10^6 \text{ OHMS}$$

NOTE THE DIFFERENCE IN THE ACTUAL RESISTANCE OF THE PATH OF THE DISCHARGE AND THE VOLUMETRIC RESISTIVITY OF THE MATERIAL.

COMBINING EQUATIONS (32) AND (33) THE SURFACE RESISTIVITY ρ_S IS EQUAL TO:

$$\rho_S = \frac{\rho_V}{t} \quad \text{..... (34)}$$

EQUATION (33) SHOWS THAT ρ_S IS NOT CONSTANT FOR A HOMOGENEOUS MATERIAL BUT ONLY FOR A SPECIFIED THICKNESS (t) OF THE CONDUCTIVE MATERIAL. THEREFORE, THE RELATIONSHIP OF ρ_S TO ρ_V IS MEANINGLESS FOR

A HOMOGENEOUS BULK CONDUCTIVE MATERIAL UNLESS THE THICKNESS (t) IS ALSO GIVEN. FROM EXAMPLE (J):

$$\rho_s = (30 \times 10^3)/(.065)$$

$$= .461 \times 10^6 \text{ OHMS/}$$

THIS IS MUCH CLOSER TO THE ACTUAL RESISTANCE OF THE DISCHARGE PATH BUT DIFFERS BY A RATIO OF THE LENGTH TO THE WIDTH OF THE DISCHARGE PATH (I.E., 50:1).

SINCE SURFACE RESISTIVITY IS COMMONLY USED AS A RESISTANCE MEASUREMENT PARAMETER OF LAMINATED MATERIALS HAVING A THIN CONDUCTIVE SURFACE OVER AN INSULATIVE BASE, IT IS USED TO MEASURE THE RESISTIVITY OF SURFACE CONDUCTIVE MATERIALS SUCH AS: HYGROSCOPIC ANTI-STATIC POLYETHELENES, NYLON AND VIRGIN COTTON (WHICH ARE SURFACE CONDUCTIVE DUE TO THE FORMATION OF A SWEAT LAYER ON THEIR SURFACE UNDER NORMAL HUMIDITY CONDITIONS); METAL OR CARBON COATED PAPER OR PLASTICS, AND OTHER CONDUCTIVELY COATED OR LAMINATED INSULATIVE MATERIALS. CONDUCTIVE LAYERS ON THESE MATERIALS ARE USUALLY OF NEAR UNIFORM THICKNESS (E.G., SWEAT LAYER OF HYGROSCOPICALLY ANTI-STATIC MATERIAL) AND THE SURFACE RESISTIVITY (OR MATERIAL RESISTANCE) DOES NOT EFFECTIVELY CHANGE BY INCREASING OR DECREASING THE THICKNESS OF THE BASE INSULATIVE MATERIAL IF ITS ρ_V IS HIGH IN RELATION TO THAT OF THE CONDUCTIVE SURFACE MATERIAL. SEE FIGURE 7.1.

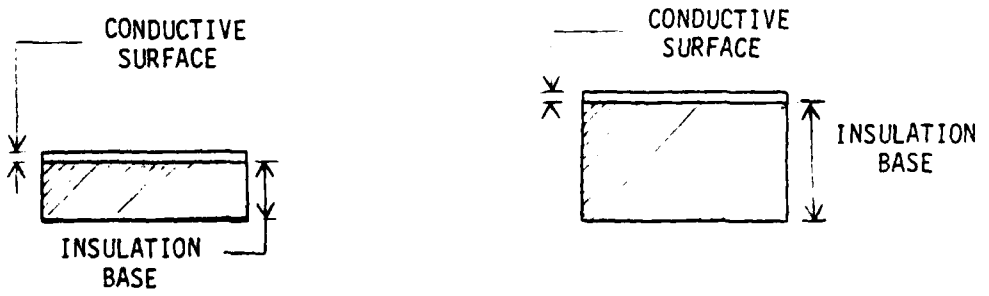


FIGURE 7.1

SURFACE CONDUCTIVE MATERIALS WITH DIFFERENT INSULATIVE BASE THICKNESSES

(c) DECAY TIME

DECAY TIME IS AN INDIRECT METHOD OF MEASURING MATERIAL SURFACE RESISTIVITY. DECAY TIME IS MEASURED BY CHARGING A SECTION OF MATERIAL WITH A STATIC VOLTAGE AND MEASURING THE TIME FOR A VOLTAGE TO DECAY TO A GIVEN LEVEL (E.G., 10% OF ITS ORIGINAL VALUE). MATERIALS WHOSE SURFACE RESISTIVITIES VARY WITH RELATIVE HUMIDITY (E.G., HYGROSCOPIC ANTI-STATIC MATERIALS) WILL SHOW VARIATIONS IN DECAY TIME AT DIFFERENT RELATIVE HUMIDITIES. DECAY TIME MEASUREMENTS ARE USED TO SPECIFY THE ELECTROSTATIC PROPERTIES FOR MIL-B-81705 (REFERENCE 17) TYPE II MATERIAL.

(d) TEST PROCEDURES FOR ESD PROTECTIVE MATERIALS

A NUMBER OF EXISTING TEST PROCEDURES FOR MEASURING RESISTIVITIES OF CONDUCTIVE, STATIC DISSIPATIVE AND ANTI-STATIC MATERIALS ARE:

(1) AMERICAN SOCIETY OF TESTING MATERIALS PROCEDURE, ASTM-D-991 (REFERENCE 18) FOR CONDUCTIVE MATERIALS (FIGURE 7.2);

(2) AMERICAN SOCIETY OF TESTING MATERIALS PROCEDURE, ASTM-D-257 (REFERENCE 19) FOR STATIC DISSIPATIVE, ANTI-STATIC AND INSULATING MATERIALS (FIGURES 7.3, 7.4 AND 7.5).

(3) THE METHOD FOR MEASURING DECAY TIME (FIGURE 7.6) IS PROVIDED IN FEDERAL TEST METHOD STANARD NO. 101, TEST METHOD NO. 4046, "ELECTROSTATIC PROPERTIES OF MATERIAL" (REFERENCE 20).

(4) FIGURE 7.7 SHOWS A SINGLE SETUP USED BY THE 3M COMPANY TO MEASURE SURFACE AND VOLUME RESISTIVITY OF CONDUCTIVE PLASTIC FILMS.

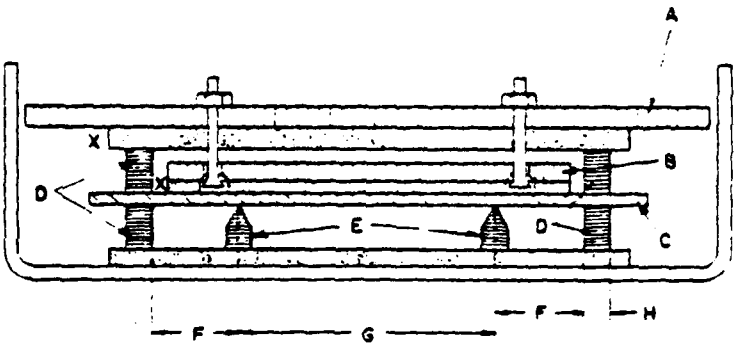
(2) ELECTROSTATIC PROTECTIVE PROPERTIES

THE MAIN PROTECTIVE PROPERTIES OF ESD PROTECTIVE MATERIALS INCLUDE (REFERENCE 1):

(a) PROTECTION AGAINST THE GENERATION OF ELECTROSTATIC CHARGES (E.G., TRIBOELECTRIC GENERATION DUE TO RUBBING OR MATERIAL SEPARATION AS MIGHT OCCUR DURING TRANSPORTATION);

(b) PROTECTION AGAINST DIRECT DISCHARGE FROM CONTACT WITH CHARGED PERSONNEL OR A CHARGED OBJECT;

(c) SHIELDING FROM ELECTROSTATIC FIELDS (THIS APPLIES TO CONTAINERS USED TO TRANSPORT AND PACKAGE ESDS ITEMS).



A—Mass for applying contact force between current electrodes and specimen (300 N·m times specimen width in meters) (Note 1)
B—Mass for applying contact force between potential electrodes and specimen (60 N·m times specimen width in meters) (Note 2)
C—Specimen
D—Current electrodes
E—Potential electrodes
F—Distance between current and potential electrodes (20 mm minimum)
G—Distance between potential electrodes (see Note 2 in Section 7) depends on specimen size.
H—Width of current electrode, 5 to 3 mm (0.2 to 0.3 in.)
X—Insulation

NOTE 1—For a specimen 150 mm (6 in.) wide, mass is approximately 4.5 kg (10 lb).

NOTE 2—For a specimen 150 mm (6 in.) wide, mass is approximately 0.9 kg (2 lb).

Electrode Assembly.

By publication of this standard no position is taken with respect to the validity of any patent rights in connection therewith, and the American Society for Testing and Materials does not undertake to insure anyone utilizing the standard against liability for infringement of any Letters Patent nor assume any such liability.

FIGURE 7.2: ELECTRODE ASSEMBLY USED IN ASTM-D-991

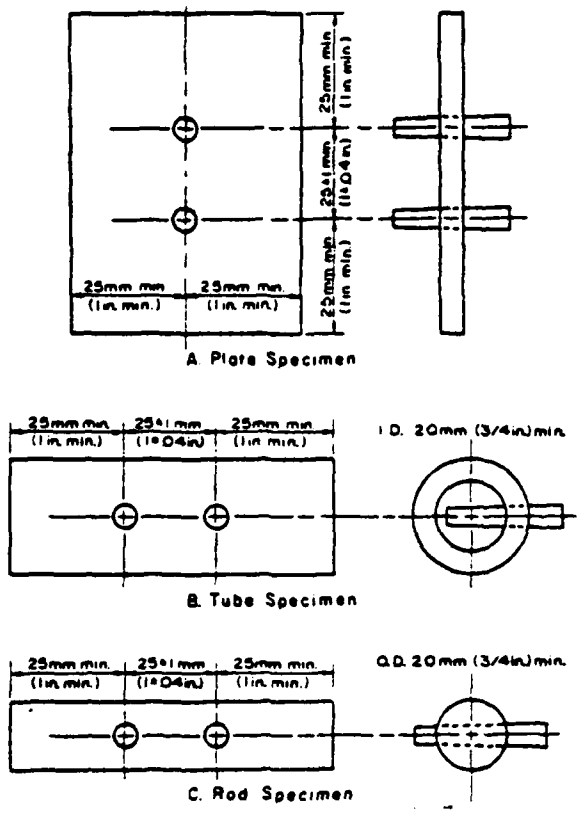


FIGURE 7.3: TAPER-PIN ELECTRODES

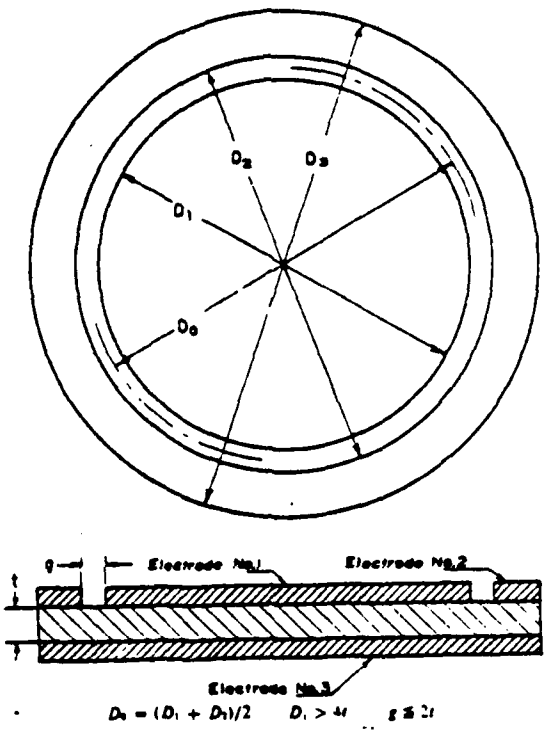


FIGURE 7.4: FLAT SPECIMEN FOR MEASURING VOLUME AND SURFACE RESISTANCES OR CONDUCTANCES

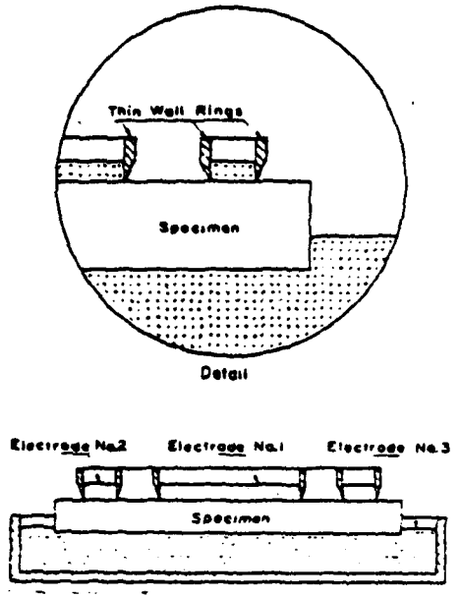


FIGURE 7.5: MERCURY ELECTRODES FOR FLAT, SOLID SPECIMENS

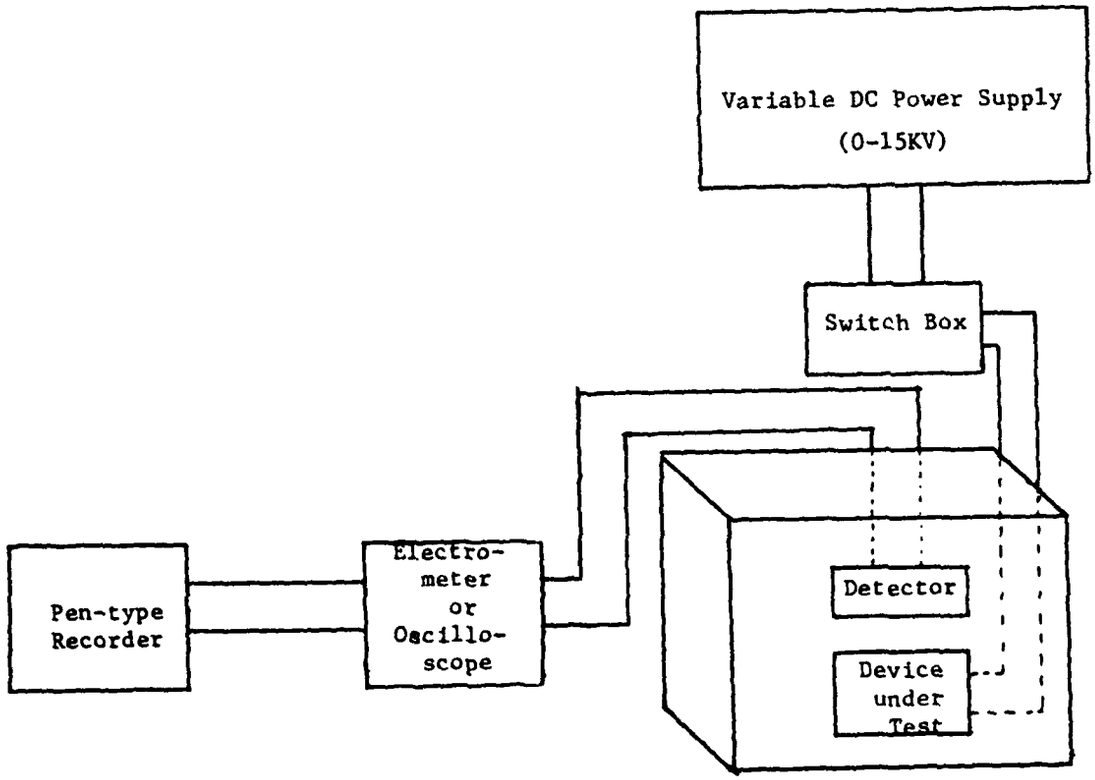


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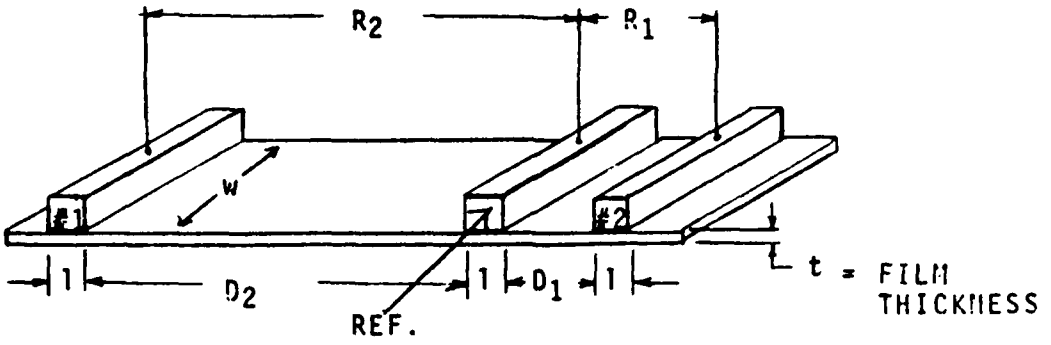
FIGURE 7.6: ELECTROSTATIC TEST CIRCUIT (FEDERAL TEST METHOD STANDARD NO. 101B, 4046)



THEORY: CONTACT OR SURFACE RESISTANCE, R_S BETWEEN THE ELECTRODES AND THE SURFACE OF CONDUCTIVE PLASTIC FILMS CAN MAKE TWO ELECTRODE TECHNIQUES INVALID FOR THE MEASUREMENT OF SURFACE AND VOLUME RESISTIVITY, ρ_S AND ρ_V. IN ORDER TO ELIMINATE THE CONTACT RESISTANCE, A THREE ELECTRODE TECHNIQUE CAN BE EMPLOYED TO GIVE QUICK AND FAIRLY RELIABLE RESULTS.

THE RESISTANCE BETWEEN THE REFERENCE ELECTRODE AND ELECTRODES NUMBERED 2 AND 1 ARE:

$$R_2 = \frac{\rho_V D_2}{tw} + R_S \text{ AND } R_1 = \frac{\rho_V D_1}{tw} + R_S$$

SINCE:

$$\rho_S = \frac{\rho_v}{t}$$

$$R_1 = \frac{\rho_S D_1}{W} + R_2 - \frac{\rho_S D_2}{W}$$

$$\rho_S = \frac{R_2 - R_1}{D_2 - D_1} \; W$$

AND

$$\rho_V = \frac{R_2 - R_1}{D_2 - D_1} \; Wt$$

IN ORDER TO ELIMINATE THE ERROR DUE TO THE SHUNTING EFFECT OF THE FILM, MEASUREMENTS MUST BE TAKEN ON A STRIP OF FILM WITH THE SAME WIDTH, W, AS THE ELECTRODES

FIGURE 7.7: MEASUREMENTS OF SURFACE AND VOLUME RESISTIVITY OF CONDUCTIVE PLASTIC FILMS USING THE THREE ELECTRODE TECHNIQUE (THE 3M COMPANY)

PROTECTION AGAINST THE GENERATION OF ELECTROSTATIC CHARGES IS ONE OF THE BEST METHODS OF ESD CONTROL. ONE OF THE PRIME CHARACTERISTICS OF MATERIALS IN REDUCING THE GENERATION OF STATIC BY TRIBO-ELECTRIC GENERATION IS LUBRICITY (SURFACE SMOOTHNESS AND MOISTNESS). THE HIGHER THE LUBRICITY OF THE SURFACES BEING RUBBED, THE LOWER THE FRICTION AND HENCE THE LOWER THE GENERATED CHARGES. MOISTNESS ON THE SURFACE OF MATERIALS BEING SEPARATED CARRY OPPOSITELY CHARGED LIQUID PARTICLES TO THE CHARGED SOURCES AND FORMS A CONDUCTIVE PATH TO ALLOW CHARGES TO FLOW BACK NEUTRALIZING THE CHARGES AS THEY ARE GENERATED.

CONDUCTIVITY IS ALSO A PRIME CHARACTERISTIC OF A MATERIAL USED TO PROVIDE PROTECTION AGAINST STATIC CHARGES. CONDUCTIVITY DISTRIBUTES CHARGES OVER MATERIAL SURFACES THUS REDUCING THE STATIC VOLTAGE LEVELS. CONDUCTIVITY IS ALSO THE PRIMARY CHARACTERISTIC OF GROUNDING APPARATUS SUCH AS PERSONNEL GROUND STRAPS, CONDUCTIVE FLOORS, CONDUCTIVE TABLE TOPS, CONDUCTIVE STOOLS, ETC. IF THE CONDUCTIVITY OF THE MATERIAL CAN BE CONTROLLED, THEN, PREVENTING STATIC ELECTRICITY BECOMES RELATIVELY EASY.

SHIELDING FROM ELECTROSTATIC FIELDS REQUIRES ENCLOSING THE ITEM TO BE PROTECTED (E.G., ESDS PART) IN A RELATIVELY CONDUCTIVE MATERIAL. NORMALLY, THE GREATER THE CONDUCTIVITY OF THE ENCLOSURE (BOX, BAG, ETC.) THE GREATER THE ATTENUATION OF THE ELECTROSTATIC FIELD THROUGH THE ENCLOSURE. THUS ESDS ITEMS SHOULD HAVE AN OVERWRAP OF CONDUCTIVE PACKAGING FOR PROTECTION AGAINST ELECTROSTATIC INDUCED FIELDS.

THE DISSIPATION OF A STATIC CHARGE INDUCED EITHER FROM AN APPROACHING CHARGED OBJECT OR PERSONNEL OR FROM DIRECT DISCHARGE FROM A CHARGED OBJECT OR PERSON GENERALLY OCCURS BY ONE OR A COMBINATION OF FIVE DIFFERENT PHENOMENA: SPARK DISCHARGE, CORONA DISCHARGE, SURFACE CONDUCTION TO GROUND, VOLUME CONDUCTION TO GROUND, AND IONIZATION PROVIDED BY IONIZATION

EQUIPMENT. IONIZERS, HOWEVER, TYPICALLY WORK QUITE SLOWLY. THEREFORE, THE TENDENCY TO BUILD UP STATIC CHARGE CAN BE DECREASED BY IONIZING THE SURROUNDING AREA TO PROMOTE CORONA DISCHARGE, INCREASING THE SURFACE ELECTRICAL CONDUCTIVITY, OR BY INCREASING THE VOLUME CONDUCTIVITY OF THE MATERIAL. IT IS OFTEN DIFFICULT TO PROMOTE CORONA DISCHARGE BY IONIZATION OF THE AIR FOR MOST IN-USE SYSTEMS, AND THEREFORE THE ACHIEVEMENT OF ANTI-STATIC BEHAVIOR IN MATERIALS IN THE ELECTRONICS INDUSTRY HAS COMMONLY BEEN ATTEMPTED BASED UPON METHODS WHICH WOULD INCREASE THE SURFACE OR VOLUME CONDUCTIVITY.

(3) THE PROS AND CONS OF CONDUCTIVITY

CONDUCTIVITY PROVIDES CHARACTERISTICS THAT ARE HIGHLY BENEFICIAL IN THE CONTROL OF STATIC ELECTRICITY. THESE CHARACTERISTICS CAN BE SUMMARIZED AS FOLLOWS (NOTE: CONDUCTIVITY IS RELATIVE AND, TO AN EXTENT, IS CHARACTERISTIC OF STATIC DISSIPATIVE AND ANTI-STATIC MATERIALS):

(a) STATIC DISSIPATIVE AND TO AN EXTENT ANTI-STATIC MATERIALS CAN BE CONDUCTIVE ENOUGH TO DISTRIBUTE CHARGES AND BLEED CHARGES TO GROUND. ONCE A CHARGE IS GENERATED THE DISTRIBUTION OF THAT CHARGE IS DEPENDENT UPON THE RESISTIVITY AND SURFACE AREA OF THE MATERIAL. THE MORE CONDUCTIVE THE MATERIAL THE FASTER THE CHARGE IS DISSIPATED. THE GREATER THE SURFACE AREA OVER WHICH A CHARGE IS SPREAD, THE LOWER THE CHARGE DENSITY AND THE LEVEL OF THE RESIDUAL VOLTAGE. IN CONTRAST TO INSULATORS, LOCALIZED CHARGES CANNOT EXIST ON CONDUCTIVE MATERIALS.

(b) CONDUCTIVITY IS ALSO A PRIME CHARACTERISTIC FOR PROVIDING PROTECTION AGAINST STATIONARY OR APPROACHING CHARGED OBJECTS OR PERSONNEL BY LIMITING ACCUMULATION OF RESIDUAL VOLTAGES. AS A CHARGED OBJECT OR PERSON APPROACHES AN OBJECT MADE OF AN ESD PROTECTIVE MATERIAL,

ELECTRONS TEND TO MOVE IN THAT MATERIAL TOWARD OR AWAY, DEPENDING UPON ITS POLARITY, FROM THE POINT OF CONTACT WITH THE CHARGED PERSON OR OBJECT, POLARIZING THAT OBJECT. THIS POLARIZATION OCCURS GRADUALLY AS THE CHARGED OBJECT OR PERSON APPROACHES LIMITING THE VOLTAGE LEVELS INDUCED ACROSS THE MATERIAL SURFACE. IN CONDUCTIVE ESD PROTECTIVE MATERIALS THESE ELECTRONS MOVE QUITE RAPIDLY WITH RESPECT TO THE SPEED OF AN APPROACHING CHARGED OBJECT RESULTING IN LOW VOLTAGES APPLIED ACROSS THE ESD PROTECTIVE MATERIAL. AS THE RESISTIVITY OF THE ESD PROTECTIVE MATERIAL (AS IN THE CASE OF STATIC DISSIPATIVE AND ANTI-STATIC MATERIALS) INCREASES THE ELECTRONS MOVE MORE SLOWLY WITH RESPECT TO THE SPEED OF AN APPROACHING OBJECT AND HIGHER VOLTAGES WILL RESULT ACROSS THE ESD PROTECTIVE MATERIAL. FOR HIGHER RESISTANCE ANTI-STATIC MATERIALS, FEWER ELECTRONS CAN MOVE TOWARD OR AWAY FROM THE APPROACHING CHARGED OBJECT OR PERSON AND SIGNIFICANT VOLTAGES COULD OCCUR ACROSS THE ANTI-STATIC MATERIAL. IF THE VOLTAGE ACROSS THE MATERIAL IS HIGH ENOUGH AND AN ESDS ITEM IS PRESENT ON THE MATERIAL (SUCH AS AN ESDS ITEM CONTAINED IN A TOTE BOX OR ON A TABLE TOP) THE INDUCED VOLTAGE COULD BE SUFFICIENT TO DAMAGE THAT ESDS ITEM.

(c) COMPLETE SHIELDING FROM ELECTROSTATIC FIELDS (OR ESD SPARK INDUCED ELECTROMAGNETIC PULSES (EMP) FOR OPERATIONAL DIGITAL EQUIPMENT REQUIRES ENCLOSING THE ESDS ITEMS IN A CONDUCTIVE MATERIAL. NORMALLY, THE GREATER THE CONDUCTIVITY OF THE ENCLOSURE THE GREATER THE ATTENUATION OF THE ELECTROSTATIC FIELD AND ESD SPARK INDUCED EMP WITHIN THE ENCLOSURE.

THERE ARE ALSO SOME PRECAUTIONS TO BE CONSIDERED IN THE USE OF CONDUCTIVE MATERIALS:

- THE PROTECTIVE CHARACTERISTICS OF MATERIALS NEEDED TO PROTECT ESDS ITEMS FROM DIRECT DISCHARGE FROM A CHARGED OBJECT OR PERSON DEPENDS UPON THE METHOD OF DISCHARGE. IF THE DISCHARGE IS THROUGH AN ESDS

ITEM A HIGH RESISTANCE TO GROUND IS BENEFICIAL IN REDUCING THE VOLTAGE ACROSS AND THE DISCHARGE CURRENT THROUGH THE ESDS ITEM (GREATER PART OF VOLTAGE DROP IS ACROSS THE RESISTANCE TO GROUND).

- THE MORE CONDUCTIVE THE MATERIAL, THE HIGHER THE PROBABILITY OF CREATING A SPARK AND THE HIGHER THE DISCHARGE CURRENT (HIGHER DISCHARGE CURRENTS CONDUCTED THROUGH AN ESD PART COULD INCREASE THE PROBABILITY OF PART FAILURE). THEREFORE THE TOTE BOX OR TABLE TOP SHOULD BE CONDUCTIVE ENOUGH NOT TO INDUCE SIGNIFICANT VOLTAGES ACROSS THE TOTE BOX OR TABLE TOP AND AT THE SAME TIME NOT TO BE SO CONDUCTIVE AS TO CREATE A HIGH CURRENT OR SPARK DISCHARGE.

- CONDUCTIVITY CAN BE A SAFETY HAZARD WHERE ELECTRICAL TEST EQUIPMENT IS USED, ELECTRONIC PARTS OR ASSEMBLIES ARE TESTED, OR WHERE THE CONDUCTIVE MATERIAL CAN FLAKE, SHRED OR OTHERWISE CAUSE CONDUCTIVE PARTICULATE. SUCH PARTICULATE CAN CAUSE SHUNT PATHS IN ELECTRONIC EQUIPMENT.

(4) FORMS AVAILABLE IN ESD PROTECTIVE MATERIALS

ESD PROTECTIVE MATERIALS WHETHER CONDUCTIVE, STATIC DISSIPATIVE OR ANTI-STATIC, ARE CAPABLE OF BEING FORMED INTO MANY SHAPES. FOR EXAMPLE, METALS CAN BE CAST, STAMPED OR PIECES WELDED INTO MOST ANY SHAPE WHILE MOST CONDUCTIVE, STATIC DISSIPATIVE AND ANTI-STATIC PLASTIC MATERIALS CAN BE MOLDED INTO FORMED SHAPES. FIBERBOARD, MELAMINE LAMINATES AND OTHER MATERIALS (LAMINATED OR HOMOGENEOUS) CAN BE CONSTRUCTED INTO BOXES AND VARIOUS OTHER SHAPES. MANY TYPES OF ESD PROTECTIVE MATERIALS ARE AVAILABLE IN DIFFERENT FORMED SHAPES OR PRODUCTS SUCH AS THE FOLLOWING:

(a) SHEETS AND PLATES - PROVIDED IN VARIOUS SIZES AND THICKNESSES FOR USE AS WORK BENCH TOPS, FLOORS, FLOOR MATS, WRAPS AND COVERINGS.

(b) FORMED SHAPES - AVAILABLE IN FORMED PARTS TRAYS, VIALS, CARRIERS, BOXES, BOTTLES AND OTHER CUSTOM SHAPES.

(c) RIGID SHORTING BARS AND CLIPS - USED FOR ELECTRICAL SHORTING OF ESDS LEADS OR CONNECTOR PINS OF ELECTRONIC AND ELECTRICAL PARTS AND HIGHER ASSEMBLIES.

(d) FOAM USED FOR SHORTING PART LEADS OR AS A CUSHIONING FOR PACKAGING.

(e) BUBBLE PACK MATERIAL OR OPEN CELL PLASTIC FOAM USED FOR CUSHIONING FOR PACKAGING (E.G., MIL-P-81997 AND PPP-C-1842 TYPE II STYLE A) (REFERENCES 21, 22).

(f) FLEXIBLE MATERIALS IN THE FORM OF BAGS (E.G., MIL-B-81847 AND MIL-B-82647) (REFERENCES 23 AND 24), TRASH CAN LINERS, SEAT COVERS, PERSONNEL APPAREL SUCH AS SMOCKS, GAUNTLETS, FINGER COTS, ETC.

(g) PERSONNEL GROUND STRAPS - INSULATED WIRE OR FLEXIBLE STRAPS OF THE CONDUCTIVE PLASTIC USED IN THE FORM OF PERSONNEL GROUND STRAP CABLES.

(h) HEEL GROUNDERS - FLEXIBLE FORMED STRIPS OF THE CONDUCTIVE PLASTICS PLACED INSIDE THE SHOE AND CONNECTED TO THE OUTSIDE SHOE HEEL, USED TO GROUND PERSONNEL TO THE BOTTOM OF THE SHOE HEEL (USED IN CONJUNCTION WITH CONDUCTIVE FLOORS AND FLOOR MATS).

(i) CONDUCTIVE SHOES - CONDUCTIVE RUBBER OR PLASTIC INNER AND OUTER SOLES AND HEELS.

(j) CONDUCTIVE, STATIC DISSIPATIVE AND ANTI-STATIC CARPETING AND FLOORING (INCLUDING CARBON IMPREGNATED VINYL TILES AND TERRAZZO FLOORS).

(5) APPLICATION INFORMATION OF ESD PROTECTIVE MATERIALS

GENERAL APPLICATION FOR THE THREE CLASSIFICATIONS OF ESD PROTECTIVE MATERIALS ARE PROVIDED IN TABLE VII-A. ADDITIONAL APPLICATION INFORMATION FOR VARIOUS FORMED SHAPES OF ESD PROTECTIVE MATERIALS IS PROVIDED IN TABLE VII-B. IT SHOULD BE NOTED THAT THE INFORMATION PROVIDED IN THESE TABLES IS RELATIVE FROM ONE MATERIAL TYPE TO ANOTHER. ALSO, IT SHOULD BE EMPHASIZED AGAIN THAT THERE ARE NO CLEAR DEMARCATIONS BETWEEN THE THREE TYPES OF MATERIALS LISTED (E.G., THE PROPERTIES OF A CONDUCTIVE MATERIAL AT THE HIGHER END OF ITS RESISTIVITY RANGE COULD BE EQUIVALENT IN PROPERTIES TO A STATIC DISSIPATIVE MATERIAL AT THE LOWER ENDS OF ITS RESISTIVITY RANGE).

C. ELEMENTS OF AN ESD PROTECTED AREA

THE INTENT OF THIS DISCUSSION IS TO PRESENT THE APPROACHES USED IN THE DESIGN AND CONSTRUCTION OF ESD PROTECTED AREAS. NOT ALL THE ELEMENTS DISCUSSED HERE ARE REQUIRED IN THE PROTECTED AREAS, BUT IT IS HOPED THIS DISCUSSION WILL PROVIDE AN INSIGHT TO THE ELEMENTS THAT ARE AVAILABLE.

(1) ESD PROTECTIVE FLOORS

TWO OF THE MOST SIGNIFICANT SOURCES INVOLVED IN STATIC VOLTAGE GENERATION ARE THE PERSON AND THE FLOOR. THE TYPE OF FLOOR, FLOOR POLISH, WAX, CLEANER, SEALER, AND THE HUMIDITY LEVEL DETERMINE THE ABILITY OF PERSONNEL AND ROLLING CARTS TO GENERATE DAMAGING STATIC POTENTIALS. A SHORT DISCUSSION OF TWO COMMERCIALLY AVAILABLE FLOORING MATERIALS AND CONSIDERATIONS FOR THLIR USE IN ESD PROTECTIVE AREAS ARE AS FOLLOWS:

(a) MONILE POLYACRYLATE THINSET CONDUCTIVE TERRAZZO

THIS MATERIAL (MARBLE CHIPS) IS 75% MARBLE, 25% CARBON

TABLE VII-A. General Application Information for Different Types of ESD Protective Formed Shapes

Application	Conductive	Static Dissipative	Anti-Static
General application considerations	1. Could present a personnel safety hazard when contacting high voltages and hard grounds. 2. Could damage electrical circuitry of parts or assemblies during testing if electrical connections contact conductive surfaces. 3. Steels (except corrosion resistant) are prone to corrosion. Protective coatings such as paint will destroy the surface conductive properties and could be static generative. 4. Aluminum will form aluminum oxide on its surface reducing conductivity and increasing its ability to generate static. 5. Hard surfaces such as metal provide little protection from physical shock to items dropped thereon	1. Presents the same hazards as listed under "Conductive" 1 and 2 except to a lesser degree. Hazards depend upon the magnitude of the voltages and the types of parts and circuits tested. 2. See item (6) under "Conductive". 3. See item (7) under "Conductive".	1. The effectiveness of hygroscopic antistatic materials are reduced in low relative humidities since their antistatic properties are dependent upon absorbing moisture from the air. 2. The accumulation of dirt, oils and silicone have an adverse effect on the anti-static properties of hygroscopic antistats. Cleaning with solvents such as alcohols, ketones and other hydrocarbon based solvents can remove the antistats. May require periodic treatment with a topical antistat. 3. Antistats used in some hygroscopic anti-static materials can track onto items and act as a foreign substance which could react with other materials

TABLE VII-A. General Application Information for Different Types of ESD Protective Formed Shapes (Cont'd)

Application	Conductive	Static Dissipative	Anti-Static
	6. Materials should be reviewed for flammability, corrosivity, toxicity, bacterial growth, crumbling, powdering, shedding, flaking, brittleness, outgassing, long term chemical reaction with parts. 7. Protection against triboelectric generation depends upon the material used.		3. (Cont'd). adversely. This has been shown to be a problem with the lubricant in miniature bearings. 4. See item (6) under "Conductive". 5. Hygroscopic antistatic materials generally provide protection against triboelectric generation. The triboelectric generation characteristics of other anti-static materials depends upon the material used.

TABLE VII-B. Additional Application Information for Different Types of ESD Protective Formed Shapes

Application	Conductive	Static Dissipative	Anti-Static
Bench tops (Also see 7.2.8)	1. Dissipates charges rapidly throughout the material and to ground, and will not maintain a high static voltage. 2. Could discharge an ESD in the form of a spark causing EMP. 3. Could cause a high current discharge through an ESDS part. 4. Could present a safety hazard or short if a high voltage source contacted the bench top. Could hard ground the table top if test equipment with grounded chassis contacted the bench top surface. 5. Safety could require that series resistances be provided in connection to ground where high voltages can be contacted by personnel.	1. Charge dissipation rate generally adequate for most ESDS parts. 2. Provides greater resistance for personnel protection from high voltages or hard grounding if the table top is contacted with test equipment ground. 3. Reduces discharge currents through ESDS parts. 4. Safety could require that series resistances be provided in connection to ground where high voltages can be contacted by personnel.	1. Provides slow bleed-off of static charges. If ground straps are used by personnel working at the work bench high ESD voltages should be rapidly dissipated through the ground strap. 2. Reduces the possibility of a spark from ESD. 3. Limits discharge currents through ESDS parts to low levels. 4. Generally provides adequate resistance for personnel safety.

TABLE VII-B. Additional Application Information for Different Types of ESD Protective Formed Shapes (Cont'd)

Application	Conductive	Static Dissipative	Anti-Static
Floor mats (should be used with conductive shoes or heel grounders).	1. Dissipates charges rapidly throughout the material and to ground, and will not maintain a high static voltage. 2. Safety could require that series resistances be provided in connection to ground where high voltages can be contacted by personnel.	1. Provides adequate conductivity for dissipation of charges. 2. Generally provides sufficient resistance for personnel safety. External series resistance to ground may not be required.	1. Provides slow bleed-off of high static charges. 2. Accumulations of dirt, contaminants and wear reduce anti-static properties. Requires frequent cleaning and treatment with a topical antistat.
Packaging Material (bags and other containers used to enclose ESDS items. Note: Combination of different ESD protective materials may be required to provide the best protection from triboelectric generation, direct discharge and electrostatic fields. Multilayered packaging containers using different types of ESD protective materials as intimate and outside wraps are available.	1. Provides protection of highly sensitive ESDS items from high ESD voltages. 2. Provides protection of ESDS items from electrostatic fields. 3. Thin metallized coatings on some containers can be abraded reducing shielding effectiveness from electrostatic fields.	1. Provides protection of moderately sensitive ESDS items from high ESD voltages. 2. Provides protection of highly sensitive ESDS items from moderate voltages. 3. Provides moderate protection of ESDS items from electrostatic fields.	1. Provides protection of moderately sensitive ESDS items from moderate ESD voltages, highly sensitive items from low voltages.

TABLE VII-B. Additional Application Information for Different Types of ESD Protective Formed Shapes (Cont'd)

Application	Conductive	Static Dissipative	Anti-Static
Tote boxes and parts trays	1. Same as for packaging material except that openings in box or tray could reduce protection from electrostatic fields.	1. Same as for packaging material except that openings in box or tray could reduce protection from electrostatic fields.	1. Same as for packaging material except that openings in box or tray could reduce protection from electrostatic fields.
Shunt bars, clips, foam.	1. Provides low impedance shunt and good protection for ESDS parts.	1. Provides relatively high impedance shunt which could be suitable for ESDS parts with impedances considerably higher than the shunt impedance.	1. Typically is too high in resistance to act as a good shunt.
Personnel Apparel (smocks, gauntlets, finger cots, etc.).	1. Provides good dissipation over its surface and will conduct charges from a person's body to ground if a ground strap is worn.	1. Provides good dissipation over its surface and will conduct charges from a person's body to ground if a ground strap is worn.	1. Provides slow bleed-off of charges from person's body to ground when a strap is worn.

BLACK, AND HAS 25 KΩ TO 1MΩ SURFACE RESISTIVITY PER SQUARE. THIS FLOORING IS COMMONLY USED BY MANY HOSPITALS TO CONTROL STATIC POTENTIALS. ONE ADVANTAGE OF THIS KIND OF FLOOR IS THAT IT WOULD NEVER WEAR OUT, BUT THE CONDUCTIVITY HAS BEEN KNOWN TO DROP SLIGHTLY AFTER A FEW YEARS OF USE.

(b) CONDUCTIVE VINYL FLOORING

THIS MATERIAL HAS A SURFACE RESISTIVITY OF 25 KΩ TO 1 MΩ PER SQUARE. THIS FLOORING IS RESILIENT AND COMFORTABLE TO WALK ON. IT IS SOLVENT, WEAR, HEAT AND SOLDER RESISTANT. CONDUCTIVE ADHESIVE SHOULD BE USED IN INSTALLING CONDUCTIVE VINYL FLOORING.

THE PRINCIPLE BENEFITS OF UTILIZING THE PERMANENT TYPE OF ESD PROTECTIVE FLOORING ARE:

- HIGH RELATIVE HUMIDITY IS NOT NECESSARY. TYPICALLY USED VALUE OF RH IS 25%.
- ELIMINATION OF REPLACEMENT COSTS FOR CONDUCTIVE FLOOR MATS.
- GOOD CONTROL OF STATIC CHARGE BUILDUP FROM PEOPLE WALKING ACROSS THE FLOOR.
- PROTECTION OF ESDS DIGITAL EQUIPMENT FROM TRANSIENT UPSET.

(c) HARD SURFACED FLOORING SHOULD NEVER BE WAXED UNLESS A CONDUCTIVE WAX IS USED SINCE SURFACES WAXED WITH TYPICAL INSULATIVE WAXES CAN CREATE SUBSTANTIAL ELECTROSTATIC CHARGES AND CAN INSULATE THE SURFACE OF CONDUCTIVE FLOORS.

(d) CONCRETE FLOORS WITH SEALERS AND FINISHED WOOD FLOORS ARE TYPICAL PRIME GENERATORS OF STATIC ELECTRICITY. OFTEN THEY CAN BE RENDERED ANTI-STATIC BY THE USE OF TOPICAL ANTISTATS.

(e) ANTI-STATIC CARPETS ARE AVAILABLE, SOME OF WHICH ARE PERMANENTLY ANTI-STATIC (E.G., CONTAINER CARBON FILAMENT OR CONDUCTIVE WIRES). TYPICALLY, ANTI-STATIC CARPETS WILL NOT REDUCE GENERATED VOLTAGE LEVELS BELOW 2000 VOLTS UNDER WORST CASE CONDITIONS OF HUMIDITY.

(2) CONDUCTIVE SHOES

THE USE OF CONDUCTIVE FLOORS AND MATS IN DISSIPATING CHARGES HAS SEVERAL SHORTCOMINGS. THE ABILITY OF THE MAT TO DEPLETE CHARGES ON A PERSON IS DEPENDENT UPON THE COMPOSITION OF A PERSON'S SHOE SOLES AND, TO A DEGREE, THE CLEANLINESS OF THE SOLE SURFACE. SHOES WHICH HAVE A WAX BUILDUP DUE TO WALKING OVER WAXED FLOORS CAN LOSE THEIR CONDUCTIVITY. THEREFORE, CONDUCTIVE FLOORS AND MATS WILL ONLY BE EFFECTIVE WHEN THE PROPER FOOTWEAR (I.E., CONDUCTIVE OR LEATHER-SOLED SHOES) HEEL GROUNDERS ARE WORN.

CERTAIN TYPES OF SHOE SOLES SUCH AS CREPE OR HEAVY RUBBER CAN PREVENT THE DISCHARGE OF A PERSON STANDING ON ANY KIND OF FLOOR, CONDUCTIVE OR INSULATIVE. A PERSON WITH CREPE OR HEAVY RUBBER SOLED SHOES IS A WALKING STATIC GENERATOR WITH THE LEVEL OF VOLTAGE GENERATED DEPENDENT UPON THE FLOOR MATERIAL. A CHARGED PERSON IS ALSO THE SOURCE OF ELECTROSTATIC FIELD(S). ANY ESDS PART OR ASSEMBLY CAUGHT IN THAT ELECTRIC FIELD OR IN THE DISCHARGE PATH TO GROUND IS SUBJECT TO POSSIBLE ESD DAMAGE.

IT IS UNREALISTIC TO TELL PEOPLE WHAT KIND OF SHOES THEY CAN WEAR TO WORK, AND EVEN IF THEY WERE SO INSTRUCTED, IT WOULD BE ALMOST IMPOSSIBLE TO ENFORCE. THEREFORE IT IS BENEFICIAL TO SUPPLY PERSONNEL WITH CONDUCTIVE SHOES THAT ARE ONLY WORN IN THE ESD PROTECTED AREAS. AN ALTERNATE SOLUTION TO THIS PROBLEM IS TO REQUIRE THE USE OF CONDUCTIVE HEEL GROUNDERS, OR BOOTIES WHERE ESDS PARTS ARE HANDLED AND CONDUCTIVE FLOORING OR MATS ARE USED. TABLE VII-C SHOWS EFFECTIVE SHOE RESISTANCE FOR VARIOUS SHOE TYPES.

TABLE VII-C (REFERENCE 24A)
EFFECTIVE SHOE RESISTANCE

SHOE TYPE	EFFECTIVE RESISTANCE THROUGH ONE SHOE TO GROUND
LEATHER SOLES	10 TO 100 MEG OHMS
COMPOSITION SOLES	175 TO 750 MEG OHMS
CREPE AND THICK RUBBER SOLES	1,000 TO 500,000 MEG OHMS

(3) ESD PROTECTIVE WORK AREAS

THE SURFACE OF THE WORK STATION CAN BE MADE OF, OR COVERED WITH, ESD PROTECTIVE MATERIALS SUCH AS METAL, MIL-B-81705 TYPE II, MIL-P-82646 (REFERENCES 17, 16), MELAMINE LAMINATES OR OTHER ESD PROTECTIVE MATERIALS. THE PROPERTIES OF THE DIFFERENT ESD PROTECTIVE MATERIALS SHOULD BE CAREFULLY CONSIDERED IN THEIR SELECTION FOR A BENCH TOP, ESPECIALLY REGARDING THE SAFETY ASPECTS. FOR EXAMPLE, HIGHLY CONDUCTIVE MATERIAL CAN PRESENT SAFETY HAZARDS WHERE HIGH VOLTAGE SOURCES ARE NEARBY, ESPECIALLY IF GROUNDED TEST EQUIPMENT IS PLACED ON THE TABLE TOP. HIGHLY CONDUCTIVE WORK BENCH SURFACES (I.E., METAL) WILL DISCHARGE ELECTROSTATIC CHARGES VERY QUICKLY, CREATING HIGH DISCHARGE CURRENTS. STATIC DISSIPATIVE MATERIALS PROVIDE SLOWER BLEED-OFF OF ELECTROSTATIC CHARGES REDUCING DISCHARGE CURRENT LEVELS WHILE PROVIDING REASONABLY ADEQUATE DISSIPATION TIMES. ANTI-STATIC MATERIALS BLEED-OFF THE CHARGES EVEN MORE SLOWLY LIMITING INSTANTANEOUS DISCHARGE CURRENTS AND REDUCING THE POSSIBILITY OF DAMAGE TO ESDS ITEMS DUE TO HIGH CURRENT FLOWS OR EMI FROM SPARKING. IN AREAS WHERE PERSONNEL ARE EQUIPPED WITH GROUND STRAPS, ANTI-STATIC MATERIALS PROVIDE DISTINCT ADVANTAGES FOR TABLE TOPS. ESD PROTECTIVE WORK SURFACES ARE NORMALLY GROUNDED TO INCREASE

THE DISSIPATION OF STATIC CHARGES AND TO AVOID FLOATING GROUND VOLTAGE LEVELS.

(4) CONDUCTIVE CHAIRS/STOOLS

AN UNGROUNDED OPERATOR (I.E., ONE WITH NO PERSONNEL GROUND STRAP) SITTING ON A STOOL MADE OF INSULATIVE MATERIAL IS EFFECTIVELY INSULATED FROM ALL SURROUNDINGS. ANY CHARGES WHICH MIGHT BUILD UP ON THE INDIVIDUAL WILL REMAIN SINCE THERE IS NO CONDUCTIVE PATH TO ALLOW FOR THE DEPLETION OF THOSE CHARGES. FOR THIS REASON METAL CHAIRS AND STOOLS, WITH SEATS OF ESD PROTECTIVE MATERIAL, ARE OFTEN USED IN THE ESD PROTECTIVE AREA. THIS IS ESPECIALLY IMPORTANT IF A FLOOR PERSONNEL GROUNDING SYSTEM IS USED IN PLACE OF PERSONNEL GROUND STRAPS WHEN PERSONNEL LIFT THEIR FEET OFF THE CONDUCTIVE FLOOR. EXISTING INSULATIVE CHAIRS AND STOOLS CAN BE COVERED WITH ESD PROTECTIVE MATERIALS TO REDUCE STATIC GENERATION.

(5) PERSONNEL GROUND STRAPS

PERSONNEL HANDLING ESDS ITEMS ARE USUALLY EQUIPPED WITH A SKIN-CONTACT WRIST, LEG OR ANKLE BRACELET AND STRAP MADE OF A CONDUCTIVE CABLE CONNECTED TO THE WORK STATION COMMON GROUND THROUGH A SERIES RESISTANCE. THE USE OF SUCH STRAPS ARE THE MOST ECONOMICAL AND EFFECTIVE METHOD OF DEPLETING THE CHARGES WHICH MIGHT ACCUMULATE ON THE OPERATOR REGARDLESS OF THE TYPE OF FOOTWEAR WORN. THE SERIES RESISTANCE (TYPICALLY 1/4 TO 1 MEGOHM) IS PROVIDED TO PROTECT THE OPERATOR FROM POSSIBLE SHOCK HAZARDS. PERSONNEL GROUND STRAPS SHOULD HAVE QUICK RELEASE MECHANISMS AT BOTH ENDS OF THE CABLE FOR PERSONNEL SAFETY. THEY SHOULD ALSO BE MADE OF A MATERIAL WHICH IS LIGHT ENOUGH AND FLEXIBLE ENOUGH SO AS NOT TO IMPEDE THE EFFICIENCY OF THE OPERATOR.

(6) PERSONNEL CLOTHING

PERSONNEL HANDLING ESDS ITEMS SHOULD WEAR LONG SLEEVED ESD PROTECTIVE SMOCKS OR CLOSE-FITTING, SHORT SLEEVED SHIRTS OR BLOUSES. LONG SLEEVED SHIRTS OR BLOUSES SHOULD BE ROLLED UP OR COVERED WITH ESD PROTECTIVE GAUNTLETS BANDED TO THE BARE WRIST AND EXTENDING TOWARD THE ELBOW. SOME WORKING SITUATIONS COULD REQUIRE ADDITIONAL ESD PROTECTION, SUCH AS ESD PROTECTIVE APRONS. GLOVES AND FINGER COTS WHERE USED SHOULD ALSO BE MADE OF ESD PROTECTIVE MATERIALS. HYGROSCOPIC ANTI-STATIC PERSONNEL APPAREL SHOULD BE USED WITH CAUTION WHERE RELATIVE HUMIDITY LEVELS ARE EXTREMELY LOW. SMOCKS, GLOVES OR FINGER COTS OF COMMON PLASTIC, RUBBER OR NYLON SHOULD NOT BE WORN IN AN ESD PROTECTED AREA. ESD PROTECTIVELY TREATED APPAREL SHOULD BE FREQUENTLY CHECKED, ESPECIALLY AFTER CLEANING, BY SCANNING PERSONNEL WITH AN ELECTROSTATIC FIELD METER TO ASSURE THAT DAMAGING ESD VOLTAGES CANNOT BE GENERATED.

(7) WORK STATION COMMON GROUND

ONE OF THE MOST COMMON METHODS FOR ELIMINATING SOURCES OF ELECTROSTATIC CHARGES AND EQUALIZING STATIC POTENTIALS IN A WORK AREA INVOLVES MAINTAINING EVERYTHING IN THE AREA AT THE SAME POTENTIAL. THIS CAN BE ACCOMPLISHED BY HAVING ALL ITEMS IN THE AREA ELECTRICALLY CONNECTED TO A COMMON GROUNDED POINT AND THAT GROUNDED POINT CONNECTED TO HARD (E.G., EARTH OR HULL) GROUND THROUGH A CURRENT LIMITING RESISTOR.

(8) CONTROLLED RELATIVE HUMIDITY

THE MAGNITUDE OF STATIC POTENTIAL WHICH DEVELOPS ON A BODY DEPENDS UPON THE RATE OF CHARGE GENERATION, THE CAPACITANCE OF THE BODY HOLDING THE CHARGE AND THE CHARGE LEAKAGE RATE TO GROUND. ONE TECHNIQUE USED FOR REDUCING OR MINIMIZING THE MAGNITUDE OF STATIC POTENTIALS

INVOLVES MAXIMIZING THE LEAKAGE RATE BY INCREASING RELATIVE HUMIDITY WHICH IN TURN INCREASES THE CONDUCTIVITY OF SURROUNDING MATERIALS, ESPECIALLY IF THEY ARE HYGROSCOPIC.

HIGH RELATIVE HUMIDITY CONDITIONS (E.G., ABOVE 60%) CAN, HOWEVER, INTRODUCE OTHER UNDESIRABLE EFFECTS SUCH AS CORROSION, CONTAMINATION OR POSSIBLE LEAKAGE PATHS IN PARTS OR IN EQUIPMENT. IT SHOULD BE RECOGNIZED THAT CONTROLLING THE RELATIVE HUMIDITY DOES NOT COMPLETELY ELIMINATE STATIC CHARGE BUILDUP; IT MERELY REDUCES THE MAGNITUDES OF STATIC POTENTIALS BY PROVIDING CHARGE BLEED-OFF TO GROUND. ELECTROSTATIC DISCHARGES WILL OCCUR IN ENVIRONMENTS OF HIGH RELATIVE HUMIDITY SUCH AS LIGHTNING DURING A THUNDER STORM. THE "OPTIMAL" RELATIVE HUMIDITY RANGE IS APPROXIMATELY 40% TO 60%.

CONTROLLING THE RELATIVE HUMIDITY IN EXTREMELY LARGE WORK AREAS IS OFTEN EXPENSIVE AND IMPRACTICAL. THEREFORE, THIS TECHNIQUE IS NORMALLY ONLY EMPLOYED IN SMALL TO MEDIUM SIZED, CONFINED WORK AREAS.

(9) GROUNDED SOLDERING IRONS

THE TIP OF A SOLDERING IRON REPRESENTS A POTENTIAL STATIC HAZARD IN THE WORK AREA. EVEN THOUGH THE IRON MIGHT INCORPORATE A THIRD GROUND WIRE, IT IS POSSIBLE THAT THE TIP IS ELECTRICALLY ISOLATED FROM THE GROUND. THIS WOULD ALLOW STATIC CHARGES TO ACCUMULATE ON THE TIP OF THE IRON BY THERMAL EMISSION THAT CAN DESTROY ESDS ITEMS. CARE SHOULD BE TAKEN TO ASSURE THAT THE TIPS OF THE SOLDERING IRONS ARE ELECTRICALLY GROUNDED. IF THE TIPS ARE ELECTRICALLY ISOLATED A GROUNDING PROCEDURE SUCH AS PERIODICALLY TOUCHING THE SOLDERING TIP TO A METAL GROUND POINT COULD BE IMPLEMENTED.

(10) ANTISTAT (TOPICAL ANTISTAT) LIQUID TREATMENT

TOPICAL ANTISTATS ARE CHEMICAL AGENTS WHICH WHEN APPLIED TO SURFACES OF INSULATIVE MATERIALS WILL REDUCE THEIR ABILITY TO GENERATE

STATIC. TOPICAL ANTISTATS ARE GENERALLY LIQUIDS CONSISTING OF A CARRIER AND AN ANTISTAT. THE CARRIER IS THE VEHICLE USED TO TRANSPORT THE ANTISTAT TO A MATERIAL. IT ACTS AS A SOLVENT AND CAN BE WATER, ALCOHOL OR MINERAL SPIRITS. THE ANTISTAT IS THE MATERIAL THAT REMAINS DEPOSITED ON THE MATERIAL SURFACE AFTER THE CARRIER EVAPORATES, AND PROVIDES THE STATIC CONTROL FUNCTION. SOME TOPICAL ANTISTATS ARE DETERGENT TYPE MATERIALS WHICH COMBINE WITH THE MOISTURE IN THE AIR TO WET THE SURFACE OF THE MATERIAL ON WHICH THEY ARE DEPOSITED. THESE ANTISTATS CAN BE CLASSIFIED AS HYBROSCOPIC AND THEIR EFFECTIVENESS IS REDUCED UNDER LOW RELATIVE HUMIDITY AS WITH THE MIL-B-81705 TYPE II (REFERENCE 17) MATERIALS. OTHER ANTISTATS ARE AVAILABLE WHICH ARE NOT HUMIDITY DEPENDENT. THEY REDUCE THE GENERATION OF STATIC BY INCREASING SURFACE LUBRICITY AND SURFACE CONDUCTIVITY. DILUTED SOLUTIONS CAN PROVIDE RESISTIVITIES OF 10^{12} OHMS/SQUARE. MORE CONCENTRATED SOLUTIONS OF THIS TYPE OF ANTISTAT CAN REDUCE RESISTIVITY OF SOME INSULATIVE MATERIALS AS LOW AS 10^{6} OHMS/SQUARE. THE PRIMARY EFFECT OF TOPICAL ANTISTATS IS TO REDUCE THE STATIC GENERATED BY TRIBOELECTRIC EFFECT AND PROVIDE SOME BLEED-OFF CAPABILITY. TOPICAL ANTISTATS CAN BE BRUSHED, SPRAYED, ROLLED, DIPPED, MOPPED, WIPED OR OTHERWISE APPLIED TO FLOORS, CARPETS, WORK BENCH TOPS, PARTS BINS, CHAIRS, WALLS, CEILINGS, TOOLS, PAPER, PLASTICS AND CLOTHING TO RENDER THEM ESD PROTECTIVE. SOME ANTISTATS ARE ALSO GOOD CLEANERS AND CAN BE MIXED WITH WATER TO CLEAN SURFACES (FLOORS, BENCH TOPS) WHILE AT THE SAME TIME RENDERING THEM ANTI-STATIC. VINYLS AND MYLAR DO NOT EASILY ACCEPT AND BIND SOME TOPICAL ANTISTATS AND THEREFORE CAN BE DIFFICULT TO RENDER ANTI-STATIC USING MOST TOPICAL ANTISTATS.

TOPICAL ANTISTATS WILL PROVIDE PROTECTION FOR WEEKS OR YEARS DEPENDING UPON THE USE OR WEAR ON THE SURFACE. THEREFORE THEY SHOULD BE CHECKED PERIODICALLY BY RUBBING THE TREATED SURFACE WITH A PLAIN PIECE OF POLYETHYLENE AND MONITORING THE CHARGE WITH AN ELECTROSTATIC FIELD METER.

(a) FACTORS IN SELECTION OF ANTISTATS

CHARACTERISTICS TO BE CONSIDERED IN SELECTING AN ANTISTAT IN ADDITION TO ITS ANTI-STATIC PROPERTIES INCLUDE:

- INHIBITS BACTERIAL GROWTH
- NON-TOXICITY
- NON-CORROSIVITY
- NON-FLAMMABILITY
- NON-IRRITATING TO PERSONNEL

(b) CAUTIONS IN THE USE OF TOPICAL ANTISTATS

- TOPICAL ANTISTATS INCREASE CONDUCTIVITY AND THEREFORE SHOULD NOT BE APPLIED TO PRINTED CIRCUIT BOARDS, ELECTRICAL PARTS OR ELECTRICAL ASSEMBLIES; HIGH RESISTANCE LEAKAGE PATHS COULD RESULT, CAUSING POSSIBLE CIRCUIT MALFUNCTION.

- TOPICAL ANTISTAT RESIDUE ON A PERSON'S HANDS CAN CONTAMINATE PRINTED CIRCUIT BOARDS AND ELECTRICAL ASSEMBLIES. PERSONS THAT APPLY TOPICAL ANTISTATS SHOULD WASH THEIR HANDS THOROUGHLY WITH SOAP BEFORE HANDLING PRINTED CIRCUIT BOARDS, PARTS OR ELECTRICAL ASSEMBLIES.

- TOPICAL ANTISTATS CAN BE REMOVED ACCIDENTLY OR ON PURPOSE WITH CHEMICALS SUCH AS ALCOHOL, DETERGENTS, FLUX, TRICHLOROETHANE, SOAP AND WATER, AND REPEATED CLEANING WITH JUST PLAIN WATER. A PRE-TREATED WORK SURFACE EXPOSED TO ANY OF THESE TYPICAL CLEANING AGENTS SHOULD BE RE-TREATED WITH TOPICAL ANTISTATS IF ESD PROTECTION IS TO BE MAINTAINED.

(11) ESD PROTECTIVE CARRIERS USED IN ESD PROTECTED AREAS

(a) BAGS, TRAYS AND OTHER CONTAINERS

BAGS, TRAYS, TOTE BOXES, CONTAINERS, PARTS BINS, PARTS CARRIERS, SHORTING BARS, AND VARIOUS OTHER STANDARD FORMED SHAPES

MADE FROM ESD PROTECTIVE MATERIALS ARE COMMERCIALLY AVAILABLE. ALSO MANY MANUFACTURERS OF THESE MATERIALS WILL SUPPLY CUSTOM SHAPED CONTAINERS. THE MORE COMMON ESD PROTECTIVE MATERIALS USED IN THE CONSTRUCTION OF FORMED SHAPES ARE THE MIL-B-81705 TYPE II ANTISTATIC POLYETHYLENE, MIL-P-82646 CONDUCTIVE CARBON IMPREGNATED POLYOLEFIN AND COMMON METALS SUCH AS ALUMINUM.

OTHER ESD PROTECTIVE CONTAINERS INCORPORATE CARBON COATED, ALUMINUM COATED, NICKEL COATED PLASTIC AND PAPER BASED MATERIALS AND OTHER LAMINATES WHICH PROVIDE INTERNAL PROTECTION FROM TRIBOELECTRIC GENERATION (I.E., ANTISTATIC INSIDE) WITH METAL SHIELDING ON THE EXTERIOR (E.G., NICKEL, ALUMINUM FOIL).

TRAYS AND CONTAINERS MADE OF NON-ESD PROTECTIVE MATERIALS CAN BE RENDERED ANTI-STATIC, STATIC DISSIPATIVE OR CONDUCTIVE WITH THE USE OF TOPICAL ANTISTATS AND METALLIZED COATINGS. CERTAIN FABRIC SOFTENERS HAVE ALSO BEEN FOUND TO BE EFFECTIVE ANTISTATS FOR A LIMITED TIME AND CAN BE USED TO RENDER CLOTHING AND OTHER OBJECTS (E.G., TABLE TOPS) ANTI-STATIC. ANTI-STATIC COATINGS SHOULD BE CHECKED BEFORE USING FOR THEIR POSSIBLE INCORPORATION OF SUBSTANCES SUCH AS SILICONE OR SODIUM WHICH CAN HAVE DETRIMENTAL EFFECTS ON ELECTRICAL CIRCUITRY. THERE ARE SEVERAL TYPES OF COATINGS OR SPRAYS, FOR THE VARYING REQUIREMENTS OF DIP TUBES, BLISTER PACKS, TOTE BOXES, CLOTHING, RUBBER, GLASS AND MISCELLANEOUS ORGANIC MATERIALS. THE PROPERTIES OF ANTI-STATICALLY TREATED MATERIALS SHOULD BE PERIODICALLY MONITORED.

CONDUCTIVE PAINTS AND COATINGS WITH CONDUCTIVITIES RANGING FROM LESS THAN 1Ω/SQ. TO LESS THAN 1000 Ω/SQ. ARE AVAILABLE FOR ESD PROTECTION. THE LOWER RANGES ARE ALSO VERY USEFUL FOR EMI/RFI SHIELDING. ONLY CONDUCTIVE CONTAINERS ARE RECOMMENDED FOR STORING ESDS ITEMS. SUCH CONTAINERS SHOULD BE SUBJECTED TO A "TOUCH GROUND" PROCEDURE PRIOR TO REMOVAL OF THE ESDS ITEM TO DISCHARGE ANY CHARGES ON THE CONTAINER.

(b) SHUNTING BARS, CLIPS AND FOAM

THE TERMINALS OF ESDS ITEMS AT A WORK STATION SHOULD BE SHORTED TOGETHER USING METAL SHUNTING BARS, METAL CLIPS OR NON-CORROSIVE CONDUCTIVE FOAMS WHEN NOT BEING USED. (THE RESISTANCE OF THE SHUNTING DEVICE SHOULD BE ORDERS OF MAGNITUDE BELOW THE MINIMUM IMPEDANCE BETWEEN ANY TWO PINS OF THE ESDS PART). HOWEVER, SHUNT BARS, CLIPS AND CONDUCTIVE FOAM WILL NOT ALWAYS PROTECT AN ESDS ITEM FROM AN ESD AND SHOULD NOT BE USED AS PROTECTIVE COVERING FOR TRANSPORTATION OF ESDS ITEMS OUTSIDE AN ESD PROTECTED AREA. ESDS PARTS WITH NON-CONDUCTIVE CASES, OR ASSEMBLIES SUBJECTED TO ELECTROSTATIC FIELDS OR DIRECT DISCHARGES FROM AN ESD COULD INDUCE CURRENTS TO FLOW WITHIN THE ESDS ITEM TO THE SHUNT, SOMETIMES DAMAGING THAT ESDS ITEM. FOR PARTS WITH METAL CASES THE SHUNTING DEVICE SHOULD ALSO CONTACT THE ESDS ITEM CASE. FOR PARTS WITH NON-CONDUCTIVE CASES AND FOR ESDS ASSEMBLIES THE SHUNTING MATERIAL SHOULD ENCIRCLE THE ESDS ITEM.

(12) GROUNDING CONSIDERATIONS IN ESD PROTECTED AREAS

(a) GENERAL

THE SAFETY REQUIREMENTS OF MIL-STD-454, REQUIREMENT NO. 1 (REFERENCE 25) SHOULD BE CONSIDERED IN THE CONSTRUCTION OF ESD PROTECTED AREAS AND ESD GROUNDED WORK STATIONS TO REDUCE THE CHANCE OF ELECTRICAL SHOCK TO PERSONNEL.

CURRENT RATHER THAN VOLTAGE IS THE MOST IMPORTANT VARIABLE IN ESTABLISHING THE CRITERION FOR SHOCK INTENSITY. THREE FACTORS THAT DETERMINE THE SEVERITY OF ELECTRICAL SHOCK ARE: (1) QUANTITY OF CURRENT FLOWING THROUGH THE BODY; (2) PATH OF CURRENT THROUGH THE BODY; AND (3) DURATION OF TIME THAT THE CURRENT FLOWS THROUGH THE BODY. THE VOLTAGE NECESSARY TO PRODUCE THE FATAL CURRENT IS DEPENDENT UPON THE RESISTANCE OF

THE BODY, CONTACT CONDITIONS, AND THE PATH THROUGH THE BODY. SEE TABLE VII-D.

TABLE VII-D

EFFECTS OF ELECTRICAL CURRENT ON HUMANS

CURRENT VALUES (MILLIAMPERES)		EFFECTS
AC 60 Hz	DC	
0-1	0-4	PERCEPTION
1-4	4-15	SURPRISE
4-21	15-80	REFLEX ACTION
21-40	80-160	MUSCULAR INHIBITION
40-100	160-300	RESPIRATORY BLOCK
Over 100	Over 300	USUALLY FATAL

SUFFICIENT CURRENT PASSING THROUGH ANY PART OF THE BODY WILL CAUSE SEVERE BURNS AND HEMORRHAGES. HOWEVER, RELATIVELY SMALL CURRENTS CAN BE LETHAL IF THE PATH INCLUDES A VITAL PART OF THE BODY, SUCH AS THE HEART OR LUNGS. ELECTRICAL BURNS ARE USUALLY OF TWO TYPES, THOSE PRODUCED BY HEAT OF THE ARC WHICH OCCURS WHEN THE BODY TOUCHES A HIGH-VOLTAGE CIRCUIT, AND THOSE CAUSED BY PASSAGE OF ELECTRICAL CURRENT THROUGH THE SKIN AND TISSUE. CURRENTS OF 4 TO 21 MILLIAMPS CAN CAUSE REFLEX ACTION. ALTHOUGH NOT ELECTRICALLY DANGEROUS THIS COULD RESULT IN OTHER SAFETY HAZARDS TO PERSONNEL OR EQUIPMENT. THERE ARE VARIOUS METHODS OF INCORPORATING ADEQUATE SAFEGUARDS FOR PERSONNEL, MANY OF THESE METHODS BEING IMPLICIT IN ROUTINE DESIGN PROCEDURES.

(b) GROUND POTENTIAL OF ELECTRICAL/ELECTRONIC EQUIPMENT AND TOOLS

THE DESIGN AND CONSTRUCTION OF THE ESD PROTECTED AREA AND ESD GROUNDED WORK STATIONS COULD ENSURE THAT ALL EXTERNAL PARTS, SURFACES AND SHIELDS OF ELECTRONIC TEST EQUIPMENT AND POWER TOOLS ARE AT

A COMMON GROUND POTENTIAL AT ALL TIMES DURING NORMAL OPERATION. THE DESIGN SHOULD INCLUDE CONSIDERATION OF GROUND FAULTS AND VOLTAGE LIMITS ESTABLISHED ON A BASIS OF HAZARDOUS LOCATION. ANY EXTERNAL OR INTERCONNECTING CABLE, WHERE A GROUND IS PART OF THE CIRCUIT, SHALL CARRY A GROUND WIRE IN THE CABLE TERMINATED AT BOTH ENDS IN THE SAME MANNER AS THE OTHER CONDUCTORS. IN NO CASE, EXCEPT WITH COAXIAL CABLES, SHOULD THE SHIELD BE DEPENDED UPON FOR A CURRENT-CARRYING GROUND CONNECTION. PLUGS AND CONVENIENCE OUTLETS FOR USE WITH METAL CASED PORTABLE TOOLS AND EQUIPMENT SHOULD HAVE PROVISIONS FOR AUTOMATICALLY GROUNDING THE METAL FRAME OR CASE OF TOOLS AND EQUIPMENT WHEN THE PLUG IS MATED WITH THE RECEPTACLE, AND THE GROUNDING PIN SHALL MAKE FIRST, BREAK LAST. CAUTIONS MUST BE REQUIRED IN LOCATING SUCH TOOLS AND TEST EQUIPMENT ON ESD GROUNDED WORK BENCHES WITH METAL OR OTHER CONDUCTIVE COVERINGS SINCE THE HARD CASE GROUND OF THE TOOL AND TEST EQUIPMENT CAN SHUNT THE PROTECTIVE RESISTANCE IN THE WORK BENCH GROUND CABLE. AS AN ADDED PRE-CAUTION FOR PERSONNEL SAFETY GROUND FAULT INTERRUPTERS SHOULD BE USED WITH TEST EQUIPMENT. THE GROUND FAULT INTERRUPTER SENSES LEAKAGE CURRENT FROM FAULTY TEST EQUIPMENT AND INTERRUPTS THE CIRCUIT ALMOST INSTANTANEOUSLY WHEN THESE CURRENTS REACH A POTENTIALLY HAZARDOUS LEVEL. CAUTION MUST BE OBSERVED IN EMPLOYING PARALLEL PATHS TO GROUND (E.G., WRIST STRAPS, TABLE TOPS, FLOOR MATS, ETC.) THAT COULD REDUCE EQUIVALENT RESISTANCE OF PERSONNEL TO GROUND TO UNSAFE LEVELS.

(c) GROUND POTENTIAL OF ESD GROUNDED WORK BENCHES

ESD GROUNDED WORK BENCHES SHOULD BE SOFT GROUNDED TO ELIMINATE THE SAFETY HAZARD OF TOUCHING A HIGH VOLTAGE CIRCUIT WITH ONE HAND AND A HARD GROUND WITH THE OTHER. A SOFT GROUND SHOULD INCORPORATE APPROP-RIATE RESISTANCE TO LIMIT CURRENTS FROM ACCESSIBLE VOLTAGE SOURCES TO 5 MILLIAMPERES.

(d) GROUNDING MATERIALS

RESISTANCES BETWEEN THE WORK BENCH AND HARD GROUND SHOULD BE LOCATED AT THE POINT OF CONNECTION TO THE WORK BENCH TO REDUCE THE POSSIBILITY OF THE RESISTANCE BEING SHUNTED. WORK BENCH ESD PROTECTIVE MATERIALS AND GROUND CABLES SHOULD BE INSTALLED AS FOLLOWS:

- ATTACH THE ESD PROTECTIVE MATERIAL TO THE WORK BENCH SURFACE WITH STAINLESS STEEL SCREWS USING APPROXIMATELY ONE-INCH DIAMETER STAINLESS STEEL FLAT WASHERS UNDER THE SCREW HEADS. ALTERNATELY, DOUBLE-FACED CARPET TAPE CAN BE USED INSTALLING ONE STAINLESS STEEL SCREW WITH A STAINLESS STEEL WASHER UNDER THE SCREW HEAD FOR CONNECTING GROUNDING CABLES (PERSONNEL GROUND STRAP AND TABLE TOP GROUNDING CABLE).

- CONNECT ONE TERMINAL OF THE RESISTIVE GROUND CABLE BETWEEN THE SCREW HEAD AND THE METAL WASHER. CONNECT THE TERMINAL ON THE OTHER END OF THE GROUND CABLE TO THE GROUNDED WORK BENCH FRAME. IF THE WORK BENCH FRAME IS NOT GROUNDED CONNECT THE CABLE TO AN EARTH, POWER OR SHIP HULL GROUND. RESISTANCE OF THE GROUND CABLE SHOULD BE SUFFICIENT TO LIMIT LEAKAGE CURRENT TO 5 mA MAXIMUM.

(e) GROUNDING SAFETY CONSIDERATIONS

- CABLES AND RESISTORS SHOULD HAVE AMPLE CURRENT CARRYING CAPACITY. SINCE THE WORK BENCH GROUND IS FOR BLEEDING OFF ELECTRO-STATIC CHARGES A ONE-WATT RESISTOR SHOULD BE SUFFICIENT.

- THE GROUND CABLE CONNECTIONS SHOULD BE CONTINUOUS AND PERMANENT.

- RESISTANCE(S) TO GROUND SHOULD BE HIGH ENOUGH CONSIDERING ALL PARALLEL PATHS TO LIMIT LEAKAGE CURRENT TO PERSONNEL TO THE 5 MILLIAMPERES MAXIMUM LEVEL BASED UPON THE HIGHEST VOLTAGE SOURCE

ACCESSIBLE BY GROUNDED PERSONNEL.

• THE GROUND CABLE AND CONNECTION MATERIAL SHOULD BE OF SUFFICIENT MECHANICAL STRENGTH TO MINIMIZE THE POSSIBILITY OF GROUND DISCONNECTIONS. PROTECTION TO LESS THAN 5 mA MAY BE ADVISABLE WHERE REFLEX ACTION COULD CAUSE PROBLEMS.

• WORK BENCHES, CONDUCTIVE MATS, AND OTHER ESD WORK STATION GROUNDS USED TO DISCHARGE STATIC ELECTRICITY SHOULD BE CONNECTED TO A COMMON POINT AND THAT POINT CONNECTED TO EARTH, POWER SYSTEM OR SHIP'S HULL GROUND AS APPROPRIATE, THROUGH THE APPROPRIATE RESISTANCE. WRIST STRAPS SHOULD BE CONNECTED TO THE GROUND POINT (E.G., SCREW HEAD) ON THE WORK BENCH TOP. WORK BENCH GROUNDS SHOULD NOT BE CONNECTED IN SERIES WITH ONE ANOTHER.

• WHERE DISCRETE RESISTORS ARE USED FOR ESD PROTECTIVE WORK BENCH GROUNDS TO GROUND STATIC ELECTRICITY, THEY SHOULD BE LOCATED AS CLOSE AS POSSIBLE TO THE ITEM BEING GROUNDED (E.G., AT THE BRACELET END OF A WRIST STRAP) TO REDUCE THE CHANCES OF BYPASSING THE GROUND RESISTANCE AS MAY OCCUR WHEN A GROUND STRAP CABLE WITH FRAYED INSULATION CONTACTS A HARD GROUND.

• IN TRANSFERRING ESD SENSITIVE PARTS FROM ONE CARRIER OR LOCATION TO ANOTHER, THE TWO CARRIERS, HOLDERS OR CONTAINERS SHOULD BE ELECTRICALLY CONNECTED BEFORE AND DURING THE TRANSFER TO EQUALIZE ELECTRICAL POTENTIALS OF BOTH CARRIERS.

(f) ESD GROUNDING RESISTANCE CONSIDERATIONS

WHEREAS THE SAFETY CONSIDERATIONS PROVIDE THE MINIMUM RESISTANCE TO GROUND FOR PROTECTION OF PERSONNEL, THE MAXIMUM RESISTANCE TO HARD GROUND FOR PERSONNEL GROUNDING SHOULD BE LIMITED BY THE DECAY TIME FOR AN ELECTROSTATIC CHARGE. THIS DECAY TIME BASED UPON THE RC CONSTANT

(CONSIDERING THE CAPACITANCE AND RESISTANCE OF THE HUMAN MODEL OF FIGURE 10.1 AND THE RESISTANCE OF THE GROUND TECHNIQUE TO HARD GROUND) SHOULD BE SHORT ENOUGH TO DISSIPATE CHARGES AT OR BELOW THE RATE AT WHICH THEY ARE NORMALLY GENERATED. IN ORDER TO LIMIT RESIDUAL VOLTAGES CAUSED BY STATIC GENERATION AT A TYPICAL ESD GROUNDED WORK BENCH TO APPROXIMATELY 10 VOLTS THE MAXIMUM RESISTANCE TO HARD GROUND SHOULD NOT EXCEED 10 MEGOHMS.

VIII. ESD PROTECTIVE EQUIPMENT

A. GENERAL

VARIOUS TYPES OF EQUIPMENT ARE AVAILABLE FOR CONTROLLING AND MONITORING STATIC ELECTRICITY. THEY INCLUDE:

- IONIZERS
- ESD PROTECTIVE TOOLS
  - SPECIAL SOLDERING IRONS, SOLDER SUCKERS
- STATIC DETECTORS AND ALARMS
- PORTABLE ESD WORK STATION KITS
- SPECIAL ESD TEST EQUIPMENT

ALL OF THE ITEMS TO BE DISCUSSED HEREIN ARE NOT NEEDED IN ALL ESD PROTECTED AREAS. THE INTENT OF THIS DISCUSSION IS TO DESCRIBE THE DIFFERENT TYPES OF ESD PROTECTIVE EQUIPMENT WHICH ARE PRESENTLY AVAILABLE.

B. IONIZERS

IONIZERS DISSIPATE ELECTROSTATIC CHARGES BY IONIZING AIR MOLECULES, FORMING BOTH POSITIVE AND NEGATIVE IONS. THE POSITIVE IONS ARE ATTRACTED TO NEGATIVELY CHARGED OBJECTS AND NEGATIVE IONS TO POSITIVELY CHARGED OBJECTS RESULTING IN CHARGE NEUTRALIZATION.

IONIZERS COME IN THE FORM OF STATIC NEUTRALIZER BARS, BLOWERS AND IONIZER NOZZLES. IONIZED AIR CAN BE USED WHERE EFFECTIVE GROUNDING CANNOT BE ACCOMPLISHED TO BLEED-OFF STATIC CHARGES OR TO DISSIPATE IMMOBILE CHARGES ON INSULATORS. IONIZERS ARE ESPECIALLY USEFUL IN DISSIPATING CHARGES WHERE SPRAYING ACTIONS (E.G., SANDBLASTING, SPRAY CLEANING, AIR FLOW FOR CLEAN ROOMS, TEMPERATURE CHAMBERS, OR PAINTING) ARE PERFORMED. TECHNIQUES COMMONLY EMPLOYED TO IONIZE AIR ARE: RADIOACTIVE AND ELECTRIC STATIC COMB.

RADIOACTIVE MATERIAL PROVIDES ALPHA PARTICLES WHICH COLLIDE WITH AIR MOLECULES FORMING POSITIVELY CHARGED MOLECULES AND ELECTRONS. THE ELECTRICAL TECHNIQUE EMPLOYS A HIGH VOLTAGE SQUARE WAVE SIGNAL TO A STATIC COMB. THE STATIC COMB, SIMILAR TO THE LIGHTNING ROD CONCEPT, EMPLOYS SHARP NEEDLE POINTS WHERE THE CHARGE CONCENTRATION ON THE POINT CAN IONIZE AIR (BASED ON THE PRINCIPLE THAT FROM A NON-SPHERICAL BODY THE SELF-REPULSION OF THE CHARGE WILL MAKE IT CONCENTRATE ON THE SURFACES HAVING THE LEAST RADIUS OF CURVATURE). THE RADIOACTIVE MATERIAL USED IN IONIZED AIR BLOWERS IS PROVIDED UNDER LICENSE FROM THE U.S. NUCLEAR REGULATORY COMMISSION AND THEREFORE BLOWERS USING RADIOACTIVE MATERIALS ARE LEASED. IN ADDITION, DUE TO HALF-LIFE CONSIDERATIONS, THE RADIOACTIVE MATERIALS MUST BE REPLACED PERIODICALLY (TYPICALLY ONCE A YEAR).

IONIZERS SHOULD PROVIDE NEAR EQUAL AMOUNTS OF POSITIVE AND NEGATIVE IONS TO DISSIPATE BOTH THE NEGATIVE AND POSITIVE CHARGES PRODUCED WHEN STATIC ELECTRICITY IS GENERATED. PLACEMENT OF IONIZERS SHOULD BE IN ACCORDANCE WITH MANUFACTURER'S RECOMMENDATIONS. MANUFACTURER'S SPECIFICATIONS NORMALLY PROVIDE DATA WITH RESPECT TO DECAY TIME VS THE DISTANCE AND THE ANGLE OF THE IONIZER TO THE CHARGE GENERATOR. IONIZERS CAN TAKE SEVERAL SECONDS OR EVEN MINUTES TO DISSIPATE CHARGES, DEPENDING UPON THE AMOUNT OF CHARGE AND THE DISTANCE OF THE CHARGE FROM THE IONIZING SOURCE. IONIZERS SHOULD BE TURNED ON FOR AT LEAST TWO TO THREE MINUTES TO BUILD UP IONIZATION IN THE AIR PRIOR TO HANDLING ESDS ITEMS. IONIZERS CAN LEAVE RESIDUAL VOLTAGES HIGH ENOUGH TO DAMAGE SOME SENSITIVE ESDS ITEMS. SELECTION AND PLACEMENT OF IONIZERS FOR ADEQUATE ESD CONTROL WILL REQUIRE MEASUREMENT OF RESIDUAL VOLTAGES IN THE AREA TO BE PROTECTED AND COMPARISON WITH THE VOLTAGE SENSITIVITY LEVELS OF ESDS ITEMS BEING HANDLED.

FROM A SAFETY STANDPOINT IT SHOULD BE NOTED THAT: SOME IONIZERS DEVELOP HIGH VOLTAGES WHICH COULD CAUSE DANGEROUS ELECTRICAL SHOCK TO

PERSONNEL; OTHER CONSIDERATIONS IN THE USE OF ELECTRICAL IONIZERS ARE THE DEVELOPMENT OF ELECTROMAGNETIC INTERFERENCE AND THE PRODUCTION OF OZONE WHICH CAN CAUSE NAUSEA IN PERSONNEL. (NOTE: CODE OF FEDERAL REGULATIONS OCCUPATIONAL SAFETY AND HEALTH STANDARD, AIR CONTAMINANTS, TABLE Z-1, PART 1910.1000, CHAPTER XVII, TITLE 29 DEFINES THE MAXIMUM ALLOWABLE CONCENTRATION FOR OZONE IN A PERSONNEL WORK AREA). NUCLEAR IONIZERS COULD AFFECT NUCLEAR BADGES WORN BY PERSONNEL IN NUCLEAR AREAS.

C. ESD PROTECTIVE TOOLS

TOOLS COMMONLY USED IN THE ASSEMBLY AND TEST OF ELECTRONIC EQUIPMENT CAN HOLD DAMAGING LEVELS OF STATIC ELECTRICITY. THESE INCLUDE:

- SOLDER SUCKERS
- SOLDERING IRONS
- COMMON HAND TOOLS (SCREW DRIVERS, PLIERS, ETC.) WITH PLASTIC HANDLES
- VOLT OHM METER (VOMs) AND OTHER TEST EQUIPMENT PROBES

COMMONLY USED SOLDER SUCKERS ARE MADE OF PLASTIC AND WHEN TRIGGERED CAN GENERATE MANY THOUSANDS OF VOLTS OF STATIC ELECTRICITY. SOLDERING IRONS WITH UNGROUNDED TIPS CAN CARRY SUFFICIENT STATIC CHARGES ON THE SOLDERING IRON TIPS TO DAMAGE MANY ESDS PARTS. ONLY SOLDERING IRONS WITH GROUNDED TIPS SHOULD BE USED IN ESD PROTECTED AREAS.

COMMON HAND TOOLS WITH PLASTIC OR RUBBER COATED HANDLES CAN CREATE SUBSTANTIAL ELECTROSTATIC CHARGES ALTHOUGH WITH USE SWEAT AND DIRT CAN RENDER THE HANDLES SUFFICIENTLY CONDUCTIVE. HAND TOOLS WITH METAL HANDLES CAN BE USED OR THE PLASTIC HANDLES CAN BE TREATED WITH ANTISTATS TO ENSURE THAT THEY ARE ESD PROTECTIVE.

THE PROBES ON VOMs AND OTHER MEASURING INSTRUMENTATION CAN ALSO HOLD SUBSTANTIAL ELECTROSTATIC CHARGES AND SHOULD BE SHORTED TO GROUND PRIOR TO POWERING UP. BENCH TEST EQUIPMENT SHOULD BE GROUNDED VIA A THREE-PRONGED PLUG TO ASSURE EQUIPMENT CASES DO NOT HAVE STATIC CHARGES OR HAVE HIGH FLOATING GROUNDS.

TEMPERATURE CHAMBERS SHOULD BE EQUIPPED WITH GROUNDED BAFFLES TO DISSIPATE CHARGES FROM CIRCULATED AIR. ALTERNATELY IONIZED AIR CAN BE USED IN THE CHAMBER TO DISSIPATE STATIC CHARGES CAUSED BY THE AIR FLOW OR SHIELDS CAN BE USED TO DIVERT THE CHARGED AIR AWAY FROM ESDS ITEMS IN THE CHAMBER. CAUTION SHOULD BE USED IN COOLING CHAMBERS WITH CO_2 THE FLOW OF WHICH CAN GENERATE HIGH STATIC CHARGES. ESDS PARTS BEING TESTED IN A CHAMBER SHOULD BE PLACED IN CONDUCTIVE BOXES OR TRAYS ON GROUNDED METAL RACK WITHIN THE CHAMBER. THE THERMAL STABILITY CHARACTERISTICS OF ESD PROTECTIVE MATERIALS USED IN TEMPERATURE CHAMBERS SHOULD BE SUITABLE OVER THE TEMPERATURE RANGES TESTED.

D. ELECTROSTATIC DETECTORS AND ALARMS

(1) ELECTROSTATIC DETECTORS

TYPES OF STATIC DETECTORS INCLUDE ELECTROMETER AMPLIFIERS, ELECTROSTATIC VOLTMETERS, ELECTROSTATIC FIELD METERS, AND LEAF DEFLECTION ELECTROSCOPES. COMMONLY USED DETECTORS INCLUDE ELECTROSTATIC FIELD METERS. MOST OF THESE METERS ARE BATTERY OPERATED AND THEREFORE QUITE PORTABLE. FIELD METERS PROVIDE READINGS OF THE ELECTROSTATIC FIELDS PRODUCED BY CHARGED OBJECTS USING A NON-CONTACT PROBE OR SENSOR, AND PROVIDE READINGS IN ELECTROSTATIC FIELD STRENGTH OR ELECTROSTATIC VOLTAGE AT A CALIBRATED DISTANCE(S) FROM A CHARGED OBJECT. SOME ELECTROSTATIC FIELD METERS USE RADIOACTIVE SOURCES SIMILAR TO THOSE OF RADIOACTIVE IONIZERS. THESE

RADIOACTIVE METERS COULD AFFECT NUCLEAR BADGES WORN BY PERSONNEL IN NUCLEAR AREAS. ELECTROSTATIC DETECTORS CAN BE USED FOR MONITORING THE MAGNITUDE OF ELECTROSTATIC CHARGES EXISTING ON MATERIALS, OBJECTS OR PERSONNEL. ADDITIONALLY, THEY CAN BE USED TO MEASURE THE APPROXIMATE MAGNITUDE OF ELECTROSTATIC CHARGES GENERATED BY PERSONNEL MOVEMENTS (E.G., WALKING) AND THE TRIBOELECTRIC CHARGES GENERATED BY RUBBING TWO SUBSTANCES. ELECTROSTATIC METERS CAN ALSO BE USED TO EVALUATE THE ABILITY OF PACKAGING MATERIAL TO SHIELD AGAINST ELECTROSTATIC FIELDS BY ENCLOSING THE METER PROBE OR SENSOR INSIDE THE PACKAGING MATERIAL AND MOVING A CHARGED OBJECT NEAR AND AROUND THE COVERED PROBE.

THE BASIC LIMITATION OF MOST ELECTROSTATIC METERS IS THEIR RESPONSE TIME. MOST METERS ARE INCAPABLE OF RESPONDING TO PULSES WITH FAST RISE AND DECAY TIMES (I.E., SHORT PULSE WIDTHS). FOR MEASUREMENT OF PULSES WITH VERY FAST RISE AND DECAY TIMES, A HIGH SPEED STORAGE OSCILLISCOPE CAN BE USED.

FOR CASUAL MONITORING AND FOR CERTIFYING ESD PROTECTED AREAS WHERE ONLY MODERATELY SENSITIVE OR MARGINALLY SENSITIVE ESDS ITEMS ARE HANDLED, SMALL PORTABLE ELECTROSTATIC FIELD METERS MAY BE USED. HOWEVER, FOR CERTIFYING AREAS WHERE HIGHLY SENSITIVE ESDS ITEMS ARE HANDLED MORE ACCURATE LABORATORY-TYPE DETECTORS SHOULD BE USED. IN SUMMARY, CHARACTERISTICS TO CONSIDER IN SELECTING AN ELECTROSTATIC DETECTOR ARE:

- SENSITIVITY (MINIMUM VOLTAGE LEVEL THAT CAN BE ACCURATELY MEASURED);
- RESPONSE TIME;
- RANGE(S) OF VOLTAGES THAT CAN BE MEASURED;
- ACCURACY IN VARIOUS RANGES;
- RADIOACTIVE OR ELECTRICALLY OPERATED;

- PORTABILITY;
- RUGGEDNESS;
- SIMPLICITY OF OPERATION AND READABILITY;
- ACCESSORIES (REMOTE PROBES, STRIP CHART RECORDER OUTPUT).

(2) STATIC SENSORS AND ALARMS

STATIC LEVEL ALARM SYSTEMS ARE AVAILABLE FOR CONSTANTLY MONITORING THE LEVELS OF STATIC ELECTRICITY GENERATED IN AN ESD PROTECTED AREA. SOME SYSTEMS HAVE MULTIPLE REMOTE SENSORS WHICH CAN MONITOR SEVERAL STATIONS SIMULTANEOUSLY. SOME SYSTEMS ALSO CONTAIN STRIP CHART RECORDERS WHICH PROVIDE A PERMANENT RECORD OF STATIC LEVELS WITHIN AN AREA.

E. PORTABLE ESD WORK STATION KITS

PORTABLE ESD WORK STATION KITS ARE AVAILABLE FOR USE IN THE FIELD OR WHERE PERMANENT ESD PROTECTED AREAS ARE NOT NEEDED. THESE KITS TYPICALLY INCLUDE AN ESD PROTECTIVE WORK BENCH COVER OR PAD (WITH GROUNDING CABLE AND A PERSONNEL GROUND STRAP), AND AN ASSORTMENT OF ESD PROTECTIVE PACKAGING AND SHUNTING MATERIAL.

THESE PORTABLE WORK STATION KITS PROVIDE ONLY THE BARE NECESSITIES OF AN ESD PROTECTED AREA AND MUST BE SUPPLEMENTED WITH GOOD ESD PROTECTIVE HANDLING PROCEDURES. STEPS HAVE BEEN TAKEN TO PROVIDE PORTABLE ESD WORK STATION KITS FOR "2M" STATIONS USED ABOARD MANY NAVY SHIPS.

F. SPECIAL ESD TEST EQUIPMENT

SPECIAL ESD TEST EQUIPMENT HAS BEEN DEVELOPED FOR TESTING OF ESD MATERIALS AS PREVIOUSLY DISCUSSED. THIS INCLUDES FIXTURES FOR PERFORMING RESISTIVITY AND DECAY TIME MEASUREMENTS.

(1) ELECTROSTATIC DISCHARGE SIMULATOR

THESE ARE COMMERCIALLY AVAILABLE INSTRUMENTS DESIGNED TO EVALUATE THE ELECTROSTATIC DISCHARGE CHARACTERISTICS OF ESDS PARTS. A TYPICAL SIMULATOR INCORPORATES A HUMAN MODEL TEST CIRCUIT THAT IS DISCHARGED ACROSS ANY SELECTED PINS OF THE PART UNDER TEST. A BUILT-IN VARIABLE POWER SUPPLY MAY PROVIDE A TESTING RANGE OF 20 VOLTS TO 15,000 VOLTS. SOME OF THESE INSTRUMENTS INCORPORATE A VARIABLE GROUND PATH WHICH CAN USE EITHER RESISTORS, RC NETWORKS, OR ACTUAL MATERIAL USED IN BAGS, TABLE TOPS, ETC. SO THAT A GIVEN DISCHARGE LEVEL CAN BE EVALUATED UNDER DIFFERENT REAL LIFE OPERATING CONDITIONS. OTHER ESD SIMULATORS ARE AVAILABLE FOR DISCHARGING VIA A SPARK TO TEST THE EFFECTS OF SPARK INDUCED EMI ON COMPUTERS, COMPUTER PERIPHERALS AND OTHER DIGITAL EQUIPMENT OR ESDS PARTS.

(2) STATIC DECAY METER

STATIC DECAY METERS THAT MEASURE THE ELECTROSTATIC PROPERTIES OF MATERIALS IN ACCORDANCE WITH FEDERAL STANDARD 101B, METHOD 4046 (REFERENCE 20) ARE COMMERCIALLY AVAILABLE. THIS EQUIPMENT CONSISTS OF A ONE-PIECE UNIT REPLACING THE STANDARD TEST EQUIPMENT (HIGH VOLTAGE POWER SUPPLY, RECORDER, TIMER, ETC.) SETUP SHOWN IN FEDERAL STANDARD 101.

IX. PACKAGING AND MARKING OF ESDS ITEMS

A. GENERAL

AVAILABLE ESD PROTECTIVE PACKAGING MATERIALS HAVE BEEN PREVIOUSLY DISCUSSED IN DETAIL. ESD PROTECTIVE PACKAGING SHOULD PROVIDE PROTECTION FROM THE FOLLOWING:

- PROTECT THE ITEM(S) FROM PHYSICAL DAMAGE, ESPECIALLY TERMINALS AND LEADS. THIS IS A BASIC REQUIREMENT FOR ALL ELECTRONICS PACKAGING.
- PROTECT THE ESDS ITEM FROM ESD DUE TO TRIBOELECTRIC GENERATION DURING HANDLING AND TRANSPORTATION.
- PROTECT THE ESDS ITEM FROM DIRECT DISCHARGE OF AN ESD.
- PROTECT THE ESDS ITEM FROM ELECTROSTATIC FIELDS.

MARKING OF THE PACKAGE IS OF PARAMOUNT IMPORTANCE SO THAT PERSONNEL WHO HANDLE, STORE OR STOW THESE ITEMS ARE AWARE THAT THEY ARE ESDS AND TAKE THE NECESSARY ESD PRECAUTIONS (SEE FIGURE 9.1).

CAUTION

FIGURE 9.1: MIL-STD-129 SENSITIVE ELECTRONIC DEVICE SYMBOL

ESD PROTECTIVE PACKAGING IS REQUIRED INTRA-PLANT DURING TRANSIT BETWEEN ESD PROTECTIVE AREAS WHERE STATIC LEVELS ARE UNCONTROLLED AND WHERE THE ESDS ITEMS COULD BE EXPOSED TO DAMAGING LEVELS OF ESD.

FOR DELIVERY, ESD PROTECTIVE PACKAGING AND MARKING WITH THE MIL-STD-129 (REFERENCE 26) SENSITIVE ELECTRONIC DEVICE CAUTION IS REQUIRED (FIGURE 9.1). THIS MARKING SHOULD ALSO INCLUDE THE FOLLOWING CAUTION STATEMENT:

"OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE ITEMS"

THE ABOVE PACKAGING AND MARKING OF ESDS ITEMS APPLIES TO PARTS, ASSEMBLIES AND EQUIPMENT.

B. PROTECTION AGAINST TRIBOELECTRIC GENERATION

TRIBOELECTRIC GENERATION OF STATIC HAS OCCURRED AS A RESULT OF SLIDING, RUBBING AND SEPARATION OF MATERIALS DURING THE SHOCK AND VIBRATION OF TRANSPORTATION AND HANDLING. THE INTIMATE COVERING OF AN ESDS ITEM SHOULD PROVIDE PROTECTION AGAINST TRIBOELECTRIC GENERATION BETWEEN THE PACKAGING MATERIAL AND THE ESDS ITEM(S). FOR EXAMPLE, MIL-B-81705 TYPE II BAGS OR SIMILAR MATERIAL IN THE FORM OF CARRIERS, CONTAINERS, ESD PROTECTIVE CUSHIONING, BUBBLE PACK OR FOAM CAN BE USED.

C. PROTECTION AGAINST DIRECT DISCHARGE

PROTECTION AGAINST DIRECT DISCHARGE REQUIRES THAT THE DISCHARGE NOT BE CONDUCTED DIRECTLY THROUGH THE PACKAGING MATERIAL TO THE ESDS ITEM. THIS REQUIRES THAT THE INTIMATE LAYER OF PACKAGING PROVIDE ADEQUATE ELECTRICAL RESISTANCE TO THE ESDS ITEM. MOST ESD PROTECTIVE MATERIALS WILL PROVIDE THIS PROTECTION; THE ANTI-STATIC BY BEING HIGHLY RESISTIVE THROUGH THE MATERIAL AND THE CONDUCTIVE BY PROVIDING A SHUNT AROUND THE OUTSIDE OF THE PACKAGING MATERIAL.

D. PROTECTION AGAINST ELECTROSTATIC FIELDS

PROTECTION AGAINST ELECTROSTATIC FIELD REQUIRES A CONDUCTIVE COVERING OR LAYER. AVAILABLE ESD PROTECTIVE MATERIALS THAT CAN BE USED FOR

THIS PURPOSE INCLUDE THE MIL-B-81705 TYPE I AND THE MIL-B-82647 BAGS. OTHER METAL LAMINATED BAGS WILL ALSO NORMALLY HAVE THIS PROPERTY. IT SHOULD BE NOTED THAT MUCH OF THE COMMONLY USED PACKAGING FILLER MATERIALS SUCH AS STYROFOAM "PEANUTS" OR "SHELLS" CAN GENERATE SUBSTANTIAL CHARGES DURING SHIPMENT. THESE HIGHLY CHARGED PIECES OF STYROFOAM CAN RESULT IN STRONG ELECTROSTATIC FIELDS WITHIN THE UNIT PACKAGE.

E. SHUNTING DEVICES

SHUNTING DEVICES WILL PROVIDE LIMITED PROTECTION FOR ESDS ITEMS. FOR ESDS ITEMS THAT DO NOT HAVE CONDUCTIVE CASES VOLTAGES CAN BE INDUCED WITHIN THE ITEMS FROM AN ELECTROSTATIC FIELD BETWEEN THE INSULATIVE CASE AND THE PINS OR TERMINALS WHICH ARE SHORTED BY THE SHUNTING DEVICE. SUCH INDUCED VOLTAGES CAN DAMAGE ESDS ITEMS. TO PROVIDE COMPLETE PROTECTION AN ENCLOSURE (E.G., BAG) OF PROTECTIVE COVERING THAT AFFORDS PROTECTION AGAINST TRIBOELECTRIC CHARGING, DIRECT DISCHARGE, AND ELECTROSTATIC FIELDS SHOULD BE USED. ALSO, FOR SHUNTING DEVICES, TO BE EFFECTIVE SHUNTS, THEY MUST BE HIGHLY CONDUCTIVE WITH RESPECT TO THE IMPEDANCE OF THE ESDS ITEM TO BE PROTECTED. IT SHOULD BE FURTHER NOTED THAT CONDUCTIVE CARBON IMPREGNATED FOAM IS OFTEN USED FOR SHUNTING. WHEN SUCH FOAM IS USED IT SHOULD BE OF A NON-CORROSIVE TYPE HAVING LOW SULFUR AND CHLORINE CONTENT. IN HIGH HUMIDITY CONDITIONS FOAM WITH SUCH IMPURITIES HAVE BEEN KNOWN TO CORRODE ELECTRICAL TERMINALS.

F. NAVY ESD PACKAGING REQUIREMENTS

THE NAVAL SEA SYSTEMS COMMAND AND SHIPS PARTS CONTROL CENTER HAS STANDARD CONTRACT CLAUSES FOR THE PRESERVATION AND PACKAGING OF ESDS ITEMS. ALSO, MIL-STD-758 (REFERENCE 26A) AND MS-90363 (REFERENCE 26B) CONTAIN ESD PROTECTIVE PACKAGING REQUIREMENTS.

G. REPACKAGING FOR DISTRIBUTION

MANY PART MANUFACTURERS TAKE THE PRECAUTIONS NEEDED TO PROTECT ESDS ITEMS DURING MANUFACTURE AND PACKAGE THE ESDS ITEMS IN ESD PROTECTIVE MATERIALS. MOST EQUIPMENT MANUFACTURERS, HOWEVER, PROCURE ESDS PARTS FROM PARTS DISTRIBUTORS WHO OFTEN SPLIT UP PACKAGED QUANTITIES AND FAIL TO RE-PACKAGE ESDS PARTS IN THE PROPER PROTECTIVE PACKAGING. THE HANDLING AND PACKAGING OF ESDS ITEMS AT THE DISTRIBUTOR PRESENTS ONE OF THE MORE DIFFICULT PROBLEMS IN IMPLEMENTING A COMPLETE "CRADLE TO GRAVE" ESD CONTROL PROGRAM ESPECIALLY CONSIDERING THE POSSIBILITY OF INDUCING LATENT DEFECTS INTO THE ESDS PARTS.

X. ESD IN DESIGN

A. GENERAL

IN ORDER TO FULLY ASSESS THE TYPES OF PROBLEMS RESULTING FROM ESD IT IS NECESSARY TO INVESTIGATE: THOSE STRUCTURAL FEATURES MAKING THE PARTS SUSCEPTIBLE TO ESD DAMAGE AND METHODS OF IMPROVING PARTS' DESIGN. ACCORDINGLY, A TOPIC TO EXPLORE IS THE VARIOUS TYPES OF PROTECTIVE CIRCUITRY MANUFACTURERS HAVE INCORPORATED INTO THE PART DESIGNS TO REDUCE SUSCEPTIBILITY TO ESD.

ANY PART OR CIRCUIT THAT INCORPORATES AN ELEMENT CONSISTING OF TWO CONDUCTORS OR A CONDUCTOR AND AN ACTIVE SEMICONDUCTOR AREA SEPARATED BY A THIN DIELECTRIC IS SUSCEPTIBLE TO ESD DAMAGE, ESPECIALLY IF THESE CONDUCTORS ARE DIRECTLY ACCESSIBLE TO ELECTRICAL TERMINALS. STRUCTURES OF THIS TYPE INCLUDE MOS TRANSISTORS, MOS CAPACITORS, N+ GUARD RINGS, AND METALLIZATION CROSSOVERS. THE DEGREE OF SUSCEPTIBILITY OF THESE STRUCTURES TO ESD IS DETERMINED BY THEIR PHYSICAL CHARACTERISTICS SUCH AS THE SIZE OF THE CONDUCTOR AND THE MATERIAL THICKNESS OF THE DIELECTRIC. SUCH ELEMENTS FAIL BY BREAKDOWN OF THE DIELECTRIC DUE TO AN ESD. OTHER PARTS WITH SMALL ACTIVE JUNCTION ELEMENTS ARE ALSO SUSCEPTIBLE TO ESD. SUCH PARTS FAIL DUE TO THERMAL FAILURE (JUNCTION MELT) DUE TO AN ESD.

VARIOUS PROTECTIVE CIRCUITS HAVE BEEN PROPOSED AND IMPLEMENTED IN VARIOUS MANUFACTURERS' CIRCUITS. THESE PROTECTIVE CIRCUITS CONSIST OF RESISTORS, DIODES, FIELD PLATE DIODES, REACH-THROUGH AND PUNCH-THROUGH DIODES, AND SPARK GAP DEVICES. TO DETERMINE THE EFFECTS OF ESD ON PARTS AND ELEMENTS OF PARTS THE PARAMETERS OF THE ESD PULSE MUST BE UNDERSTOOD. THESE PARAMETERS CAN BE DETERMINED BY USE OF A HUMAN MODEL EQUIVALENT CIRCUIT WHICH REPRESENTS THE PRIMARY SOURCE OF AN ESD PULSE.

B. HUMAN MODEL EQUIVALENT CIRCUIT

PERSONNEL ARE THE PRIME SOURCES OF ESD FOR DAMAGING ELECTRICAL AND ELECTRONIC PARTS. ELECTROSTATIC CHARGES GENERATED BY THE RUBBING OR SEPARATION OF MATERIALS ARE READILY TRANSMITTED TO A PERSON'S CONDUCTIVE SWEAT LAYER CHARGING THAT PERSON. WHEN A CHARGED PERSON HANDLES OR COMES IN CLOSE PROXIMITY TO AN ESDS PART, HE CAN DAMAGE THAT PART BY DIRECT CONTACT OR BY SUBJECTING THE PART TO HIS ELECTROSTATIC FIELD. THE ESD FROM A HUMAN CAN BE CLOSELY SIMULATED FOR TEST PURPOSES BY MEANS OF A HUMAN MODEL TEST CIRCUIT AS SHOWN IN FIGURE 10.1. THIS TEST CIRCUIT IS USED IN DOD-STD-1686 AND IS ALSO USED IN MIL-M-38510 (REFERENCE 27) FOR TESTING CMOS AND MOS MICROCIRCUITS. THIS MODEL HAS ALSO BEEN WIDELY USED BY INDUSTRY TO REPRESENT A HUMAN IN ESD TESTING. HUMAN CAPACITANCE AND HUMAN RESISTANCES ARE THE BASIC CIRCUIT ELEMENTS IN A HUMAN MODEL.

(1) HUMAN CAPACITANCE

THE HUMAN BODY, VIEWED AS AN ESD SOURCE, IS A COMPLEX, NONLINEAR NETWORK. IT IS BASICALLY A RESISTIVE BULK, WITH A CONTACT RESISTANCE AND A CAPACITANCE TO GROUND. THE HUMAN BODY CAPACITANCE CAN BE MODELED IN TERMS OF TWO COMPONENTS (REFERENCE 28): THE PARALLEL PLATE CAPACITANCE OF THE SOLES OF THE FEET TO GROUND, AND CAPACITANCE OF THE BODY BULK TO GROUND. THE FOOT CAPACITANCE IS THE MORE VARIABLE, AND DEPENDS UPON THE SIZE OF THE SHOE SOLES, TYPES OF SHOE SOLE MATERIAL, AND SOLE THICKNESS. CONSIDERING A CONDUCTIVE FLOOR, MATHEMATICALLY, THE FOOT CAPACITANCE IS PROPORTIONAL TO THE PRODUCT OF THE SOLE AREA "A" (CM^2) AND THE RELATIVE DIELECTRIC CONSTANT "K" OF THE SOLE, AND INVERSELY PROPORTIONAL TO THE SOLE THICKNESS "t" (CM).

$$C_F = \frac{K\epsilon_0 A}{t} \qquad (35)$$

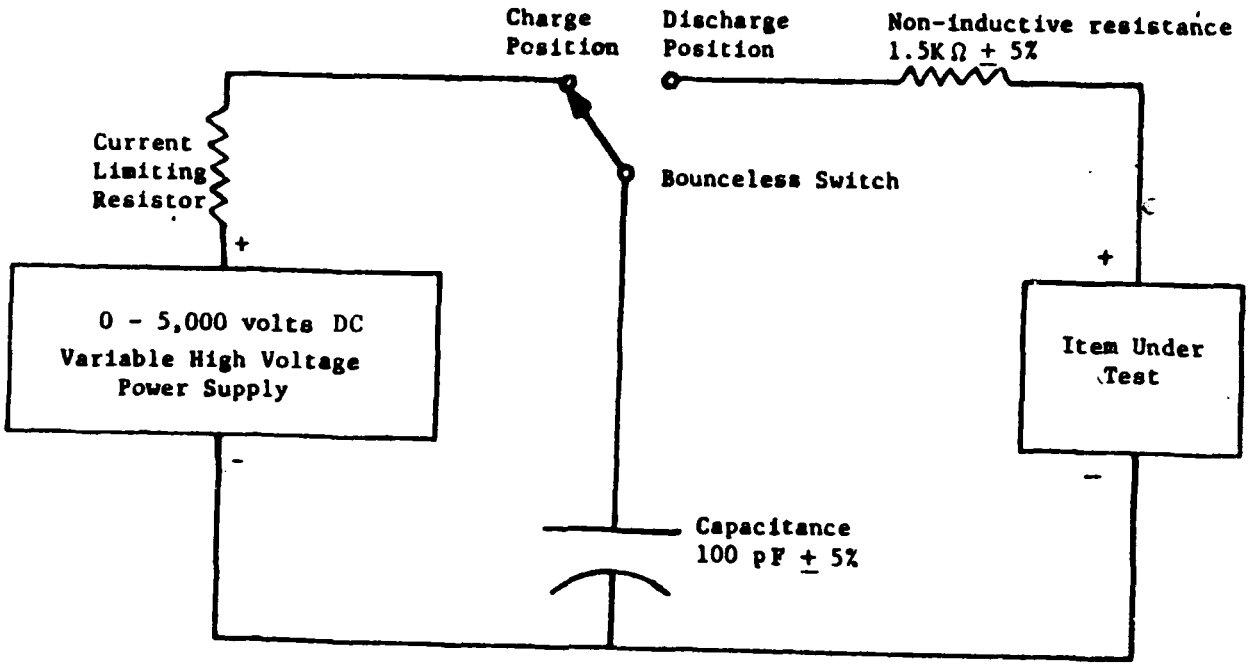


FIGURE 10.1

ESD TEST CIRCUIT

NOTE: Test voltages are measured across the capacitance. The capacitor shall be discharged through the series resistor into the item under test by maintaining the bounceless switch to the discharge position for a time no shorter than required to decay the capacitor voltage to less than 1 percent of the test voltage or 5 seconds, whichever is less. Power supply voltage shall be within a tolerance of ±5 percent of test voltage.

$$C_F = .0886 \frac{KA}{t} \text{ (PICOFARADS)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (36)$$

WHERE:

ε_o = PERMITTIVITY OF FREE SPACE AND IS EQUAL TO 8.86×10^{-14} FARADS PER CM

BODY BULK CAPACITANCE, BY CONTRAST, IS APPROXIMATELY LINEARLY RELATED TO BODY HEIGHT BY THE SIMPLE EQUATION:

$$C_B = 0.55\ H$$

WHERE:

0.55 IS THE NUMBER IN PICOFARADS PER CM OF BODY HEIGHT, H IS THE BODY HEIGHT IN CM

TOTAL BODY CAPACITANCE IS EQUAL TO:

$$C_T = C_F + C_B \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (37)$$

$$= .55\ H + .089\ KA/t \text{ (PICOFARADS)}$$

IT SHOULD BE NOTED THAT THE ABOVE EQUATION CONSIDERS A UNIFORM THICKNESS FOR BOTH THE SHOE SOLE AND HEEL. IF THE SOLE AND HEEL VARY IN THICKNESS OR COMPOSITION, THE FORMULA SHOULD BE MODIFIED ACCORDINGLY.

HUMAN CAPACITANCES CAN BE AS HIGH AS SEVERAL THOUSAND PICOFARADS (PF) BUT MORE TYPICALLY 60 TO 218 PF. A STUDY (REFERENCE 28) PERFORMED ON HUMAN CAPACITANCE SHOWED THAT THE RANGE OF CAPACITANCE FITS A POISSON DISTRIBUTION WITH A VARIANCE OF 7 PF. THIS EXPERIMENTAL DATA

INDICATED THAT APPROXIMATELY 80% OF THE POPULATION TESTED HAD A CAPACITANCE OF 100 PF OR LESS.

(2) HUMAN RESISTANCE

AN APPROPRIATE RESISTANCE VALUE TO BE USED IN THE HUMAN MODEL IS DIFFICULT TO CALCULATE. THE VARIATION IN HUMAN RESISTANCES IS DUE TO VARIATIONS IN THE AMOUNT OF MOISTURE, SALT AND OILS AT THE SKIN SURFACE, SKIN CONTACT AREA AND PRESSURE. MEASURED HUMAN RESISTANCE RANGES FROM 100 TO 100,000 OHMS, BUT TYPICALLY BETWEEN 1,000 AND 5,000 OHMS FOR ACTIONS SUCH AS FINGER-THUMB GRASP, HAND HOLDING AND PALM TOUCH. THESE ARE THE ACTIONS CONSIDERED MOST PERTINENT TO HOLDING OR TOUCHING ESDS PARTS OR CONTAINERS WITH ESDS PARTS. A VALUE OF 1,500 OHMS PROVIDES A LOWER PROBABLE BOUND SIMILAR TO THAT OF THE SELECTED VALUE OF THE 100 PF HUMAN CAPACITANCE.

IN SUMMARY, THE PROPOSED HUMAN MODEL TEST CIRCUIT USES A 100 PF CAPACITANCE AND A 1,500 OHM RESISTANCE.

C. ELECTROSTATIC DISCHARGE TESTING

ESD TESTING ESTABLISHES THE ESD SENSITIVITY OF PARTS BASED UPON THE HUMAN MODEL TEST CIRCUIT AND THE PARTS' ABILITY TO MEET THE PERFORMANCE LIMITS SPECIFIED IN THE APPLICABLE PART SPECIFICATION. ESD TESTING HAS BEEN INCORPORATED IN VARIOUS MIL-M-38510 DETAILED SPECIFICATIONS FOR CMOS PARTS. HOWEVER, TODAY'S SPECIFICATIONS FOR OTHER MICROCIRCUITS, DISCRETE SEMICONDUCTORS, FILM RESISTORS AND CRYSTALS DO NOT HAVE COMPARABLE TEST REQUIREMENTS. THE TEST METHOD PROPOSED HEREIN APPLIES TO ALL TYPES OF ESDS PARTS, DISCRETE ELECTRICAL PARTS, SEMICONDUCTORS AND ALL MICROCIRCUITS, AND COULD ALSO BE USED FOR ASSEMBLIES AND EQUIPMENT ESD SUSCEPTIBILITY TESTING. THE PROPOSED TEST PROCEDURE IS AS FOLLOWS:

(1) SELECTING THE CRITICAL ELECTRICAL PARAMETERS

THE CRITICAL PART ELECTRICAL PARAMETERS SUSCEPTIBLE TO ESD SHOULD BE DETERMINED AND CHARACTERIZED PRIOR TO ESD SENSITIVITY TESTING. PARAMETERS SHOULD BE CHECKED PRIOR TO AND AFTER EACH ESD TEST PULSE. THE PRIMARY DC PARAMETERS FOR DIFFERENT PART TYPES ARE PROVIDED IN TABLE X-A.

(2) SELECTING PIN COMBINATIONS

IN ORDER TO HAVE A COST EFFECTIVE TEST PROCEDURE, THE NUMBER OF PIN COMBINATIONS TO BE SUBJECTED TO ESD TESTING SHOULD BE LIMITED TO THE MOST SUSCEPTIBLE PIN COMBINATIONS. THESE COMBINATIONS CAN BE DETERMINED FROM PAST EXPERIENCE AND PUBLISHED REPORTS (REFERENCES 29 TO 33).

INPUT TERMINALS PULSED WITH RESPECT TO COMMON ARE GENERALLY THE MOST SUSCEPTIBLE MICROCIRCUIT PINS TO ESD. THUS, THIS PIN COMBINATION SHOULD ALWAYS BE INCLUDED IN ESD TESTING. FOR A MULTIPLE INPUT CIRCUIT, THE INPUT SHOULD BE SELECTED EITHER FROM SAMPLE TESTING OR FROM STUDIES ON INTERNAL CIRCUITRY. THE INPUT WITH THE SMALLEST FAN-IN SHOULD BE CHOSEN FOR TESTING SINCE IT OFFERS THE LEAST NUMBER OF PATHS TO SHUNT THE OVERSTRESS PULSE.

OUTPUT PINS WITH RESPECT TO COMMON, AND POWER TERMINALS WITH RESPECT TO COMMON ARE OFTEN LIKELY TO EXPERIENCE ESD OVERSTRESS CONDITIONS. AS IN SELECTING THE CANDIDATE INPUT PIN FOR A MULTIPLE OUTPUT MICROCIRCUIT, THE OUTPUT PIN WITH A MINIMUM OF SHUNT PATHS TO DISSIPATE THE ESD PULSE SHOULD BE TESTED, LIKEWISE, A PIN COMBINATION WITH SMALLER ACTIVE JUNCTION AREAS WOULD BE CHOSEN FOR TESTING OVER A PIN COMBINATION WITH LONGER ACTIVE JUNCTION AREAS.

THE MORE NEGATIVE VOLTAGE PIN OF A MICROCIRCUIT, "V-" OR "GND", IS GENERALLY CHOSEN AS COMMON FOR MICROCIRCUITS EMPLOYING N-P-N

TABLE X-A

PART TYPE DC ELECTRICAL PARAMETERS

PART TYPE	ELECTRICAL PARAMETERS AFFECTED
MICROCIRCUITS:	
CMOS DIGITAL MICRO-	REVERSE BIAS CURRENTS AND BREAKDOWN VOLTAGES OF INPUT PROTECTION DIODES
LINEAR MICROCIRCUITS	INPUT BIAS CURRENTS, SUPPLY CURRENTS, OFFSET VOLTAGE, OPEN LOOP VOLTAGE GAIN
DISCRETE SEMICONDUCTORS:	
DIODE	SOFTENING IN THE BREAKDOWN KNEE AND/OR A REDUCTION IN BREAKDOWN VOLTAGE, OR AS A SHORT OR OPEN
TRANSISTOR	BETA OF TRANSISTOR
FILM RESISTORS:	RESISTANCE SHIFT
CRYSTALS:	OPERATIONAL DEGRADATION

TECHNOLOGY (VIRTUALLY ALL BIPOLAR LOGIC CIRCUITS AND LINEAR DEVICES). THIS CHOICE IS MADE BECAUSE IT RESULTS IN REVERSE BIASING EMITTER-BASE JUNCTIONS (USUALLY THE SOFTEST JUNCTION) WHEN A PART IS PULSED WITH RESPECT TO COMMON. IN TESTING POWERLINE SUSCEPTIBILITY, PULSING IS USUALLY DONE AT THE POSITIVE TERMINAL (+) WITH RESPECT TO COMMON (-).

FOR CERTAIN TECHNOLOGIES AND PART CONSTRUCTION SPECIAL PIN COMBINATIONS MAY BE THE MOST SENSITIVE TO ESD. THE MANUFACTURER'S EQUIVALENT CIRCUIT SCHEMATIC SHOULD BE USED TO AID IN DETERMINING THESE SPECIAL PIN COMBINATIONS. SINCE THESE EQUIVALENT CIRCUIT SCHEMATICS DO NOT ALWAYS REFLECT THE TRUE CONSTRUCTION OF THE MICROCIRCUIT (E.G., PARASITIC CURRENT PATHS), THE SCHEMATIC SHOULD BE SUPPLEMENTED WITH VISUAL INSPECTION OF THE MICRO-CIRCUIT, WHERE PRACTICAL.

GUIDELINES FOR DETERMINING SPECIAL PIN COMBINATIONS INCLUDE PINS HAVING:

- UNPROTECTED MOS GATE TERMINALS
- POORLY PROTECTED MOS GATE PINS
- PINNED-OUT MOS CAPACITORS IN LINEAR MICROCIRCUITS
- THIN OXIDE UNDERPASSES (WHEN KNOWN TO EXIST)
- PIN PAIRS CONNECTED BY A SMALL NUMBER OF JUNCTIONS WITH LITTLE OR NO CURRENT LIMITING ELEMENT

TO ILLUSTRATE THE CONCEPT IN THE LAST GUIDELINE ABOVE, CONSIDER THE TYPICAL MEDIUM SPEED EMITTER COUPLED LOGIC (MECL) 10,000 STRUCTURE SHOWN IN FIGURE 10.2. THE PATH ILLUSTRATED BY THE BOLD LINE SHOWS THAT ONLY TWO JUNCTIONS NEED BE BROKEN DOWN FOR CURRENT TO FLOW DIRECTLY FROM INPUT TO OUTPUT. THERE ARE NO CURRENT LIMITING ELEMENTS IN THAT PATH. POLARITY OF THE MINIMUM PULSE NEEDED TO DAMAGE THE CIRCUIT THROUGH THE INPUT-OUTPUT PATH WILL BE THE INPUT (-) AND OUTPUT (+) WHICH WILL REVERSE BIAS THE EMITTER-BASE JUNCTION OF AT LEAST ONE OF THE TRANSISTORS IN THAT PATH.

THE ORDER OF THE PIN COMBINATIONS TO BE TESTED IS BASED UPON THOSE WHICH TEND TO PRODUCE SINGLE ISOLATED FAILURES. COMBINATIONS WHICH ARE LIKELY TO PRODUCE FAILURES THAT COULD BIAS OTHER TESTS BY PRODUCING SHUNT RESISTIVE PATHS OR BLOW METALLIZATION ARE RUN LAST. USING THIS CRITERION, THE USUAL ORDER OF TEST IS INPUT, OUTPUT, SPECIAL AND POWER. PROPOSED PIN COMBINATIONS TO BE USED FOR ESD TESTING AND RECOMMENDED ORDER OF TEST, WHERE MORE ANALYTICAL METHODS CANNOT BE IMPLEMENTED TO DETERMINE THE MOST SENSITIVE PIN COMBINATIONS ARE PROVIDED IN TABLE X-B.

(3) ESD TEST PROCEDURE

(a) ESD SUSCEPTIBILITY TEST

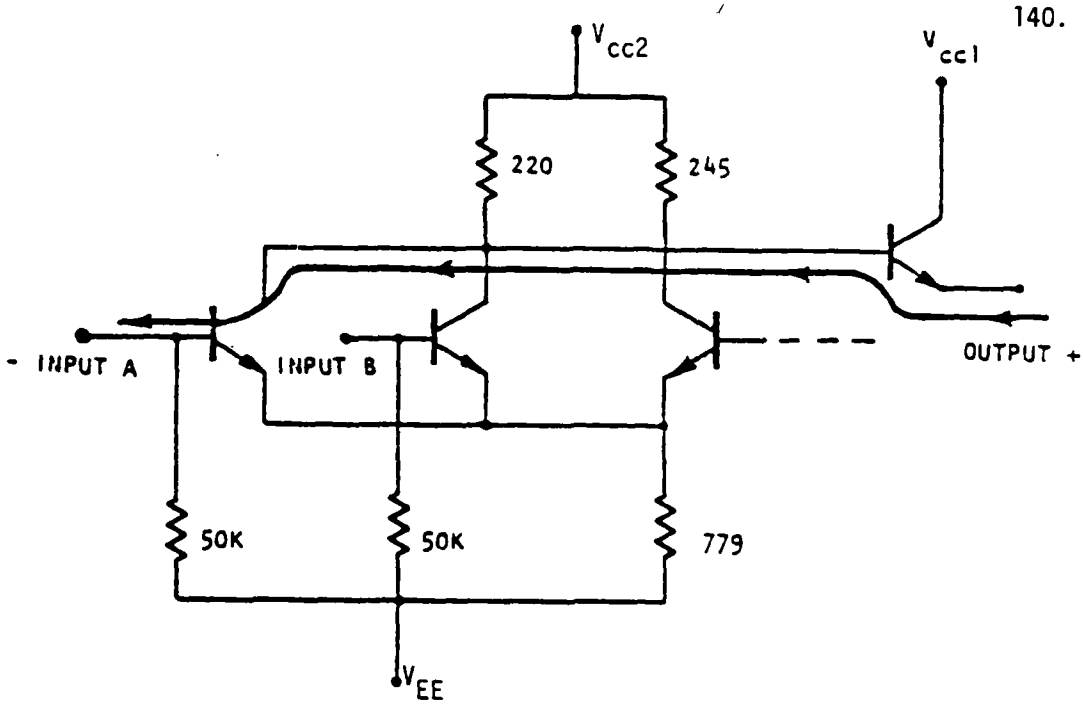


FIGURE 10.2
MECL 10,000 DAMAGE PATH (EMITTER COUPLED LOGIC CIRCUITS)

TABLE X-B
PIN COMBINATIONS FOR ESD TESTING

PART TYPES	PIN COMBINATIONS
ALL PARTS	• ALL PINS TIED TOGETHER (+) TO TOP CENTER OF CASE (-) • ALL PINS TIED TOGETHER (-) TO TOP CENTER OF CASE (+)
RESISTORS	• TERMINAL (+) TO TERMINAL (-)
DIODES	• ANODE TO CATHODE*
TRANSISTORS	• EMITTER TO BASE* • BASE TO COLLECTOR*
DIGITAL MICROCIR-CUITS	• INPUT (+) TO COMMON (-)** • OUTPUT (-) TO COMMON (+)** • INPUT (+) TO OUTPUT (-) • V+ (-) TO COMMON (+)
LINEAR MICROCIR-CUITS	• INPUT (+) TO COMMON (-) • INPUT (+) TO INPUT (-) • OUTPUT (-) TO COMMON (+) • V+ (-) TO COMMON (+)
MOS FETs AND JFETs	• GATE TO SOURCE* • GATE TO DRAIN*

*BOTH POLARITIES (+) TO)-) AND (-) TO (+)
**COMMON - FOR NPN TECHNOLOGY MICROCIRCUITS COMMON IS THE MOST NEGATIVE TERMINAL (I.E., V- OR GND); FOR PNP TECHNOLOGY COMMON IS GND.

((1)) CRITICAL PATH DETERMINATION: (SEE FIGURE 10.3).

(a) STEP 1. TEST THE PART ELECTRICAL PARAMETERS APPLICABLE TO THE PIN COMBINATIONS BEING TESTED. TEST A PART IN ACCORDANCE WITH THE TEST SETUP OF FIGURE 10.1 APPLYING A TEST VOLTAGE OF 1,250 VOLTS TO EACH PIN COMBINATION SHOWN IN TABLE X-B. MEASURE THE PART'S ELECTRICAL PARAMETERS AGAIN AFTER TESTING EACH PIN COMBINATION. TEST UNTIL A FAILURE OCCURS OR UNTIL ALL PIN COMBINATIONS HAVE BEEN TESTED WITHOUT A FAILURE. IF A FAILURE OCCURRED, PROCEED TO STEP 2: IF NO FAILURE OCCURRED, PROCEED TO STEP 4.

(b) STEP 2. TEST A SECOND PART USING THE SAME PIN COMBINATION IN WHICH THE FIRST FAILURE OCCURRED USING 1,250 VOLTS. MEASURE THE PART'S ELECTRICAL PARAMETERS AFTER TESTING AT EACH VOLTAGE LEVEL. IF A SECOND FAILURE OCCURS THE PIN COMBINATION TESTED SHALL BE DESIGNATED A CRITICAL PATH.

(c) STEP 3. CONTINUE WITH STEP 1 FOR THE REMAINING PIN COMBINATIONS TO DETERMINE WHETHER OTHER CRITICAL PATHS EXIST.

(d) STEP 4. REPEAT THE TEST OF STEP 1 FOLLOWED BY STEPS 2 AND 3, AS APPLICABLE, FOR PIN COMBINATIONS NOT PREVIOUSLY DISPLAYING THE CRITICAL PATHS, USING 5,000 VOLTS IN PLACE OF 1,250 VOLTS.

(e) STEP 5. RANK CRITICAL PATHS IN ASCENDING ORDER OF THEIR VOLTAGE SENSITIVITY AS DETERMINED BY STEPS 1 THROUGH 4.

(f) STEP 6. PROCEED TO CLASSIFICATION TESTING.

((2)) ESD CLASSIFICATION TESTING

TESTING SHALL BE PERFORMED AS FOLLOWS (SEE FIGURE 10.4).

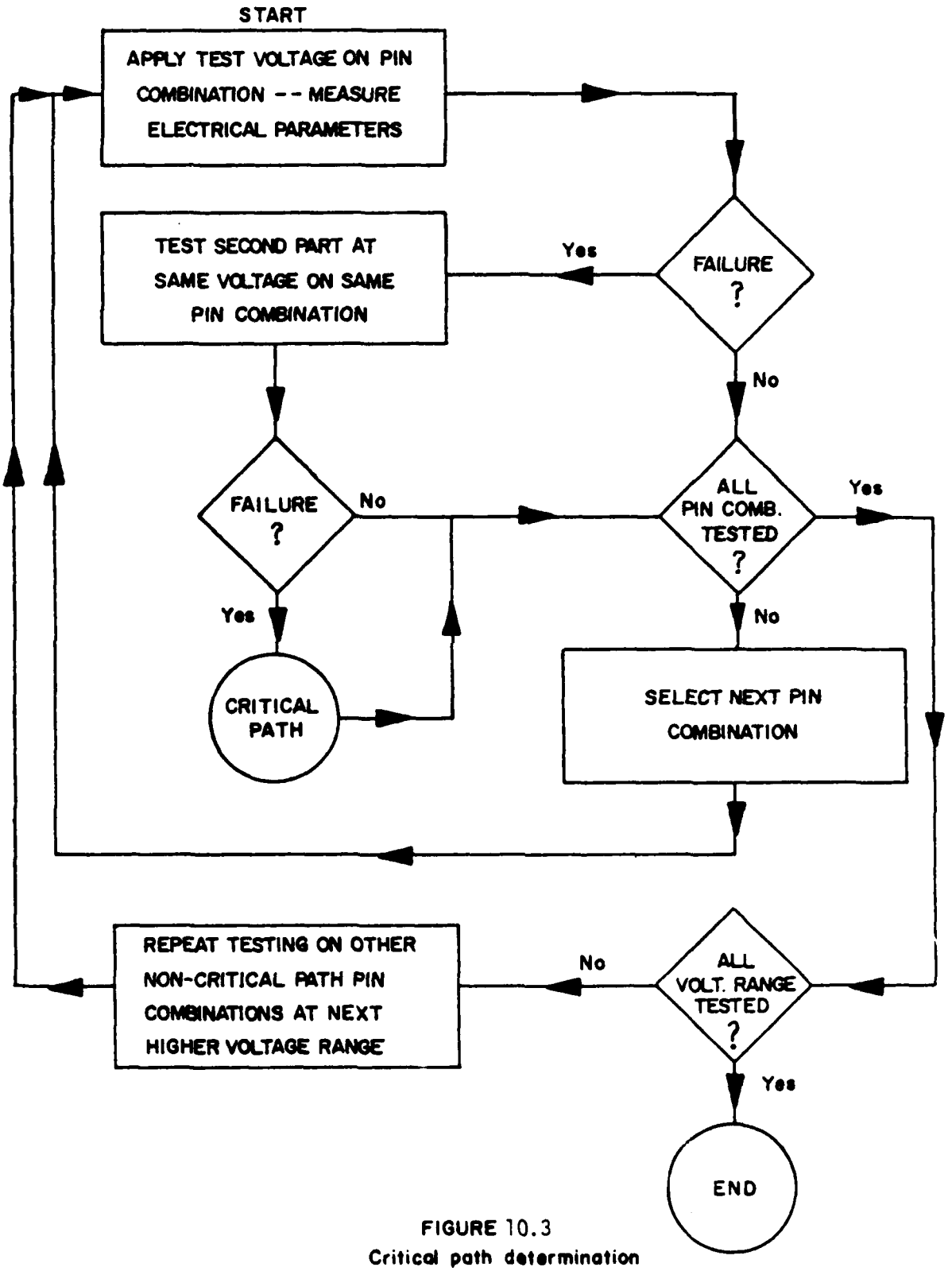


FIGURE 10.3
Critical path determination

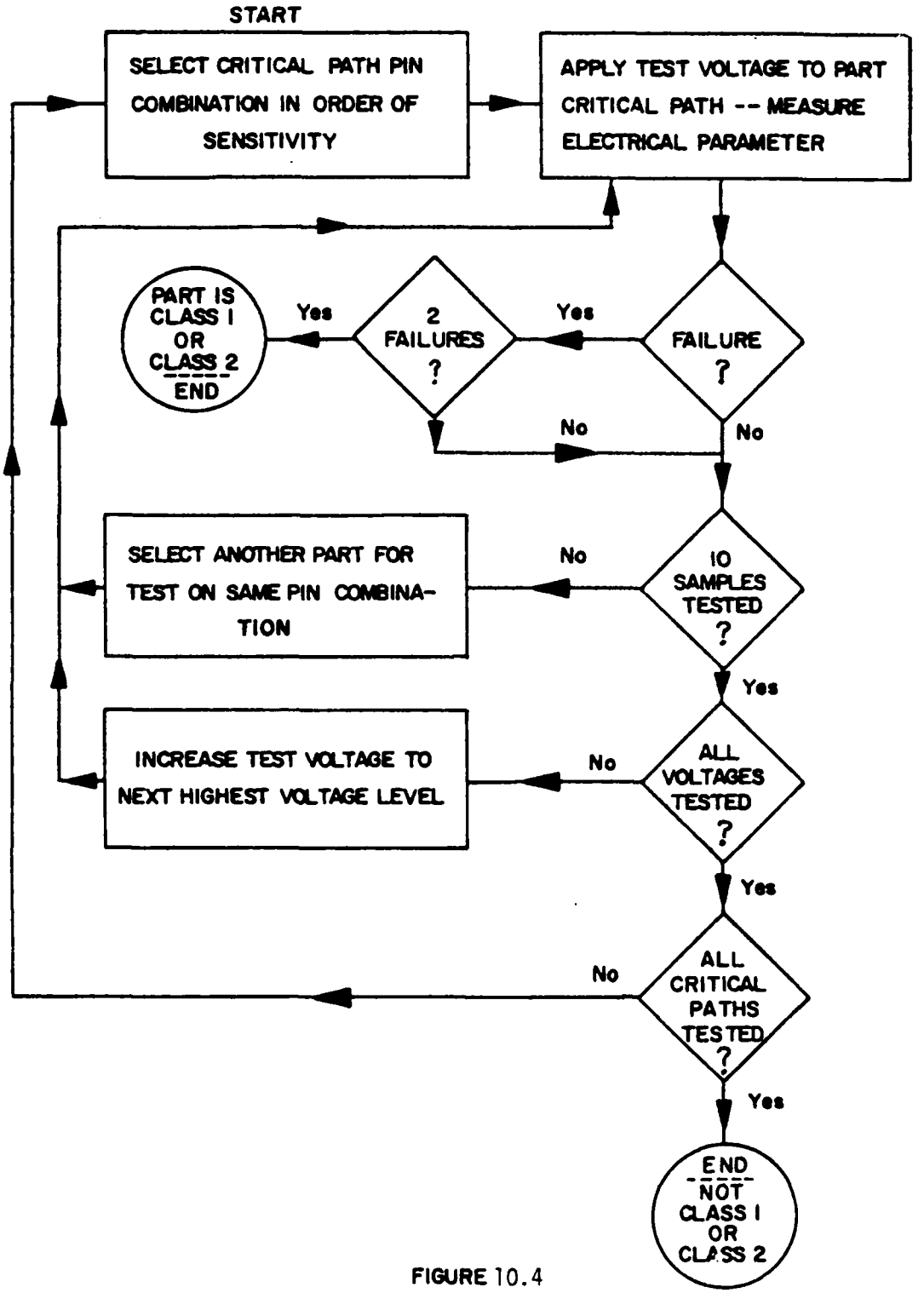


FIGURE 10.4
Classification testing

((a)) STEP 1. TEST A SAMPLE OF PARTS USING THE TEST SETUP OF FIGURE 1 FOR EACH CRITICAL PATH DETERMINED; CONTINUE TESTING UNTIL AT LEAST 10 PARTS HAVE BEEN TESTED, OR UNTIL TWO FAILURES HAVE OCCURRED ON A CRITICAL PATH AT A GIVEN VOLTAGE LEVEL. START WITH THE LOWEST VOLTAGE RANKED CRITICAL PATH:

- IF THE CRITICAL PATH WAS DETERMINED IN STEP 1 AND STEP 2 USE 1,000 VOLTS AS THE TEST VOLTAGE;
- IF THE CRITICAL PATH WAS DETERMINED IN STEP 4 USE 4,000 VOLTS AS THE TEST VOLTAGE.

((b)) STEP 2. IDENTIFY THE SENSITIVE CRITICAL PATHS WHICH EXPERIENCED A MINIMUM OF TWO FAILURES. CLASSIFY THESE PARTS WITH RESPECT TO ESD SENSITIVITY RANGE AS CLASS 1 OR CLASS 2. WHERE NO MORE THAN ONE FAILURE HAS OCCURRED, CLASSIFICATION IS NOT APPLICABLE.

IT SHOULD BE NOTED THAT THE NEED FOR ESD TESTING PER DOD-STD-1686 IS EXPECTED TO BE MINIMAL. APPENDIX A OF DOD-STD-1686 CLASSIFIES ESDS PART TYPES AND IDENTIFIES THEIR ESD VOLTAGE SENSITIVITY RANGE. SENSITIVITY VOLTAGES IN LIEU OF THOSE LISTED IN APPENDIX A OF THE DOD-STD-1686 ARE ACCEPTABLE BASED UPON:

- ESD VOLTAGE LEVEL WHEN SPECIFIED IN THE APPLICABLE MILITARY PART SPECIFICATION SUCH AS THE MIL-M-38510 V-ZAP TEST LEVELS: OR
- ESD VOLTAGE LEVELS FROM TEST DATA OBTAINED IN ACCORDANCE WITH APPENDIX B OR A TEST METHOD SIMILAR TO THAT OF DOD-STD-1686, APPENDIX B, AND APPROVED BY THE ACQUIRING ACTIVITY. COPIES OF THE TEST DATA AND TEST PROCEDURES ARE REQUIRED TO BE AVAILABLE FOR REVIEW BY THE ACQUIRING ACTIVITY.

(b) STEP-STRESS TESTING

WHEN IT IS DESIRED TO DETERMINE THE APPROXIMATE VOLTAGE

SENSITIVITY OF AN ESDS PART, A FORM OF STEP-STRESS TESTING USING A MINIMUM SAMPLE SIZE OF 10 PARTS COULD BE PERFORMED AS FOLLOWS:

- CHECK KEY PARAMETERS OF EACH PART PRIOR TO TEST TO VERIFY THAT IT IS WITHIN SPECIFICATION.

- START WITH A VOLTAGE KNOWN TO BE BELOW THE PART DAMAGE THRESHOLD, OR A LOW VOLTAGE SUCH AS 100 VOLTS. APPLY A VOLTAGE PULSE TO THE MOST SENSITIVE CRITICAL PATH PIN COMBINATION. WHERE THE CRITICAL PATH PIN COMBINATIONS ARE NOT KNOWN FOLLOW THE PROCEDURE OF X,C,(3),(a),((1)).

- MEASURE THE KEY PERFORMANCE PARAMETERS OF EACH PART TESTED ABOVE. IF THE SAME PARAMETER OF TWO OR MORE TESTED PARTS IS OUT OF SPECIFICATION LIMITS, TERMINATE THE TESTING AND DESIGNATE THE VOLTAGE SENSITIVITY EQUAL TO THE APPLIED TEST VOLTAGE.

- IF THE VOLTAGE SENSITIVITY LEVEL CANNOT BE DETERMINED FROM THE ABOVE TESTING, INCREASE THE VOLTAGE IN STEPS (SUCH AS 100 VOLT INCREMENTS) AND CONDUCT PERFORMANCE TESTS UNTIL AT LEAST TWO PARTS EXHIBIT THE SAME PERFORMANCE PARAMETER OUT OF SPECIFICATION LIMITS. AT VOLTAGE LEVELS OF 3,000 VOLTS OR HIGHER, 1,000 VOLT INCREMENTS SHOULD BE USED TO SHORTEN TESTING.

- IF THE INTENT OF THE TESTING IS TO DETERMINE THE STATISTICAL DISTRIBUTION OF ESD SENSITIVITY, A SAMPLE SIZE OF AT LEAST 25 PARTS SHOULD BE STEP-STRESS TESTED TO FAILURE, AND A HISTOGRAM PLOTTED SHOWING THE NUMBER OF PART FAILURES AT DIFFERENT TEST VOLTAGES.

(4) LATENT DEFECT TESTING

THE SUSCEPTIBILITY OF ESDS PARTS TO LATENT DEFECTS CAN ALSO BE EVALUATED BY ESD TESTING. ONE METHOD IS A FORM OF MULTIPLE PULSE TESTING WHERE ESDS PARTS ARE PULSED BELOW (E.G., 25%) THEIR KNOWN SENSITIVITY LEVELS WITH MULTIPLE DISCHARGES. THE THEORY TO THIS TESTING IS THAT ESD

DAMAGE IS CUMULATIVE AND EACH SUCCEEDING PULSE FURTHER WEAKENS THE PART. THE USE OF MULTIPLE DISCHARGE TESTING HAS A REAL LIFE MEANING SINCE PARTS CAN BE EXPOSED TO ESD PULSES MANY TIMES DURING PRODUCTION, PACKAGING, TRANSPORTATION, RECEIPT INSPECTION, KITTING, ASSEMBLY, TEST AND MAINTENANCE OVER THEIR LIFE. ANOTHER LATENT DEFECT TEST METHOD IS TO SUBJECT A SAMPLE OF PARTS TO SINGLE OR MULTIPLE DISCHARGES BELOW THEIR ESD DAMAGE THRESHOLDS, AND PUT THE PULSED PARTS ON LIFE TEST WITH A CONTROL SAMPLE NOT SUBJECTED TO THE ESD PULSING. IT SHOULD BE NOTED THAT ACCELERATED LIFE TESTING AT ELEVATED TEMPERATURE COULD RESULT IN HEALING AND INVALIDATE THE TEST RESULTS. STATISTICAL EVALUATION OF THE LIVES OF THE TWO SAMPLES CAN BE USED TO DETERMINE THE EFFECTS OF ESD LATENT DEFECT FAILURE MECHANISMS ON PART LIFE.

> CAUTION: TOO RAPID REPETITION OF DISCHARGES COULD BUILD UP INTERNAL HOT SPOTS WEAKENING THE PART. IN VIEW OF THE ABOVE, THE DISCHARGES SHOULD BE TIME SPACED TO ALLOW FOR COOLING WITHIN THE PART.

(5) OTHER ESD PART TESTING CONSIDERATIONS

MOST PARTS WHICH ARE SENSITIVE TO ESD ARE ALSO SENSITIVE TO ELECTROMAGNETIC PULSES. SOME OF THESE PARTS ARE ALSO SENSITIVE TO MAGNETIC FIELDS AND RADIOACTIVE FIELDS. ELECTROMAGNETIC PULSES (EMP) CAUSED BY HIGH VOLTAGE IN THE FORM OF A SPARK COULD CAUSE PART FAILURE BESIDES CAUSING EQUIPMENT SUCH AS COMPUTERS TO TEMPORARILY MALFUNCTION. ESD SPARK TESTING CAN BE PERFORMED BY DISCHARGING THE ESD IN THE FORM OF A SPARK ACROSS A SPARK GAP (SIZED FOR THE ESD TEST VOLTAGE) OR BY SLOWLY BRINGING THE HIGH VOLTAGE TEST LEAD OF THE TEST CIRCUIT CLOSE TO THE CONDUCTIVE LID (WHERE APPLICABLE) OR METAL TERMINAL OF A PART UNTIL THE VOLTAGE IS DISCHARGED IN THE FORM OF A SPARK.

ANOTHER ESD TESTING CONSIDERATION IS TO PERFORM TESTING ON LOT SAMPLES OF PARTS USED IN LARGE QUANTITIES. DIFFERENCES IN LOTS FROM THE SAME MANUFACTURER AND DIFFERENCES AMONG LOTS OF A MANUFACTURER COULD RESULT IN VARIATIONS IN ESD SENSITIVITY FOR THE SAME PART TYPE. LOT ESD TESTING OF PARTS ON A SAMPLE BASIS COULD BE USED AS A QUALITY CONTROL CHECK ON PURCHASED PARTS.

(6) ASSEMBLY AND EQUIPMENT ESD TESTING

THE USE OF PART TESTING PROCEDURES FOR AN ASSEMBLY AND AN EQUIPMENT COULD BE PROHIBITIVE IN TERMS OF TEST SAMPLE COSTS. CLASSIFICATION TECHNIQUES FOR ASSEMBLY AND EQUIPMENT SHOULD BE BASED EITHER: (1) CONSERVATIVELY, BASED UPON THE MOST ESDS PART CONTAINED IN THAT ASSEMBLY, OR (2) VIA A DETAILED CIRCUIT ANALYSIS OF THE VOLTAGE PROTECTION AFFORDED BY THE ASSEMBLY LEVEL ESD PROTECTION CIRCUITRY. ESD TESTING AT THE ASSEMBLY OR EQUIPMENT LEVEL DUE TO THE HIGHER COST OF REPAIR MAY BE JUSTIFIED WHERE LARGE PRODUCTION QUANTITIES ARE INVOLVED. SUCH TESTING WOULD BE VALUABLE IN VERIFYING THE ABILITY OF THE EQUIPMENT OR ASSEMBLY PROTECTIVE CIRCUITRY TO PROTECT HIGHLY SENSITIVE ESDS PARTS THEREIN (E.G., QUALIFICATION TESTING).

THE SECOND APPROACH CAN RESULT IN AN OPTIMISTIC CATEGORIZATION OF ESDS ASSEMBLIES SINCE THE ESD PROTECTION CIRCUITRY MAY NOT PROVIDE PROTECTION AGAINST ESD INDUCED BY ELECTROSTATIC FIELDS OR BY DIRECT ESD THROUGH SINGLE POINT CONTACT WITH THE PART BODY OR CONNECTIONS OF THE PRINTED CIRCUIT BOARD (PCB). SUCH FAILURES CAN OCCUR REGARDLESS OF WHETHER OR NOT THE PRINTED CIRCUIT ASSEMBLY IS CONFORMALLY COATED.

IT SHOULD BE NOTED THAT STEP-STRESS, LATENT DEFECT, ASSEMBLY, EQUIPMENT AND OTHER TESTING DESCRIBED ABOVE IS NOT A REQUIREMENT OF DOD-STD-1686.

D. EXAMPLES OF SOME TYPICAL DAMAGE PATH IN MICROCIRCUITS (REFERENCE 34)

(1) FAILURE OF A TRANSISTOR-TRANSISTOR LOGIC (TTL) DEVICE

THIS FAILURE WAS DUE TO A RESISTIVE FILAMENT ACROSS THE EMITTER-BASE JUNCTION OF THE MULTIPLE EMITTER TRANSISTOR. THE DASHED LINE IN FIGURE 10.5 SHOWS THE LOCATION OF THIS FILAMENT. THE ESD FAILURE RESULTED IN HIGH STATE LEAKAGE CURRENT BEYOND SPECIFICATION. THE FAILURE PATH AND POLARITY SHOWN IN THE FIGURE INDICATE THAT THE EMITTER-BASE JUNCTION OF THE INPUT TRANSISTOR WAS REVERSE BIASED. IT WAS THIS JUNCTION THAT FAILED.

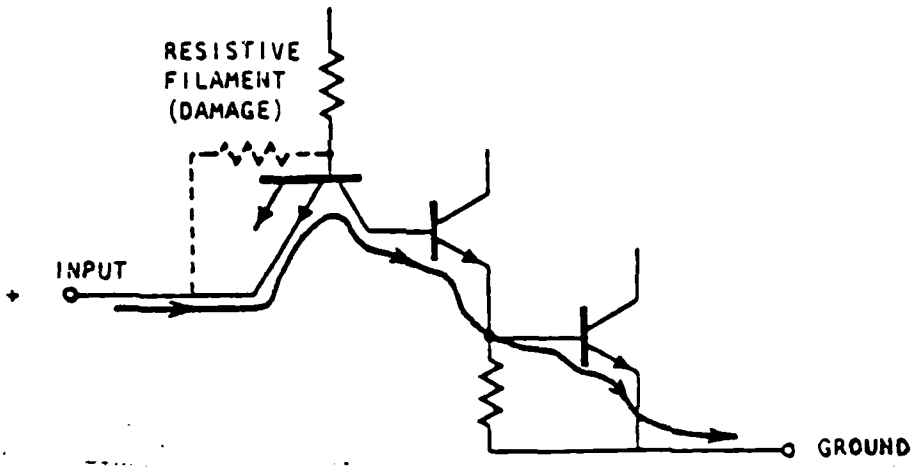


FIGURE 10.5: DAMAGE PATH IN TTL INPUT FAILURE

(2) FAILURE OF LOW POWER SCHOTTKY TTL NAND GATE

THE 54LS00 FAILURES ARE SIMILAR TO THOSE IN THE TTL STRUCTURE EXCEPT THAT A RESISTIVE FILAMENT IS FORMED NOT ONLY ACROSS THE INPUT DIODE, BUT ALSO ACROSS THE INPUT CLAMP DIODE AS SHOWN IN FIGURE 10.6. THE INPUT LEAKAGE CURRENT IS NOTED TO BE HIGHER THAN SPECIFICATION LIMITS.

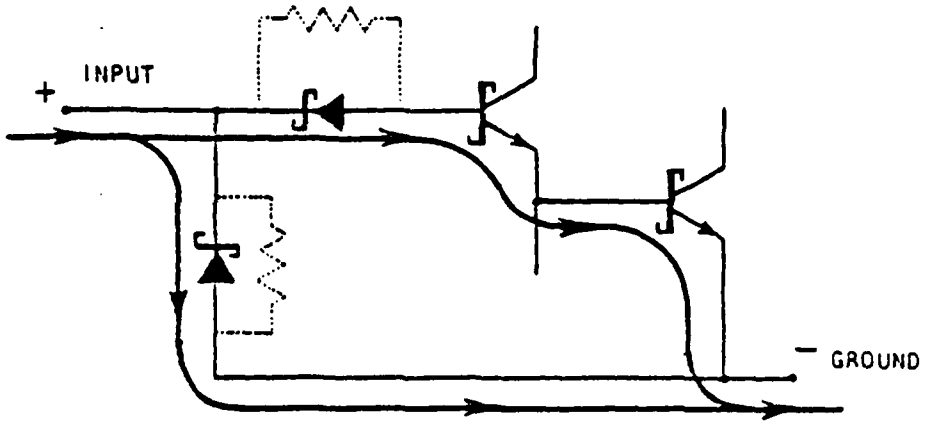


FIGURE 10.6: DAMAGE PATHS FOR 54LS00 (LOW POWER SCHOTTKY TTL NAND GATES)

(3) FAILURE OF INTEGRATED INJECTION LOGIC (I^2L) DEVICE

ANOTHER ILLUSTRATION OF THE FAILURE DUE TO A RESISTIVE FILAMENT ACROSS THE BASE-EMITTER JUNCTION OF THE OUTPUT INVERTER TRANSISTOR OF XC401 I^2L GATE IS SHOWN IN FIGURE 10.7.

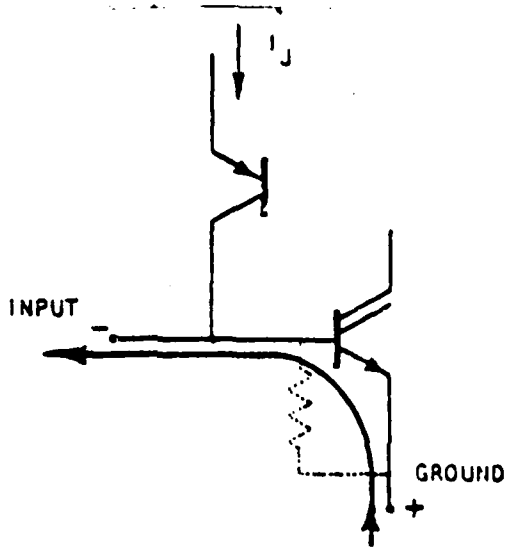


FIGURE 10.7: DAMAGE PATH IN I^2L GATE

(4) OXIDE BREAKDOWN OF A MOS STRUCTURE

FIGURE 10.8 ILLUSTRATES THE THIN OXIDE BREAKDOWN OF A MOS STRUCTURE.

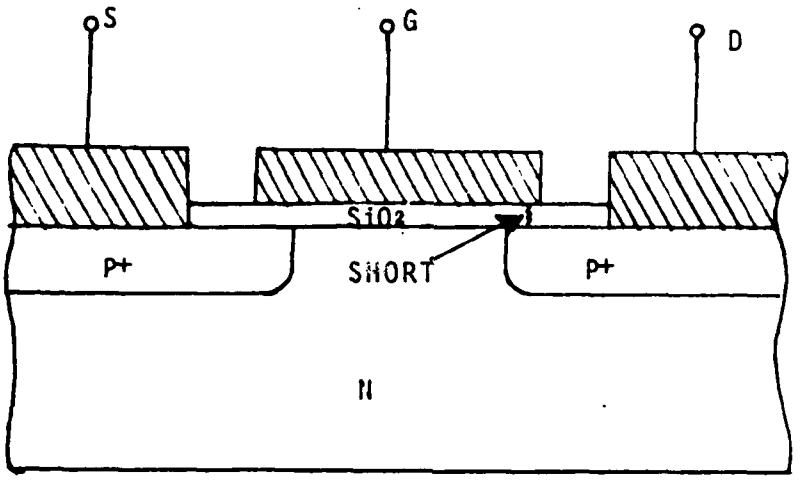


FIGURE 10.8: OXIDE BREAKDOWN IN A MOS STRUCTURE

E. COMMENTS ON EMP TESTING AND CONVERSION OF EMP DATA TO ESD

A LARGE QUANTITY OF FAILURE THRESHOLD DATA FOR MICROCIRCUITS HAS BEEN GENERATED USING RECTANGULAR HIGH VOLTAGE PULSES OF VARIOUS PULSE WIDTHS (REFERENCE 34). TO USE THESE DATA, A RELATION BETWEEN SQUARE PULSE DAMAGE AND EXPONENTIAL PULSE DAMAGE IN TERMS OF TIME AND AMPLITUDE IS PRESENTED (REFERENCE 35). THE DIRECT POINTS OF COMPARISON OF EMP AND ESD TEST ARE:

- THE PHYSICAL DAMAGE MECHANISMS FOR ESD AND EMP ARE BASICALLY THE SAME.
- BOTH ARE PULSE TESTS.
- BOTH TYPES OF TEST INDICATE BOTH ENERGY DEPENDENT AND VOLTAGE STRESS DAMAGE MECHANISMS.

THE PRINCIPLE DIFFERENCES ARE:

- VOLTAGE SOURCE WAVE FORM AND THE COUPLING MECHANISM TO THE SENSITIVE COMPONENT ARE DIFFERENT FOR EMP AND ESD.

(1) EMP TO ESD V-ZAP DATA CONVERSION

WUNSCH AND BELL'S MODEL (REFERENCE 36) CAN BE USED TO DETERMINE THE THRESHOLD FAILURE LEVEL OF DIODES AND TRANSISTORS DUE TO PULSED VOLTAGES. THIS MODEL RELATES THE POWER DISSIPATED PER UNIT AREA TO THE THERMAL CHARACTERISTICS OF THE SEMICONDUCTOR TO DETERMINE THE LOCAL TEMPERATURE RISE AND THE THRESHOLD POWER DENSITY FOR FAILURE. FAILURE IS ASSUMED TO OCCUR WHEN THE TEMPERATURE REACHES THE MELTING POINT OF THE SEMICONDUCTOR MATERIAL. LINEAR HEAT FLOW THEORY IS USED TO DERIVE THE FOLLOWING EQUATION:

$$P/A = \sqrt{\pi \kappa \rho C_p}\ [T_m - T_i]\ t^{-\frac{1}{2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ (38)$$

WHERE:

P = PULSE POWER DISSIPATED IN THE DEVICE

A = JUNCTION AREA

κ = THERMAL CONDUCTIVITY OF JUNCTION MATERIAL, WATTS/CM-^{o}K

ρ = DENSITY OF JUNCTION MATERIAL, GM/CM^3

C_p = SPECIFIC HEAT OF JUNCTION MATERIAL, JOULES/CM-^{o}K

T_m = FINAL JUNCTION TEMPERATURE = MELTING POINT TEMPERATURE OF MATERIAL FOR FAILURE, ^{o}K

T_i = INITIAL JUNCTION TEMPERATURE, ^{o}K

t = RECTANGULAR PULSE DURATION

FOR "t" IN MICROSECONDS, "P/A" IS GIVEN IN KILOWATTS/CM^2. THIS EQUATION WITH "$t^{-\frac{1}{2}}$" DEPENDENCE IS ACCURATE FOR PULSE WIDTHS IN THE RANGE OF .1 μS

TO 10 μS. FOR SHORTER PULSE WIDTHS THE HIGH CURRENTS REQUIRED FOR FAILURE CAUSES MORE VOLTAGE DROP, AND CONSEQUENTLY MORE ENERGY DISSIPATION IN THE BULK MATERIAL, RESULTING IN A PULSE DURATION DEPENDENCE OF "t^{-1}". FOR LONGER PULSES THE POWER REQUIRED FOR FAILURE APPROACHES THE CONTINUOUS POWER DISSIPATION OF THE PART WHICH IS EQUIVALENT TO A "t" DEPENDENCE. THEREFORE THE ENERGY (E) DISSIPATED AT THE JUNCTION IS PROPORTIONAL TO A POWER OF THE RECTANGULAR PULSE DURATION (t), WHICH IS DEPENDENT UPON THE LENGTH OF THE PULSE DURATION. THAT IS:

FOR $t < .1\ \mu s$	$E \alpha t^{-1}$
$.1\ \mu s \leq t \leq 10\ \mu s$	$E \alpha t^{-\frac{1}{2}}$
$t > 10\ \mu s$	$E \alpha t$

THE EMP DAMAGE DATA COULD BE OBTAINED EMPIRICALLY OR ANALYTICALLY BY USING THE WUNSCH/BELL THEORETICAL MODEL. WHEN OBTAINED ANALYTICALLY THE DATA ARE GENERALLY EXPRESSED IN TERMS OF THE AVERAGE POWER PER UNIT AREA. WHEN OBTAINED EMPIRICALLY THE POWER FOR FAILURE IS USUALLY GIVEN AND IS COMPUTED BY MEASURING THE VOLTAGE ACROSS AND THE CURRENT THROUGH THE JUNCTION.

IN PRACTICE EMP DAMAGE DATA ARE CALCULATED USING THE FOLLOWING EQUATION:

$$P = k\, t^{-\frac{1}{2}} \qquad (39)$$

WHERE:

k IS THE WUNSCH DAMAGE CONSTANT $(kw)(SEC)^{\frac{1}{2}}$

THE CONSTANT k IS USUALLY OBTAINED EMPIRICALLY USING SQUARE PULSES OF 1 μS DURATION.

(2) USE OF EMP DATA TO ESD THRESHOLD ESTIMATES

SINCE SEMICONDUCTOR JUNCTION FAILURE AND THERMAL TYPE FAILURES OF MANY OTHER COMPONENTS IS ENERGY DEPENDENT, THE EMP DAMAGE CONSTANT, CONTINUOUS DISSIPATION RATING AND SHORT PULSE DATA ARE ALL APPLICABLE TO THE ESD PROBLEM. THERE ARE OF COURSE PRECAUTIONS IN THE USE OF THE EMP DATA. FOR SHORT PULSE WIDTHS THE FAILURE OF A SEMICONDUCTOR JUNCTION IS VOLTAGE DEPENDENT, NOT ENERGY. SINCE THE WUNSCH DAMAGE CONSTANT IS OBTAINED AT A PULSE WIDTH OF ONE MICROSECOND IT DOES NOT PROVIDE SHORT PULSE FAILURE INFORMATION, THAT IS, DIELECTRIC BREAKDOWN DATA. THE "k" VALUE IS FOR THE REVERSE BREAKDOWN OF THE B-E JUNCTION, UNLESS OTHERWISE SPECIFIED. IT IS TO BE STATED THAT THE DIELECTRIC BREAKDOWN VOLTAGE LEVEL IS ALSO A FUNCTION OF THE RATE OF THE RISE OF THE PULSE, BEING LOWER FOR FASTER RATES OF RISE.

TO USE THE EMP ENERGY DATA, THE ENERGY IN THE SQUARE PULSE SHOULD BE EQUATED TO THE ENERGY IN THE TIME DURATION OF $t = o$ TO $t = 5\tau$ OF THE CAPACITOR DISCHARGE PULSE USED FOR MOST ESD STUDIES. THE VALUE OF 5τ SHOULD BE IN THE RANGE OF 0.1 μS TO 10 μS FOR THE MOST ACCURATE RESULTS SINCE THIS IS THE RANGE WHERE THE $\tau^{-\frac{1}{2}}$ DEPENDENCE HOLDS. BELOW "5τ = 0.01 μS", USE OF THE EMP DATA IS HIGHLY QUESTIONABLE UNLESS THE VOLTAGE FAILURE SENSITIVITY OF THE PART IS KNOWN. THE METHOD TO CALCULATE THE THRESHOLD VOLTAGE FOR FAILURE IS DESCRIBED BELOW:

(a) CALCULATE THE TIME CONSTANT, "τ", THROUGH THE USE OF THE PROPER EQUIVALENT CIRCUIT. MULTIPLY IT BY "5" TO INCLUDE 99% OF THE ENERGY IN THE PULSE, AND USE WITH THE EMP DAMAGE CONSTANT OR POWER VERSUS PULSE DURATION PLOTS.

(b) USE THE DAMAGE CONSTANT (k) AND EQUATION (39) WITH "$t = 5\tau$" TO OBTAIN THE AVERAGE POWER FOR FAILURE (P_{AV}); (FOR ENERGY MULTIPLY BY t).

(c) CALCULATE THE PEAK CURRENT USING EQUATION (41).

(d) CALCULATE THE ELECTROSTATIC VOLTAGE THAT WILL PRODUCE THIS CURRENT FROM THE EQUIVALENT CIRCUIT. THE PART CHARACTERISTICS WHICH MUST BE KNOWN FOR CONVERSION ARE:

((1)) THE REVERSE BREAKDOWN VOLTAGE OF THE EMITTER-BASE JUNCTION.

((2)) THE CROSS SECTIONAL AREA OF THE CURRENT PATH NEAR THE EMITTER BASE JUNCTION.

((3)) THE INTERNAL RESISTANCE OF THE SILICON NEAR THE EMITTER-BASE JUNCTION. THIS PROVIDES THE "R_J" PARAMETER OF THE EQUIVALENT CIRCUIT.

IN A V-ZAP TEST THE VOLTAGE SOURCE IS A CHARGED CAPACITOR REPRESENTING HUMAN CAPACITANCE (C_H) AND THE DISCHARGE CIRCUIT CONSISTS OF RESISTANCES (R_C), (R_J) AND (R_C1) REPRESENTING THE CONTACT RESISTANCE BETWEEN THE SOURCE AND THE PART UNDER TEST, THE EQUIVALENT JUNCTION RESISTANCE OF THE PART, AND THE OTHER RESISTANCES OF THE PART LEAD TO GROUND, RESPECTIVELY (FIGURE 10.9). THUS THE DISCHARGE CURRENT IS GIVEN BY:

$$i = I_p e^{-t/\tau} \quad \text{.......} \quad (40)$$

WHERE:

$$I_p = \frac{V_A - V_{BD}}{R_C + R_J + R_C1} \quad \text{.......} \quad (41)$$

τ = CIRCUIT TIME CONSTANT

$\tau = (R_C + R_J + R_C1)\ C_H$

V_{BD} = PART BREAKDOWN VOLTAGE

V_A = APPLIED VOLTAGE ACROSS C_H

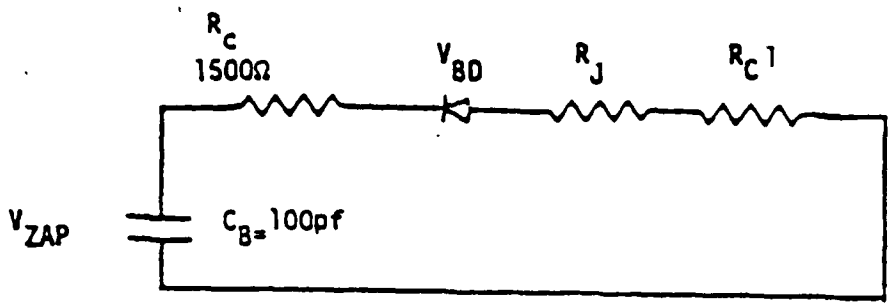


FIGURE 10.9: V-ZAP MODEL

THE POWER DISSIPATED AT THE JUNCTION IS GIVEN BY:

$$P(t) = V_{BD} + R_J i^2 \quad \ldots\ldots (42)$$

THE AVERAGE POWER FOR"5"TIME CONSTANTS (99% OF TOTAL POWER) IS GIVEN BY:

$$P_{AV} = \frac{1}{5\tau} \int_0^{5\tau} V_{BD}\, I_p e^{-t/\tau}\, dt + \frac{1}{5\tau} \int_0^{5\tau} R_J I_p^2 e^{-2t/\tau}\, dt \quad \ldots\ldots (43)$$

$$= \frac{V_{BD}\, I_p}{5} (1-e^{-5}) + \frac{R_J\, I_p^2}{10} (1-e^{-10})$$

$$= \frac{V_{BD}\, I_p}{5} + \frac{R_J\, I_p^2}{10} \quad \ldots\ldots (44)$$

THE ENERGY CAN BE OBTAINED FROM:

$$E = P_{AV}\, t_D \quad \ldots\ldots (45)$$

WHERE:

t_D IS THE PULSE WIDTH

FOR AN EXPONENTIAL PULSE $t_D = 5\tau$ AND THEREFORE

$$E = 5\, P_{AV}\tau$$

CALCULATIONS FOR THE EVALUATION OF ESD THRESHOLD CAN BE DONE USING AN EXAMPLE.

EXAMPLE (K): ASSUME THE ELECTROSTATIC CHARGE IS ON THE BODY OF A PERSON AND IS DISCHARGED THROUGH THE E-B JUNCTION OF THE PART CONSIDERED AS THE MOST SENSITIVE PATH. ASSUME THE FOLLOWING EQUIVALENT CIRCUIT ELEMENTS:

$R_J = 25\Omega$

$C_H = 100$ PF

$R_C = 1500\Omega$

$R_C1 = 10\Omega$

$V_{BD} = 4V$

k (IN EQUATION (39)) FROM EMP DATA BANK* = 1.0×10^{-2} $(kw)(SEC)^{\frac{1}{2}}$

V_{BD} (BREAKDOWN VOLTAGE THROUGH THE E-B JUNCTION) FROM EMP DATA BANK* = 4.0V

$$\tau = (R_C + R_J + R_C1)\, C_H$$

$$= (1500\,\Omega + 25\,\Omega + 10\,\Omega) \times 100 \times 10^{-12} \text{ (FARADS)}$$

*THESE DATA ARE AVAILABLE IN THE SUPERSAP II DATA BANK MAINTAINED BY THE AIR FORCE WEAPONS LABORATORY.

$= 1.535 \times 10^{-7}$ SEC

$5\tau = 7.675 \times 10^{-7}$ SEC

$= .7675\ \mu$SEC

THE VALUE OF 5τ IS IN THE RANGE OF 0.1 μSEC TO 10 μSEC FOR WHICH THE $kt^{-\frac{1}{2}}$ DEPENDENCE HOLDS.

5τ IS USED TO INCLUDE 99% OF THE ENERGY OF THE PULSE.

$$P_{AV} = kt^{-\frac{1}{2}} \text{ (KILOWATTS)}$$

$$= (1.0 \times 10^{-2})(.7672)^{-\frac{1}{2}} \text{ (KILOWATTS)}$$

$= 11.4$ WATTS

$$I_p = \frac{-2V_{BD} \pm \sqrt{4\ V_{BD}^2 + 40\ R_J\ P_{AV}}}{2R_J}$$

$$= \frac{-2\ (4) \pm \sqrt{4(4)^2 + 40\ (25)\ (11.4)}}{2\ (25)}$$

$= 1.98$ AMPS

THE THRESHOLD ESD VOLTAGE THEREFORE IS CALCULATED AS:

$$V = I_p\ (R_C + R_J + R_C1) + V_{BD}$$

$= 1.98\ (1500 + 25 + 10) + 4.0$

$= 3043$ VOLTS

(3) SOURCES OF ERROR

THERE ARE TWO PRIMARY SOURCES OF ERROR IN CONVERTING EMP DATA TO ESD DATA:

(a) UNCERTAINTY IN THE VALUE OF THE EMP DAMAGE CONSTANT.

(b) UNCERTAINTY IN THE INTERNAL CONSTANTS OF THE PART BEING CONSIDERED.

THE EXACT VALUE OF THE EMP DAMAGE CONSTANT IS UNCERTAIN SINCE THERE IS A NORMAL VARIATION IN PART GEOMETRY FROM LOT TO LOT AND MANUFACTURER TO MANUFACTURER. NORMAL PRODUCTION VARIATION (LOT TO LOT, MANUFACTURER TO MANUFACTURER) IS OFTEN ON THE ORDER OF A FACTOR OF TEN. MOREOVER, MANUFACTURERS CHANGE PART GEOMETRY IN RESPONSE TO THE THRUST OF THE MARKET PLACE THAT PREFER SMALLER AND SMALLER GEOMETRY PARTS BECAUSE THEY ARE LESS EXPENSIVE. THIS RESULTS IN A LOWERING OF THE V-ZAP VOLTAGES THESE PARTS CAN WITHSTAND.

THE OTHER MAJOR SOURCE OF UNCERTAINTY IS LACK OF DATA ON THE INTERNAL CONSTRUCTION OF THE PART. DUE TO THE RELATIVE HIGH OUTPUT IMPEDANCE (1500Ω) OF THE STATIC DISCHARGE MODEL WITH RESPECT TO THE R_J OF THE SEMICONDUCTOR JUNCTION, R_J PLAYS A MAJOR ROLE IN THE DETERMINATION OF HOW MUCH ENERGY REACHES THE JUNCTION. IT SHOULD BE NOTED THAT THE EFFECT OF SMALLER GEOMETRIES GENERALLY INCREASES R_J. ANY OTHER SERIES RESISTANCE IN THE DISCHARGE PATH ALSO LENDS SOME UNKNOWN TO THE PROBLEM DEPENDING UPON ITS MAGNITUDE. IF SUCH A RESISTANCE IS SMALL COMPARED WITH 1500Ω IT WILL HAVE RELATIVELY LITTLE EFFECT, BUT IF IT IS OF THE SAME MAGNITUDE OR GREATER IT WILL TEND TO LIMIT THE AMOUNT OF ENERGY REACHING THE JUNCTION, SINCE THE TOLERANCE ON THESE RESISTORS WHEN USED IS GENERALLY $\pm$20% THIS RESISTANCE CAN HAVE A SIGNIFICANT EFFECT ON THE V-ZAP VOLTAGE REQUIRED TO DAMAGE A PART.

THERE ARE TWO GENERAL APPROACHES TO SOLVE THIS PROBLEM: EITHER OBTAIN ESD DATA DIRECTLY OR DERATE THE DATA AVAILABLE FROM EMP DAMAGE DATA. OBTAINING THE ESD DATA DIRECTLY HAS MANY OBVIOUS ADVANTAGES AND DISADVANTAGES BUT IT DOES NOT DIRECTLY ADDRESS THE PROBLEM OF PART VARIABILITY. DERATING THE CONVERSIONS BY DIVIDING THE V-ZAP VOLTAGE BY A CONSTANT HAS THE ADVANTAGE OF BEING SIMPLE, BUT CAN REQUIRE OVER-PROTECTING A PART OR CIRCUIT BOARD. AT THE PRESENT TIME, HOWEVER, THE LATTER PROCEDURE IS PROBABLY THE BEST APPROACH.

(4) LIMITATIONS OF EMP TO ESD CONVERSION

FOR SHORT PULSE WIDTHS THE FAILURE OF A SEMICONDUCTOR JUNCTION IS VOLTAGE DEPENDENT, NOT ENERGY DEPENDENT. SINCE THE WUNSCH DAMAGE CONSTANT"k"IS OBTAINED AT A PULSE WIDTH OF 1 μSEC IT DOES NOT PROVIDE SHORTER PULSE FAILURE INFORMATION, I.E., DIELECTRIC BREAKDOWN DATA. MANY HIGHLY SUSCEPTIBLE ESDS PARTS (E.G., MOS) ARE VOLTAGE SENSITIVE, TYPICALLY EXHIBITING THE DIELECTRIC BREAKDOWN FAILURE MECHANISM THROUGH THE OXIDE LAYER UNDER THE GATE. AT THE LONGER PULSE WIDTHS, BREAKDOWN DUE TO THERMAL ENERGY HEATING OF THE JUNCTION WOULD BE EXPECTED FOR BOTH ESD AND EMP TESTS. HENCE, A SIMPLE PULSE EMP TEST COULD BE ADEQUATE TO A CERTAIN EXTENT FOR ESTIMATING ESD SENSITIVITY LEVELS OF POWER SENSITIVE ESDS PARTS.

F. ESD PROTECTIVE CIRCUITRY

(1) DESIGN OF THE PROTECTION NETWORK

THE PURPOSE OF THE PROTECTION CIRCUITRY IS TO PREVENT DESTRUCTION OR DEGRADATION OF THE ELECTRICAL CHARACTERISTICS OF THE PART. TO ACCOMPLISH THIS THE PROTECTION CIRCUITRY SHOULD BE ABLE TO WITHSTAND A SPECIFIED ELECTROSTATIC VOLTAGE LEVEL IN ADDITION TO BEING ABLE TO ABSORB A GIVEN AMOUNT OF ENERGY. ANOTHER CONSTRAINT IS THAT THE DELAY THROUGH THE

PROTECTION CIRCUITRY MUST BE SMALL FOR HIGH PERFORMANCE PARTS. THE DESIGN CRITERIA FOR PROTECTIVE CIRCUITRY, THEREFORE, INVOLVES INITIAL RESPONSE TIME, SUBSEQUENT RE-STRESSING, MAXIMUM SUSTAINABLE VOLTAGE, TOTAL ENERGY DISSIPATION, AND EFFECTS ON PERFORMANCE.

EXAMPLE (L): IF THE INPUT CAPACITANCE OF A TYPICAL IC IS TAKEN TO BE ABOUT 5 PF, THEN LITTLE VOLTAGE IS LOST BY THE 100 PF HUMAN SOURCE IN CHARGING UP THE IC TO ITS VOLTAGE. ASSUMING A HUMAN SERIES RESISTANCE OF 1.5 KILOOHM, THE PROTECTIVE CIRCUIT MUST THEN REACT IN:

$$t = RC = (5 \times 10^{-12}) \times (1.5 \times 10^{3}) = 7.5 \times 10^{-9} \text{ SEC}$$

HENCE THE PROTECTION SCHEME MUST BE FAST.

SINCE A TYPICAL STATIC ELECTRIC DISCHARGE CAN TAKE THE FORM OF A SERIES OF RAPIDLY RECURRING PULSES DUE TO A FORM OF HUMAN CONTACT BOUNCE, THIS PROBLEM MUST ALSO BE CONSIDERED IN DESIGNING EFFECTIVE PROTECTIVE CIRCUITRY.

ONCE CONTACT BOUNCE HAS STOPPED, THE PROTECTION NETWORK MUST THEN BE ABLE TO WITHSTAND THE CONTINUED DISCHARGE OF THE HUMAN THROUGH SUBSTRATE OR POWER SUPPLY PINS. USING 100 PF, CHARGED TO 15 KILOVOLTS THE ENERGY REMOVED WOULD BE ON THE ORDER OF:

$$(1/2)\ CV^2 = 1/2\ (100 \times 10^{-12})\ (15 \times 10^{3})^2 = 11.25 \times 10^{-4} \text{ JOULES}$$

OF EQUAL IMPORTANCE IN THE DESIGN OF AN EFFECTIVE GATE-PROTECTION SCHEME IN THE PROTECTION REQUIREMENTS DISCUSSED ABOVE ARE THE MECHANISMS BY WHICH FAILURE OCCURS. FAILURE MODE OF PROTECTIVE CIRCUITRY COULD OR COULD NOT RESULT IN AFFECTING THE PERFORMANCE PARAMETERS OF THE

PART OR CIRCUIT. SOME PROTECTIVE CIRCUITRY CAN FAIL WITHOUT ANY APPARENT FAILURE INDICATOR. THIS CAN RESULT IN AN UNPROTECTED PART THAT CAN BE DAMAGED BY A SUBSEQUENT ESD.

DESIGN OF A PROTECTION NETWORK SHOULD CONSIDER THE ALREADY PRESENT PROCESSING STEPS. SINCE THE CHOICE OF PROCESSING TECHNOLOGY (CMOS, PMOS, NMOS, SiGATE, ETC.) IS BASED ON CIRCUITRY PERFORMANCE REQUIREMENTS, PROTECTIVE SCHEMES SHOULD BE AVAILABLE AS PART OF EACH PROCESS. FOR EXAMPLE, THE USE OF LOW SUBSTRATE RESISTIVITY MATERIAL USING EPITAXIAL PROCESSING CAN SIGNIFICANTLY IMPROVE CURRENT CARRYING CAPABILITY OF ANY PROTECTIVE SCHEME. IN ADDITION, CIRCUIT SPEED OR SIZE REQUIREMENTS COULD RESTRICT USAGE OF CERTAIN NETWORKS, FORCING CUSTOM MODIFICATIONS OF PROTECTION CIRCUITRY WHERE NECESSARY. IN GENERAL, ANY PROTECTIVE CIRCUITRY USED SHOULD BE FABRICATED UTILIZING EXISTING TECHNOLOGY, SHOULD BE OF MINIMAL SIZE, AND SHOULD NOT ADVERSELY AFFECT CIRCUIT PERFORMANCE.

TO PROTECT PARTS WITH ENERGY SENSITIVE P-N JUNCTIONS IT IS DESIRABLE TO USE DESIGNS THAT REDUCE ENERGY DENSITY. THE WAY TO REDUCE ENERGY DENSITIES SUCH AS INCREASED JUNCTION AREA ARE USUALLY IN DIRECT CONFLICT WITH DESIRED ELECTRICAL PERFORMANCE. OPERATIONAL AMPLIFIER MICROCIRCUITS THAT EMPLOY MOS CAPACITORS FOR BANDWIDTH CONTROL CAN BE DESIGN HARDENED WITH P-N JUNCTION ELEMENTS THAT CLAMP VOLTAGES BELOW THE CAPACITOR BREAKDOWN VOLTAGE. HOWEVER, THE P-N JUNCTION ELEMENT ADDS ADDITIONAL CAPACITANCE EFFECTS WHICH CAN ALTER THE FREQUENCY PERFORMANCE OF THE PART.

ADVANCES IN HIGHER DENSITY CIRCUITRY TECHNOLOGY ARE TOWARD SMALLER GEOMETRIES, LOWER LEAKAGE, HIGHER IMPEDANCE, LOWER POWER DISSIPATION, AND HIGHER FREQUENCY. THE ESD ENVIRONMENT MUST BE RECOGNIZED AS A DESIGN CONSTRAINT TO THESE ADVANCES. EACH TECHNOLOGY OR PROCESS SHOULD BE EXAMINED BY THE PART DESIGNER TO IDENTIFY STRUCTURES THAT MAXIMIZE ESD

HARDENING WHILE MINIMIZING THE COMPROMISE IN ELECTRICAL PERFORMANCE. TABLE X-C IS AN EXAMPLE OF A STUDY WHERE AS MANY AS SEVEN MOS/LSI PROTECTIVE STRUCTURES WERE COMPARED. IT WAS CONCLUDED FROM THIS STUDY THAT A DIFFUSED SERIES RESISTOR WITH A FLOATING GATE DIODE FOLLOWED BY A SECOND RESISTOR: (A) CAN PROVIDE BETTER PROTECTION THAN A THIN-OXIDE LATERAL N-P-N; (B) HAS A LEAKAGE LESS SENSITIVE TO SURFACE INVERSION; AND (C) OCCUPIES MINIMUM AREA. ALL THESE FACTORS TEND TOWARDS AN OPTIMUM PROTECTIVE SCHEME.

(2) ESD DESIGN HARDENING GUIDELINES

ESD PART DESIGN HARDENING GUIDELINES ARE AS FOLLOWS:

(a) MOS PROTECTION CIRCUITRY IMPROVEMENT TECHNIQUES ARE: INCREASING DIODE SIZE; USING DIODES OF BOTH POLARITIES; ADDING SERIES RESISTORS; AND UTILIZING A DISTRIBUTED NETWORK EFFECT.

(b) AVOID CROSS-UNDERS BENEATH METAL LEADS CONNECTED TO EXTERNAL PINS. ALSO, SINCE CROSS-UNDERS ARE DIFFUSED DURING THE N+ (EMITTER) DIFFUSION PROCESS (RELATIVELY LATE IN THE PART FABRICATION), THE OXIDE OVER THE DIFFUSION WILL BE THINNER, CAUSING THIS AREA TO HAVE A LOWER DIELECTRIC BREAKDOWN. DEEP"N"DIFFUSIONS, RATHER THAN"N+"DIFFUSIONS, SHOULD BE USED FOR CROSS-UNDERS, IF A DEEP"N+"DIFFUSION STEP IS USED IN THE FABRICATION PROCESS.

(c) AVOID PARASITIC MOS CAPACITORS WHENEVER POSSIBLE. MICROCIRCUITS WITH METALLIZATION CROSSING OVER LOW RESISTANCE ACTIVE REGIONS (I.E., V_{CC} OVER N+ ISOLATED DIFFUSIONS) ARE MODERATELY SENSITIVE TO ESD. SUCH CONSTRUCTION INCLUDE MICROCIRCUITS WITH METALLIZATION PATHS OVER"N+" GUARD RINGS. "N+"GUARD RINGS ARE USED IN THE N-TYPE SEMICONDUCTOR TO P-TYPE SEMICONDUCTOR AND TO REDUCE THE LEAKAGE CURRENT THROUGH THE PART. SINCE THE FINAL OXIDE LAYER OVER THE"N+"GUARD RING IS RELATIVELY THIN, PARASITIC

TABLE X-C

COMPARISON OF MOS/LSI PROTECTIVE STRUCTURES

NO.	STRUCTURE	AREA (M^2)	DESTRUCTION VOLTAGE (V)	VOLTAGE CLAMPING	STRENGTH	INPUT LEAKAGE & LOW CAPAC.
1	LATERAL N-P-N WITH GATED THIN OXIDE	8129	1100	EXCELLENT	POOR	POOR
2	LATERAL N-P-N WITH GATED THIN OXIDE AND RESISTOR	9999	2300	EXCELLENT (NOTE 2)	IMPROVED OVER CASE 1	POOR
3	LATERAL N-P-N WITH GATED THICK OXIDE	8129	5500	POOR (NOTE 1)	EXCELLENT	POOR
4	FLOATING GATE DIODE	3870	800	POOREST	POOR	GOOD
5	DIFFUSED SERIES RESISTOR WITH FLOATING GATE DIODE	6451	1400	IMPROVED OVER CASE 4	IMPROVED OVER CASE 4	GOOD
6	DIFFUSED SERIES RESISTOR, FLOATING GATE DIODE, SERIES UNDERPASS RESISTOR	6645	2400	IMPROVED OVER CASE 5 (NOTE 2)	IMPROVED OVER CASE 5	GOOD
7	DIFFUSED SERIES RESISTOR, FLOATING GATE DIODE, SERIES UNDERPASS RESISTOR	8451	3400	IMPROVED OVER CASE 5	IMPROVED OVER CASE 5	GOOD

NOTE 1: THIS DEVICE CLAMPS AT 50V WHICH IS THE BREAKDOWN VOLTAGE OF GATE OXIDE TO BE PROTECTED. HOWEVER, THE TRANSIENT RESPONSE OF THE SUBSTRATE UNDERNEATH THESE GATES WHEN DRAIN AND SOURCE ARE FLOATING WILL ACT TO DROP A SUBSTANTIAL FRACTION OF THE APPLIED VOLTAGE (IN THE CORRECT POLARITY), THUS RELIEVING THE OXIDE FROM THE FULL MAGNITUDE OF THE VOLTAGE STRESS.

NOTE 2: SERIES RESISTANCE EXPONENTIALLY ATTENUATES THE OVERVOLTAGE.

MOS CAPACITORS OF RELATIVELY LOW BREAKDOWN VOLTAGE ARE CREATED WHEN A METALLIZATION PATH PASSES OVER THIS RING. THESE MOS CAPACITOR STRUCTURES ARE HIGHLY TO MODERATELY SENSITIVE TO ESD.

(d) AVOID MULTI-LEVEL METALLIZATION IN TERMINAL PATHS WHERE POSSIBLE. THESE LEVELS ARE TYPICALLY SEPARATED BY THIN DIELECTRIC LAYERS. MULTI-LEVEL METALLIZATION OFTEN IMPOSE A NUMBER OF METALLURGICAL REQUIREMENTS WHICH ARE FREQUENTLY INCOMPATIBLE. FOR EXAMPLE, ONCE THE FIRST METALLIZATION LAYER IS PLACED, THE CIRCUIT CANNOT BE SUBSEQUENTLY HEATED IN EXCESS OF 550^{o}C (EUTECTIC POINT OF Al-Si SYSTEM 575^{o}C). THUS, THE DIELECTRIC LAYER (SiO_2) MUST BE DEPOSITED BY A LOW TEMPERATURE PROCESS (E.G., PYROLYTIC DEPOSITION). THIS LAYER IS PRONE TO BREAKDOWN FROM ESD FOR TWO REASONS:

((1)) A LOW TEMPERATURE GROWTH OF SiO_2 GENERALLY IS NOT UNIFORM IN THICKNESS AND NOT FREE FROM PINHOLES.

((2)) THE DIELECTRIC LAYER IS THIN AND THUS THE BREAKDOWN VOLTAGE IS VERY LOW.

(e) MOS PROTECTION CIRCUITS SHOULD BE EXAMINED TO SEE IF THE LAYOUT PERMITS THE PROTECTION DIODES TO BE DEFECTIVE OR BLOW WITHOUT CAUSING THE CIRCUIT TO BE INOPERATIVE.

(f) DISTANCE BETWEEN ANY CONTACT EDGE AND THE JUNCTION SHOULD BE 70 MICRONS OR BETTER.

(g) LINEAR IC CAPACITORS SHOULD BE PARALLELED BY A PN JUNCTION WITH SUFFICIENTLY LOW BREAKDOWN VOLTAGE.

(h) FOR BIPOLAR PARTS AVOID DESIGNS PERMITTING A HIGH TRANSIENT ENERGY DENSITY TO EXIST IN A PN JUNCTION DEPLETION REGION DUE TO

AN ESD. USE SERIES RESISTANCE TO LIMIT ESD CURRENT OR USE PARALLEL ELEMENTS TO DIVERT CURRENT FROM CRITICAL ELEMENTS. THE ADDITION OF CLAMP DIODES BETWEEN A VULNERABLE LEAD AND ONE OR MORE POWER SUPPLY LEADS CAN IMPROVE RESISTANCE TO ESD BY KEEPING CRITICAL JUNCTIONS OUT OF REVERSE BREAKDOWN. IF A JUNCTION CANNOT BE KEPT OUT OF REVERSE BREAKDOWN, PHYSICALLY ENLARGING THE JUNCTION WILL MAKE IT MORE ESD RESISTANT BY REDUCING THE INITIAL TRANSIT ENERGY DENSITY IN INVERSE PROPORTION OF ITS AREA.

(i) THE PROTECTION OF A TRANSISTOR FROM ESD CAN BE IMPROVED BY INCREASING THE EMITTER PERIMETER ADJACENT TO THE BASE CONTACT. THIS LOWERS TRANSIENT ENERGY DENSITY IN THE CRITICAL EMITTER SIDEWALL. ENLARGING THE EMITTER DIFFUSION AREA ALSO HELPS IN SOME PULSE CONFIGURATIONS.

(j) AS AN ALTERNATIVE TO USING CLAMPING DIODES (WHICH CONSUMES CHIP AREA AND CAN CAUSE UNWANTED PARASITIC EFFECTS) A "PHANTOM EMITTER" TRANSISTOR CAN IMPROVE ESD RESISTANCE. THE PHANTOM TRANSISTOR INCORPORATES A SECOND EMITTER DIFFUSION SHORTED TO THE BASE CONTACT. THIS CREATES A DELIBERATE SEPARATION OF THE BASE CONTACT FROM THE NORMAL EMITTER WITHOUT INTERFERING WITH NORMAL TRANSISTOR OPERATION. THE SECOND EMITTER PROVIDES A LOWER BREAKDOWN PATH BV_{CEO} BETWEEN THE BURIED COLLECTOR AND THE BASE CONTACT.

(k) AVOID PIN LAYOUTS WHICH PUT THE CRITICAL ESD PATHS ON CORNER PINS.

(3) PROTECTION SCHEMES

VARIOUS INPUT PROTECTION NETWORKS HAVE BEEN DEVELOPED TO PROTECT MOS PARTS. THESE INPUT PROTECTION NETWORKS PROVIDE LIMITED PROTECTION AGAINST ESD. SOME OF THEM ARE DESCRIBED BELOW:

(a) RESISTOR PROTECTION

PERHAPS THE SIMPLEST OF ALL PROTECTIVE NETWORKS, YET THE BASIS OF EVEN THE MOST COMPLEX, IS THE INPUT RESISTOR USED TO LIMIT CURRENT FLOW TO THE ACTIVE CIRCUITRY. TO BE EFFECTIVE, IT MUST BE COMBINED WITH A SCHEME THAT WILL PREVENT THE GATE VOLTAGES FROM REACHING DESTRUCTIVE LEVELS. WHILE THE RESISTOR CAN BE SMALL IN AREA IT CAN ADVERSELY AFFECT THE CIRCUIT SPEEDS DUE TO THE INCREASE IN THE RC TIME CONSTANT.

(b) DIODE PROTECTION

THE NEXT SIMPLEST GATE PROTECTION SCHEME IS A P-N JUNCTION DIODE, WITH A REVERSE BREAKDOWN VOLTAGE SLIGHTLY LARGER THAN THE MAXIMUM GATE OPERATING POTENTIAL (FIGURE 10.10). DURING NORMAL OPERATION THE DIODE IS REVERSE BIASED; ITS ONLY EFFECTS ARE AN INCREASE IN THE INPUT CAPACITANCE AND THE LEAKAGE CURRENT. IN MOST APPLICATIONS, THESE EFFECTS ARE NEGLIGIBLE. WHEN VOLTAGES OUTSIDE THE NORMAL OPERATING RANGE ARE APPLIED TO THE GATE, THE PROTECTION DIODE IS EITHER FORWARD BIASED OR IT BREAKS DOWN IN THE REVERSE DIRECTION. IN EITHER CASE THE GATE VOLTAGE IS KEPT BELOW 80V. THUS DIODES COMBINE THE ADVANTAGES OF SMALL SIZE WITH MINIMAL INCREASE IN DELAY TIME. WHEN USED ALONE, HOWEVER, IT CAN EASILY BE DESTROYED BY EXCESSIVE CURRENTS.

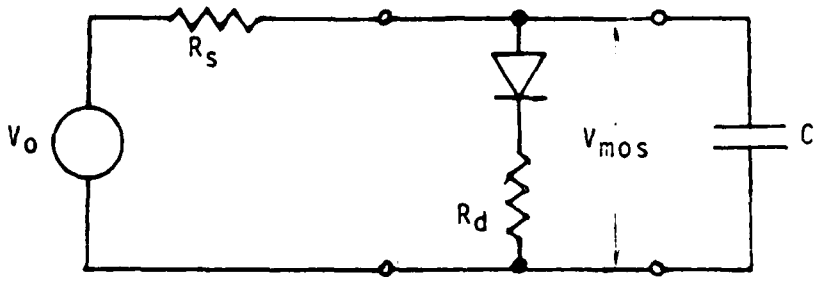


FIGURE 10.10: GATE PROTECTION USING DIODE

(c) RESISTOR/DIODE COMBINATION

BY COMBINING THE PREVIOUS TWO SCHEMES (I.E., RESISTORS AND DIODES), A MUCH MORE EFFECTIVE AND DURABLE PROTECTION NETWORK IS OBTAINED. THE RESISTOR IS USED TO LIMIT CURRENT FLOW TO THE DIODE, AND THE DIODE REVERSE BREAKDOWN VOLTAGE PROTECTS THE GATE OXIDE FROM DESTRUCTION DUE TO OVERVOLTAGE. THE VALUE OF THE INPUT RESISTOR USED DEPENDS ON THE BREAKDOWN IMPEDANCE OF THE DIODE.

EXAMPLE (M): IF A PROTECTIVE NETWORK IS TO PROVIDE PROTECTION TO 5 KV, THE DIODE HAS A RESISTANCE TO SUBSTRATE (R_{sub}) OF 25 OHMS UNDER THESE CONDITIONS, AND THE BREAKDOWN VOLTAGE (V_{bd}) ACROSS THE DIODE IS TO BE LIMITED TO 50 VOLTS, THEN THE VALUE OF THE INPUT RESISTOR (R_{in}) CAN BE FOUND BY VOLTAGE DIVISION:

$$R_{in} = (V_{prot.} - V_{bd}) \times R_{sub}/V_{bd}$$

$$= (5000 - 50) \times (25)/50 = 2.5 \times 10^3 \text{ OHMS}$$

SPEED AND AREA REQUIREMENTS FOR THIS NETWORK ARE MODERATE, MAKING IT A DESIRABLE, ALTHOUGH NOT IDEAL, SOLUTION.

(d) FIELD PLATE DIODE

AS PREVIOUSLY MENTIONED, IN ORDER TO PROVIDE PROPER PROTECTION USING A RESISTOR/DIODE NETWORK, THE DIODE REVERSE BREAKDOWN VOLTAGE MUST BE LESS THAN THAT OF THE MOS GATE OXIDE. ONE METHOD OF LOWERING THE BREAKDOWN OF A DIODE MADE FROM THE SOURCE AND DRAIN DIFFUSION (TYPICALLY

90 VOLTS), IS BY USE OF A FIELD AIDED BREAKDOWN DESIGN (FIGURE 10.11). THE IDEA IS TO COAT THE P-N JUNCTION WITH A THIN OXIDE LAYER OVERLAYED WITH A METAL ELECTRODE ATTACHED TO THE SUBSTRATE. THE APPROPRIATE BREAKDOWN VALUE CAN BE OBTAINED BY VARYING THE THICKNESS OF THE DIELECTRIC UNDER THE ELECTRODE. USING THE SAME DIELECTRIC AS THE GATE OF A MOS PART, A VALUE OF ABOUT 40 VOLTS IS GENERALLY ACHIEVED. ALTHOUGH THIS SCHEME IS SIMPLE, SINCE THE REDUCTION IN BREAKDOWN VOLTAGE OCCURS IN SUCH A SMALL REGION, THE SERIES RESISTANCE OF THE PART IS HIGH.

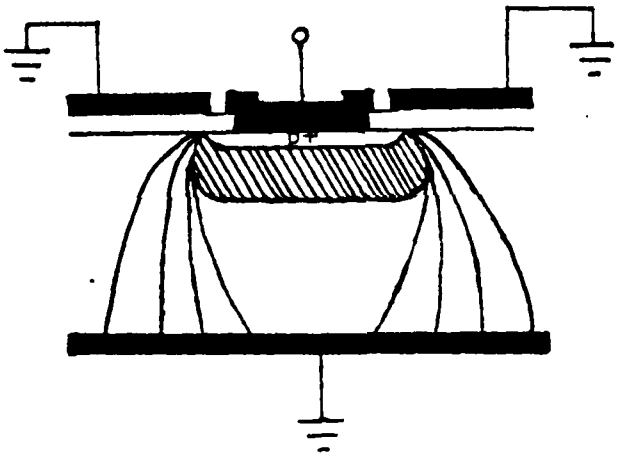


FIGURE 10.11: FIELD PLATED DIODE PROTECTION

(e) REACH-THROUGH AND PUNCH-THROUGH DIODES

IN ORDER TO OBTAIN THE APPROPRIATE BREAKDOWN VOLTAGE WITH A LOW DYNAMIC RESISTANCE, THE PART CAN BE FABRICATED IN A THIN EPITAXIAL LAYER ON A HIGHLY DOPED SUBSTRATE OF THE SAME TYPE (N EPI-LAYER ON N+ SUBSTRATE, FIGURE 10.12). AS THE VOLTAGE ACROSS THE DIODE INCREASES, THE DIODE DEPLETION LAYER REACHES THROUGH TO THE SUBSTRATE. WHEN THE VOLTAGE IS INCREASED FURTHER, THE DEPLETION LAYER CANNOT PENETRATE INTO THE

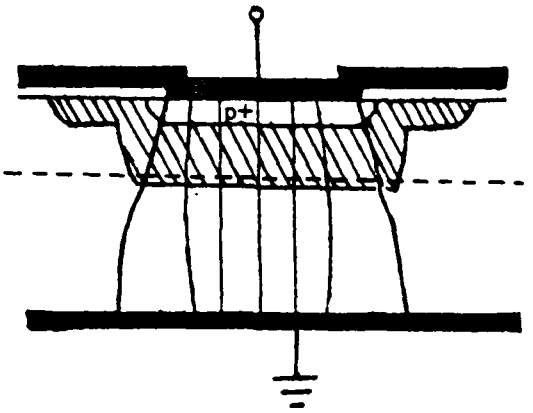


FIGURE 10.12: REACH-THROUGH DIODE

HIGHLY DOPED SUBSTRATE AND THE CRITICAL FIELD (E_{crit}) FOR BREAKDOWN IS REACHED AT A LOWER VOLTAGE THAN IN A UNIFORM MATERIAL. BREAKDOWN OCCURS UNIFORMLY OVER THE WHOLE AREA OF THE PART. THE SPREADING RESISTANCE IS VERY LOW BECAUSE OF THE LOW RESISTIVITY OF THE SUBSTRATE. THE DYNAMIC RESISTANCE IS DOMINATED BY THE RESISTANCE R_{SC} OF THE SPACE CHARGE LAYER, WHICH IN TURN IS RELATIVELY SMALL BECAUSE OF THE SMALL DEPLETION LAYER WIDTH.

INSTEAD OF REACH-THROUGH, PUNCH-THROUGH TO A SUBSTRATE OF THE OPPOSITE TYPE (N EPI-LAYER ON P SUBSTRATE) CAN SIMILARLY BE USED TO LOWER THE BREAKDOWN VOLTAGE (FIGURE 10.13). BREAKDOWN OCCURS AS SOON AS THE DIODE DEPLETION LAYER TOUCHES THE EPI-TO-SUBSTRATE DEPLETION LAYER. IN THIS CASE, DUE TO THE LARGER DEPLETION WIDTH THE SPACE CHARGER LAYER RESISTANCE R_{SC} IN PUNCH-THROUGH IS EXPECTED TO BE LARGER THAN IN REACH-THROUGH.

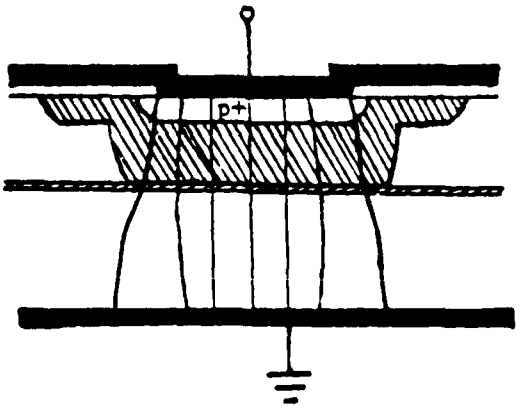


FIGURE 10.13: PUNCH-THROUGH DIODE

(f) ZENER DIODES

A SPECIAL TYPE OF GATE PROTECTION HAS TO BE USED WHERE POSITIVE AND NEGATIVE VOLTAGES ARE TO BE APPLIED TO THE GATE. FIGURE 10.14 SHOWS TWO PAIRS OF ZENER DIODES PROTECTING THE GATE. FOR THIS BILATERAL STRUCTURE, ONE STACK IS SUFFICIENT TO PROVIDE PROTECTION AGAINST EITHER POLARITY OR EXTRANEOUS VOLTAGE. ALTHOUGH TWO PAIRS OF ZENER DIODES ARE SHOWN, ANY NUMBER OF PAIRS, DEPENDING ON LOGIC LEVEL REQUIREMENTS OF THE CMOS CIRCUIT, CAN BE UTILIZED.

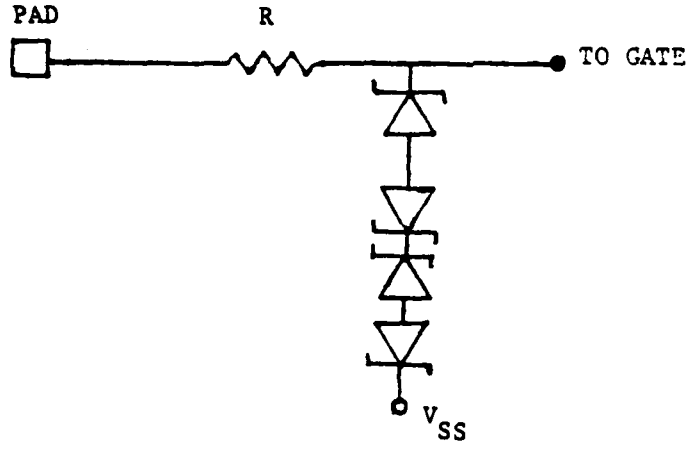


FIGURE 10.14: ZENER DIODES

(g) SPARK GAP

THIS PROTECTION TECHNIQUE USES TWO CLOSELY SPACED METAL PADS TO FORM A SPARK-GAP (FIGURE 10.15). PLACEMENT OF THE SPARK-GAP SHOULD BE BEFORE ANY ADDITIONAL PROTECTION CIRCUITRY. THIS TECHNIQUE CAN BE IMPLEMENTED BY LOCATING BONDING PADS CLOSE TO A SUBSTRATE METALLIZATION ENCIRCLING THE INTEGRATED CIRCUIT CHIP. TO PREVENT METAL TO METAL SHORTS, THE DISTANCE BETWEEN METAL SHOULD BE AT LEAST 50 MICRONS. SPARK-GAPS MUST BE USED IN

CONJUNCTION WITH A FIELD PLATED DIODE, PUNCH-THROUGH DIODE, OR SIMILAR SCHEME SINCE IT IS EFFECTIVE ONLY ABOVE 300 TO 400 VOLTS. TO ALLOW THIS VOLTAGE TO DEVELOP, IT MUST THEREFORE BE SEPARATED FROM THE ADDITIONAL CIRCUITRY BY A RESISTOR.

A REQUIREMENT FOR IMPLEMENTATION OF SPARK-GAPS IS THAT IT REQUIRES A CAVITY PACKAGE, WHICH CAN MAKE IT UNSUITABLE FOR MANY APPLICATIONS. THAT IS, THE AREA BETWEEN THE INPUT AND SUBSTRATE RING MUST BE LEFT UNPASSIVATED SO THAT THE IMPEDANCE OF THE GASEOUS DISCHARGE IS KEPT MINIMAL. THE USE OF CERTAIN HYDROCARBON-BASE COMPOUNDS AS ENCAPSULANTS SHOULD BE AVOIDED SINCE THEY CAN "CARBONIZE" AND FORM A CONDUCTIVE PATH ACROSS THE GAP. ALSO, OTHER DIFFUSIONS OR METALLIZATION SHOULD BE KEPT FURTHER AWAY FROM THE INPUT THAN THE SPARK GAP.

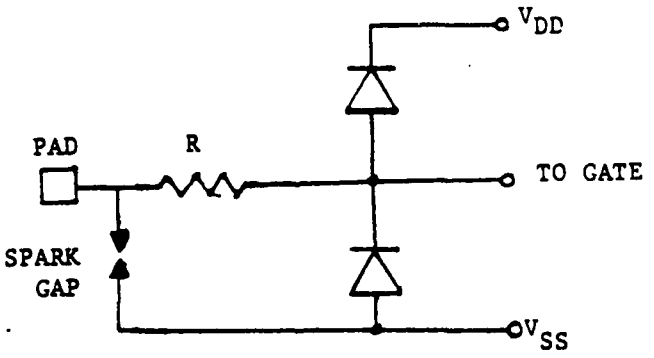


FIGURE 10.15: SPARK GAP AND DIODES

(h) OTHER TECHNIQUES

VARIOUS OTHER SPECIALIZED PROTECTION SCHEMES HAVE BEEN DEVELOPED, WHICH ARE ONLY APPLICABLE TO SPECIFIC CIRCUITS.

(3) PHANTOM EMITTER USED FOR ESD PROTECTION OF LINEAR INTEGRATED CIRCUITS (REFERENCE 37)

A LARGE PROPORTION OF ESDS DAMAGE TO LINEAR BIPOLAR INTEGRATED CIRCUITS HAS BEEN FOUND TO RESULT FROM SILICON MELTING DURING AN ESD PULSE. THIS HAS BEEN OBSERVED MOST FREQUENTLY IN THE EMITTER-BASE JUNCTION OF N-P-N INPUT TRANSISTORS, WHEN THAT JUNCTION IS PULSED INTO REVERSE BREAKDOWN. DAMAGING PULSES PERMANENTLY ALTER JUNCTION I-V CHARACTERISTICS, OFTEN DEGRADING LOW-CURRENT "h_{FE}". THIS CAN RESULT IN OFFSET ERRORS IN DIFFERENTIAL INPUT STAGES OF OP AMPS OR OTHER LINEAR CIRCUITS. DEPENDING ON PULSE STRENGTH, THE OFFSET ERRORS CAN EITHER BE SMALL ENOUGH TO PERMIT NEAR-NORMAL OPERATION, OR LARGE ENOUGH TO CAUSE CATASTROPHIC FAILURE.

THE ESD IMMUNITY OF AN N-P-N TRANSISTOR CAN BE MARKEDLY IMPROVED BY MAKING TWO CHANGES IN ITS STRUCTURE. ONE CHANGE IS TO INCREASE THE EMITTER-TO-BASE CONTACT SPACING FROM ITS USUAL DESIGN-RULE MINIMUM VALUE, TO ABOUT 50 MICRONS. THE ADDED BASE "BALLASTING" RESISTANCE IS AN EFFECTIVE DEFENSE AGAINST PULSES APPLIED BETWEEN EMITTER (+) AND BASE (-) TERMINALS. THE SECOND CHANGE IS THE ADDITION OF A SECOND EMITTER DIFFUSION, INSIDE THE BASE DIFFUSION, ADJACENT TO THE BASE DIFFUSION CONTACT AND SHORTED TO IT BY METAL. THE BASE CONTACT IS NOW BETWEEN THE TWO EMITTERS. THE ADDED "PHANTOM" EMITTER IS ACTIVE ONLY UNDER ESD CONDITIONS. IT LIMITS THE TRANSIENT VOLTAGE SUSTAINABLE BETWEEN THE BURIED COLLECTOR LAYER AND BASE CONTACT TO BV_{CEO} OF A NORMAL TRANSISTOR. IT DIVERTS PULSES APPLIED BETWEEN COLLECTOR (+) AND BASE (-) TERMINALS AWAY FROM THE NORMAL EMITTER-BASE JUNCTION, THAT OTHERWISE COULD EASILY BE DAMAGED BY AN ESD CURRENT. TOGETHER, THESE TWO STRUCTURAL CHANGES REMOVE THE MAJOR ESD WEAKNESSES OF THE CONVENTIONAL N-P-N IC TRANSISTOR.

IN TESTING THIS SCHEME A SERIES R-C CIRCUIT (1000 OHMS AND 230 pF) WAS USED AS A STANDARD ESD PULSE SOURCE; A WORST-CASE ESD DAMAGE THRESHOLD FOR THE PHANTOM EMITTER TRANSISTOR WAS FOUND TO BE 2000 VOLTS, COMPARED WITH 400 VOLTS FOR A CONVENTIONAL N-P-N IC TRANSISTOR EMPLOYING SIMILAR DESIGN RULES. THUS, THE PHANTOM EMITTER TRANSISTOR HAS BEEN FOUND TO WITHSTAND A VOLTAGE PULSE OF 1 TO 2 ORDERS OF MAGNITUDE HIGHER THAN A CONVENTIONAL N-P-N TRANSISTOR.

USING THIS PHANTOM EMITTER TRANSISTOR ON THE INPUTS OF A TYPICAL 741-TYPE OP AMP HAS RAISED THE OP AMP'S WORST-CONFIGURATION INPUT DAMAGE THRESHOLD FROM 500 VOLTS TO ABOVE 2000 VOLTS. THE IMPROVEMENT IS ACHIEVED AT THE COST OF ABOUT 50-60% MORE INPUT AREA, AND ADDITIONAL EXTRINSIC BASE RESISTANCE AND COLLECTOR-BASE CAPACITANCE. THESE PENALTIES ARE NORMALLY ACCEPTABLE ON ALL BUT THE VERY HIGHEST-FREQUENCY CIRCUITS.

THE PHANTOM EMITTER HAS ALSO BEEN SHOWN TO RAISE WORST-CASE INPUT DAMAGE THRESHOLD OF A SIMPLE DIFFERENTIAL N-P-N IC OP AMP INPUT STAGE FROM 500 VOLTS TO ABOVE 3000 VOLTS.

(4) ASSEMBLY PROTECTION CONSIDERATIONS

LEADS OF SENSITIVE PARTS MOUNTED ON PCBs SHOULD NOT BE CONNECTED DIRECTLY TO CONNECTOR TERMINALS WITHOUT SERIES RESISTANCE, SHUNTS, CLAMPS OR OTHER PROTECTIVE MEANS. ELECTRONIC ASSEMBLY DESIGNS CONTAINING ESDS ITEMS SHOULD BE REVIEWED FOR INCORPORATION OF PROTECTIVE CIRCUITRY. ONE METHOD OF ACHIEVING CIRCUIT PROTECTION FROM ESD IS TO USE TRANSIENT [illegible]PRESSORS. SOME TRANSIENT SUPPRESSORS WILL REDUCE THE VOLTAGE AND ENERGY [illegible]NDING UPON THE PULSE WIDTH AND SHAPE) FLOWING INTO AN ELECTRICAL CIRCUIT [illegible] EFFICIENTLY LOW TO AVOID DAMAGE TO ESDS ITEMS AT THE ASSEMBLY [illegible]ORS INCLUDE TIN-, ZINC OR BISMUTH OXIDE VOLTAGE-DEPENDENT

RESISTORS (VDRs) (OFTEN REFERRED TO AS METAL OXIDE VARISTORS), SILICON VOLTAGE LIMITERS, R-C NETWORKS AND SELENIUM STACKS. PRIOR TO MAKING AN ULTIMATE JUDGMENT ON ANY GIVEN TYPE OF SUPPRESSOR, A FINAL ANALYSIS MUST TAKE INTO CONSIDERATION PARAMETERS SUCH AS VOLTAGE LEVELS TO BE ENCOUNTERED, RESPONSE TIME OF THE SUPPRESSOR, PEAK CURRENT, LEAKAGE CURRENT, ENERGY ABSORPTION, OPERATING TEMPERATURE RANGE, LIFE, SIZE AND COST, AND THE END PRODUCT PROTECTION LEVEL DESIRED. A SMALL AMOUNT OF LEAD LENGTH CAN PROVIDE ENOUGH INDUCTANCE TO RUIN THE RESPONSE OF MOST SUPPRESSORS. HOWEVER, "ZERO INDUCTANCE" SUPPRESSORS ARE AVAILABLE THAT REDUCE THIS EFFECT (REFERENCE 38).

(5) PROTECTION AGAINST TRANSIENT UPSET

EQUIPMENT CONTAINING PARTS SUSCEPTIBLE TO TRANSIENT UPSET FROM ESD SPARKING SHOULD BE DESIGNED USING RADIO FREQUENCY INTERFERENCE (RFI) AND ELECTROMAGNETIC INTERFERENCE (EMI) PROTECTION SCHEMES. THESE SCHEMES INCLUDE THE FOLLOWING DESIGN PRACTICES:

(a) RFI/EMI DESIGN ZONING

INTEGRAL TO A TRANSIENT UPSET PROOF SYSTEM IS SHIELDING, SINGLE POINT GROUNDS, AND ISOLATION OF EMI SENSITIVE PARTS FROM EMI GENERATING ASSEMBLIES. THIS CONCEPT CAN BE USED TO ISOLATE ESDS PARTS FROM THE ENVIRONMENT. FIGURE 10.16 REPRESENTS THE ZONING CONCEPT AS APPLIED TO A CIRCUIT BOARD WITH ESDS PARTS. THE ESDS PARTS ARE MOVED TO THE CENTER OF THE PC BOARD WHERE ACCIDENTAL CONTACT IS UNLIKELY. THE POWER SUPPLY LEADS OF ALL THE PARTS ARE CAREFULLY BYPASSED AND ALL THE LEADS OF ESDS PARTS THAT GO EXTERNALLY ARE BUFFERED. THERE ARE NO SIGNAL LEADS NEARBY THAT CAN RF COUPLE ENERGY TO THE ESDS PARTS. ALTHOUGH ZONING IS SIMPLE IN CONCEPT,

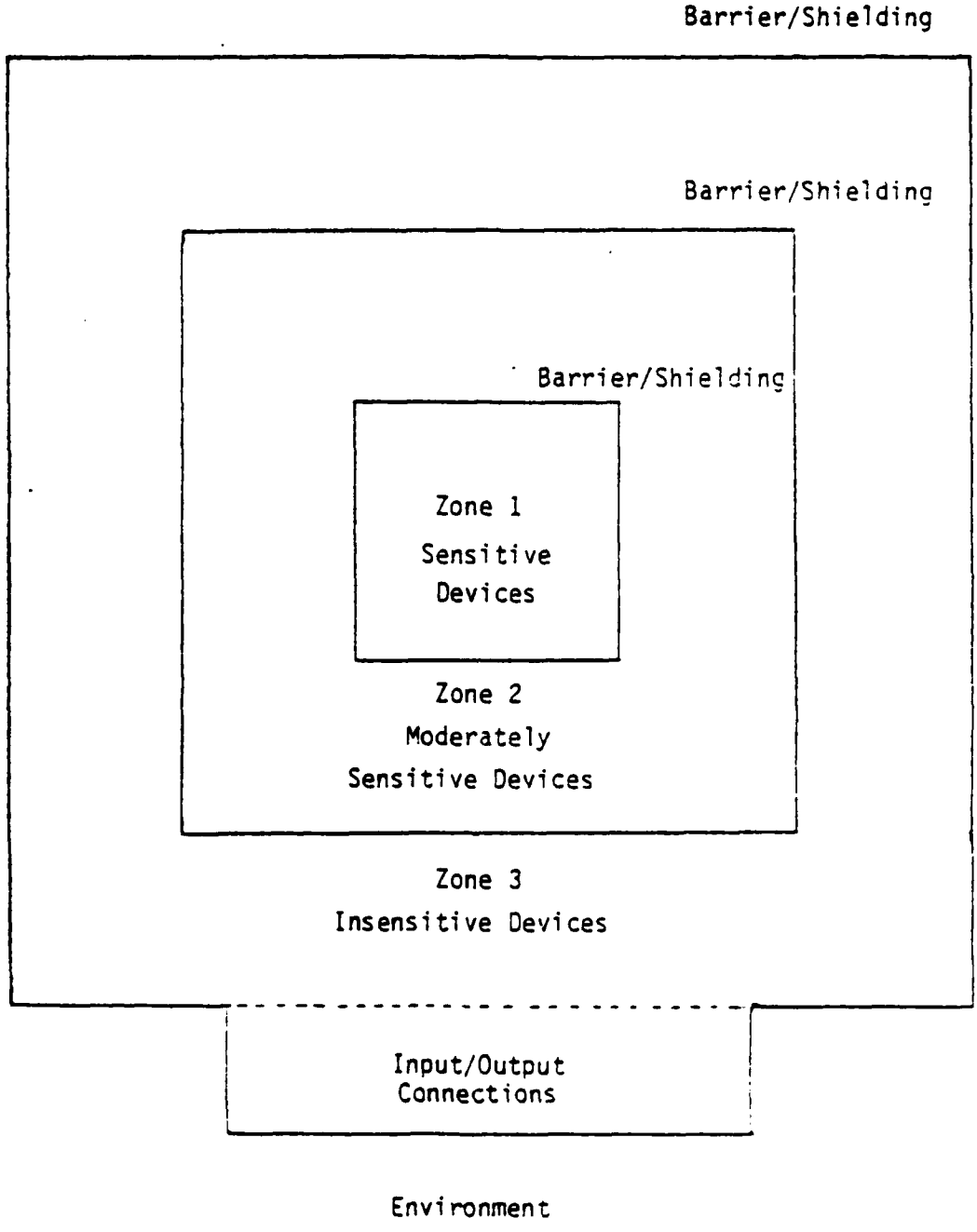


FIGURE 10.16: ZONING CONCEPT AS ESD PROTECTION FOR A PC BOARD

VIOLATIONS CAN BE SUBTLE SINCE THERE ARE NUMEROUS POSSIBLE PATHS FOR ALLOWING RF ENERGY INTO THE HIGH SENSITIVITY AREAS. SOME COUPLING CAN BE AS OBVIOUS AS ESD BREAKDOWN OF PANEL INDICATORS, OR AS SUBTLE AS RF LOOP COUPLING BETWEEN THE ESD SOURCE AND SENSITIVE AREAS. THIS LOOP COUPLING IS AN ESPECIALLY INSIDIOUS PROBLEM FOR OPERATING FREQUENCY BANDS OVER 500 MHz. THIS WIDE BANDWIDTH MAKES GOOD GROUND PLANES A NECESSITY.

(b) FARADAY SHIELDING AND MASKING

FOR MANY APPLICATIONS, SIMPLE FARADAY SHIELDING USING CONDUCTIVE FILMS OR FOILS CAN BE USED TO PROTECT VERY SENSITIVE ESDS PARTS. CARE MUST BE EXERCISED THAT THESE SHIELDS ARE NOT USED WHERE HIGHER PERFORMANCE RF SHIELDS ARE REQUIRED. A SIMPLIFIED SHIELDING CONCEPT FOR LOCALIZED PROTECTION OF AN ESDS PART IS SHOWN IN FIGURE 10.17. ALSO ONE MAY REDUCE THE SENSITIVITY OF AN ASSEMBLY BY INCREASING THE AMOUNT OF GROUND CONDUCTORS ON A PRINTED CIRCUIT BOARD. THESE EXTRA CONDUCTORS "MASK" THE SENSITIVE PART LEADS SO THAT THE PROBABILITY OF AN ESD SPARK CONNECTING TO A SIGNAL LINE IS REDUCED. A SIMILAR PROCESS RECOGNIZES THAT AN ESD SPARK IS MORE LIKELY TO STRIKE A CONDUCTOR EDGE WITH ITS MICROSCOPIC SHARP EDGES THAN THE SMOOTH SURFACE OF THE CONDUCTOR. THEREFORE, BY ETCHING A PATTERN ON THE GROUND PLANE, THE LIKELIHOOD OF AN ESD PULSE STRIKING A GROUND RATHER THAN A SIGNAL LINE IS INCREASED.

(c) GROUNDING

GROUNDING SCHEMES INCLUDE: THE MULTIPOINT UNCONTROLLED GROUND, THE FISH-BONE TYPE GROUND, AND THE SINGLE-POINT GROUND. EACH OF THESE SCHEMES LEAD TO DIFFICULTIES FOR COMPLEX SYSTEMS. A GROUNDING TECHNIQUE IS SHOWN IN FIGURE 10.18. THIS TECHNIQUE IS BASED ON IMPLEMENTATION OF THE CIRCUIT ZONING AND SHIELDING CONCEPTS PREVIOUSLY DESCRIBED, AND IT

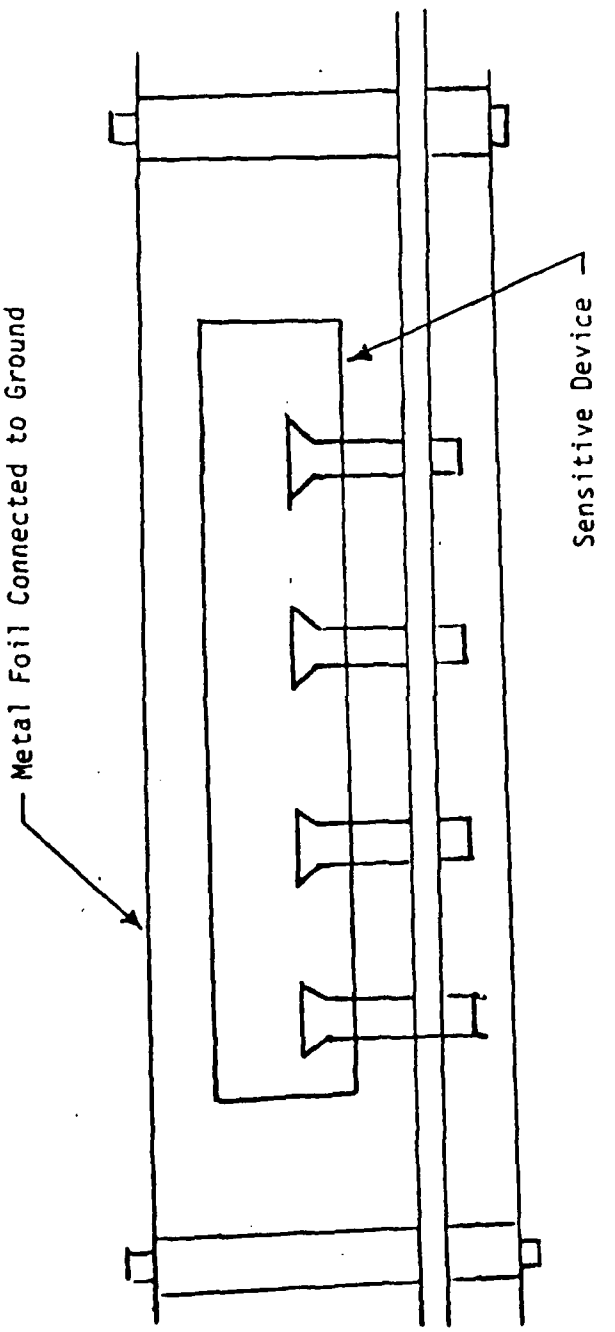


FIGURE 10.17: DEVICE FARADAY SHIELD

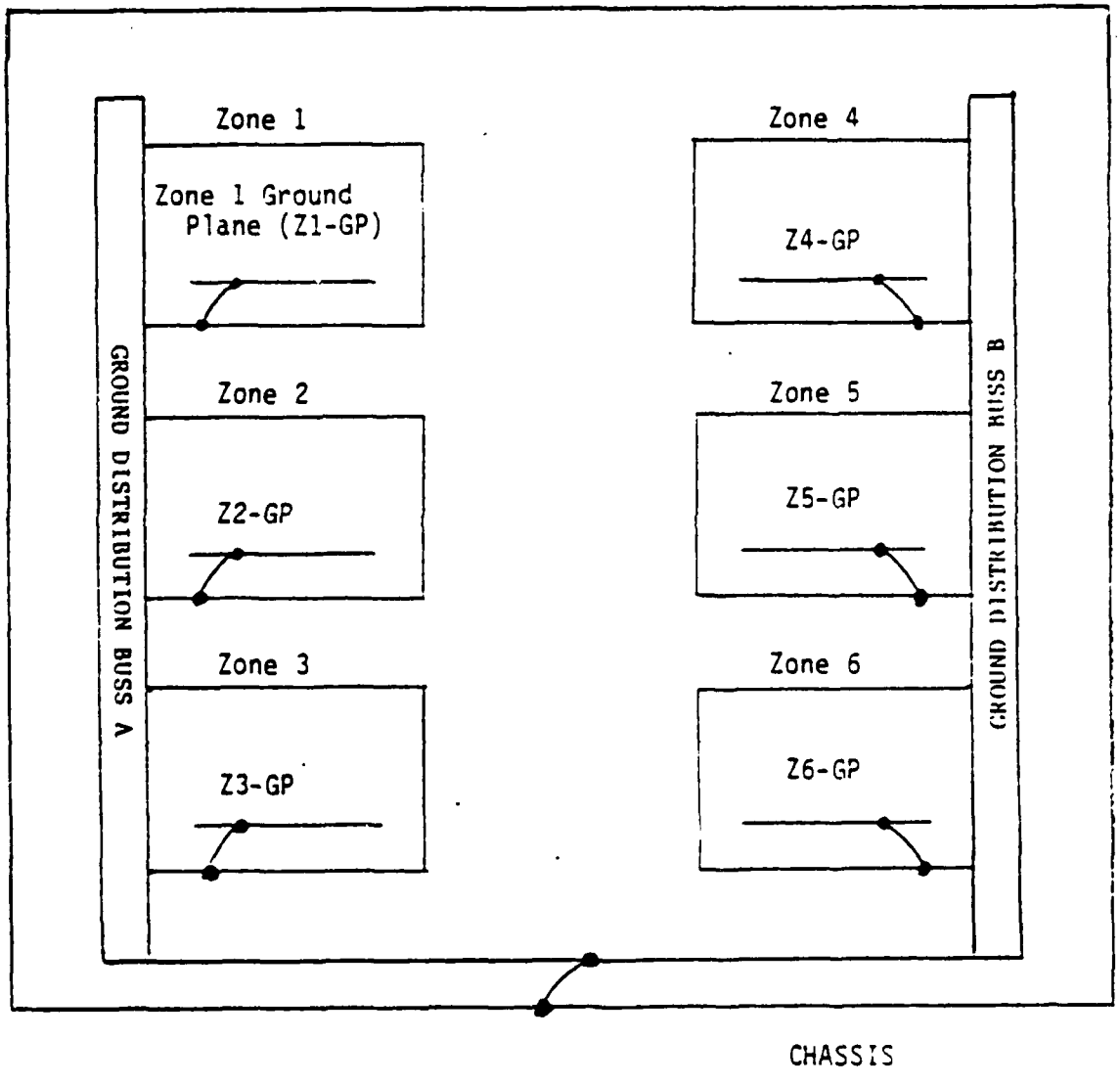


FIGURE 10.18: GROUNDING TECHNIQUE

EXHIBITS SOME ASPECTS OF THE MULTI-POINT, FISH-BONE, AND SINGLE-POINT GROUNDING SYSTEMS. AT EACH LEVEL OF ZONING, A GROUND PLANE IS PROVIDED. THIS GROUND PLANE IS CONNECTED TO THE PARTS WITHIN THE ZONE USING A MULTI-POINT GROUNDING SYSTEM. (CARE MUST BE TAKEN TO ENSURE THAT EACH COMPONENT FINDS ONLY ONE PATH TO THE GROUND PLANE). THE GROUND PLANE IS ALSO BONDED TO THE SHIELD OF THE ZONE. EACH ZONE WITHIN AN OVERALL CHASSIS IS THEN CONNECTED TO THE CHASSIS GROUND PLANE. DEPENDING ON THE COMPLEXITY OF THE SUBSYSTEM BEING DESIGNED, IT MAY BE NECESSARY TO PROVIDE MORE THAN ONE CHASSIS GROUND PLANE. FOR EXAMPLE: IN A RACK, SEPARATE PLANES MAY BE REQUIRED FOR EACH DRAWER. IN ANY CASE, THE CHASSIS GROUND PLANE(S) ARE THEN BONDED TO THE CHASSIS.

THE GENERAL SOLUTION FOR MANY OF THE COMMON IMPEDANCE PROBLEMS LIES IN ADEQUATE BONDING TECHNIQUES. IF A LOW IMPEDANCE PATH IS AVAILABLE THROUGHOUT THE GROUND PLANE, THEN COMMON IMPEDANCE PROBLEMS WILL USUALLY BE SIGNIFICANTLY REDUCED.

(d) CABLING PRACTICES

BESIDES DIRECT CONTACT INJECTION OF AN ESD, CABLE COUPLED ESD TRANSIENTS CAN BE A PROBLEM. SUCH ESD COUPLED TRANSIENTS CAN OCCUR IN SEVERAL WAYS:

- EM ENERGY PENETRATING THOUGH THE CABLE SHIELDING AND COUPLING INTO THE INNER CONDUCTORS.
- EM ENERGY TRANSFER FROM ONE CONDUCTOR TO ANOTHER WITHIN THE CABLE.
- EM-INDUCED SURFACE CURRENTS ON THE CABLE SHEATH WHICH INJECTS ENERGY INTO THE SYSTEM AT THE CABLE TERMINALS.

WIRING TO ESD ITEMS SHOULD BE SHIELDED WHERE POSSIBLE TO PREVENT TRANSIENT COUPLING. THE BEST SHIELDS ARE SOLID MATERIALS LIKE

CONDUIT, BUT METAL BRAID SHIELDS CAN BE USED EFFECTIVELY. IT IS IMPERATIVE THAT THE CONTINUITY OF SHIELDS BE MAINTAINED AT THE BACK SHELLS OF INTERFACE CONNECTORS. IN PARTICULAR, THE OVERALL SHIELD MUST HAVE CIRCUMFERENTIALLY COMPLETE TERMINATION TO THE CONNECTORS. PIGTAIL TERMINATIONS DO NOT PROVIDE ACCEPTABLE CONTINUITY. THE USE OF SPECIAL EMC/RFI PROTECTIVE CONNECTOR BACK SHELLS IS RECOMMENDED WHERE POSSIBLE. THE ORDER OF PREFERENCE FOR WIRING TO ESDS ITEMS IS: TWISTED SHIELDED PAIR; SHIELDED PAIR; AND TWISTED PAIR.

(e) CONTROLS, SWITCHES, KEY LOCKS

SYSTEMS INCORPORATING KEYBOARDS, CONTROL PANELS, MANUAL CONTROLS OR KEY LOCKS SHOULD BE DESIGNED TO DISSIPATE PERSONNEL STATIC CHARGES DIRECTLY TO CHASSIS GROUND, BYPASSING ESDS PARTS. IN COMPUTER ROOMS, ANTI-STATIC KEY LOCK SECURITY SWITCHES CAN BE EMPLOYED FOR STATIC PROTECTION.

EXAMPLE (N): DIODE PROTECTION (REFERENCE 29). ACCORDING TO FIGURE 10.10, THE SOURCE RESISTANCE "R_S" AND THE DYNAMIC RESISTANCE "R_D" CONSTITUTE A VOLTAGE DIVIDER FOR OVERVOLTAGE WHICH SHALL BE DEFINED AS THE TRANSIENT VOLTAGE "V_o", MINUS THE BREAKDOWN VOLTAGE "V_B" OF THE DIODE.

$$V_{MOS} = V_B + (V_o - V_B) \frac{R_D}{R_S + R_D} \text{ FOR } V_o \geq V_B$$

FOR PROTECTION AGAINST LARGE OVERVOLTAGE IT IS DESIRABLE TO KEEP "R_D" AS SMALL AS POSSIBLE. TO BE EFFECTIVE, "R_D" HAS TO BE MUCH SMALLER THAN THE SOURCE RESISTANCE "R_S" OF THE TYPICAL EXCITATION. "R_D" SHOULD BE THE SUM OF BOTH THE SPREADING RESISTANCE, "R_{SP}" AND THE DEPLETION LAYER RESISTANCE "R_{SC}". THE EXPRESSIONS FOR "R_{SP}" IS:

WHERE "d" IS THE DIAMETER OF THE DIODE AND "ρ" IS THE RESISTIVITY OF THE SUBSTRATE (REFERENCES 30 AND 31) AND THE EXPRESSION FOR "R_{SC}" IS:

$$R_{SC} = \frac{1}{2\varepsilon v_d} \cdot \frac{W_B^2}{A} = \frac{W_B^2}{A} \times 50 \text{ K}\Omega$$

WHERE "ε" IS THE DIELECTRIC CONSTANT OF SILICON, "v_d" IS THE LIMITING DRIFT VELOCITY, "W_B" IS THE DEPLETION LAYER WIDTH, AND "A" IS THE AREA OF THE DIODE. THE DYNAMIC RESISTANCE OF THE DIODE ($R_{SP} + R_{SC}$) DECREASES LINEARLY OR BY THE SQUARE OF "d", DEPENDING ON THE RELATIVE VALUES OF R_{SP} AND R_{SC}.

IN THIS EXAMPLE LET THE MAXIMUM OPERATING GATE VOLTAGE BE 30 VOLTS, AND LET THE BREAKDOWN VOLTAGE OF THE GATE PROTECTION DEVICE BE 40 VOLTS. FOR GATE PROTECTION, A .002 INCH DIAMETER DIODE IN A 5 Ω-CM SUBSTRATE IS USED. THE SPREADING RESISTANCE AND THE DEPLETION LAYER RESISTANCE, R_{SC} AND R_{SP} ARE CALCULATED AS FOLLOWS:

$$R_{SP} = \frac{5\ \Omega\text{-CM}}{2 \times 2 \times 10^{-3} \text{ IN.} \times 2.54 \text{ CM/IN.}} = 492 \simeq 500\Omega$$

$$R_{SC} = \frac{(7 \times 10^{-6} \times 10^{2} \text{CM})^2}{\pi(1 \times 10^{-3} \text{ IN.} \times 2.54 \text{ CM/IN})^2} \times 50 \times 10^{3}\Omega \simeq 1.0 \text{ K}\Omega$$

SINCE A DEPLETION LAYER WIDTH OF 7 μ CM CORRESPONDING TO A 40 VOLT REVERSE BIAS IS ASSUMED, THE DYNAMIC RESISTANCE OF THE DIODE IS:

$$R_D = R_{SP} + R_{SC} = .5 + 1.0 = 1.5 \text{ K}\Omega$$

FOR AN INPUT VOLTAGE, V_o = 80 V, LET US CONSIDER THREE DIFFERENT CASES:

CASE 1. IDEAL PROTECTION, I.E., $R_D = 0$

$$V_{MOS} = V_B + (V_o - V_B) \frac{R_D}{R_S + R_D}$$

$$= 40 + (80 - 40)\ (0)$$

$$= 40V$$

CASE 2. NO PROTECTION WITH ALSO $R_S = 0$

$$V_{MOS} = V_o$$

$$= 80V$$

CASE 3. DIODE PROTECTION WITH $R_D = 1.5\ K\Omega$ AND $R_S = 1.5\ K\Omega$:

$$V_{MOS} = 40 + (V_o - 40) \frac{1.5\ K\Omega}{1.5\ K\Omega + 1.5\ K\Omega}$$

$$= 40 + (V_o - 40)\ 1/2$$

$$= 40\ (80 - 40)\ 1/2 = 60V$$

THEREFORE USING A PRACTICAL DIODE THE TRANSIENT VOLTAGE ACROSS THE MOS DIELECTRIC HAS BEEN REDUCED FROM 80V TO 60V. "V_{MOS}" VS. "V_o" IS PLOTTED IN FIGURE 10.19 SHOWING IMPROVEMENT IN PROTECTION OF THE MOS PART USING A DIODE.

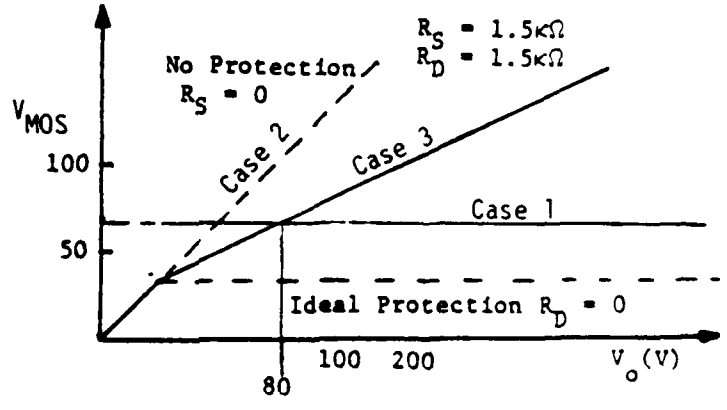
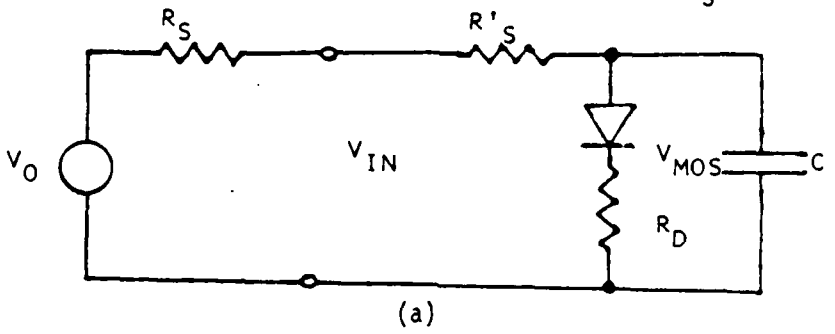


FIGURE 10.19: DIODE PROTECTION: VOLTAGE V_{MOS} ACROSS MOS DEVICE VERSUS SOURCE VOLTAGE V_o

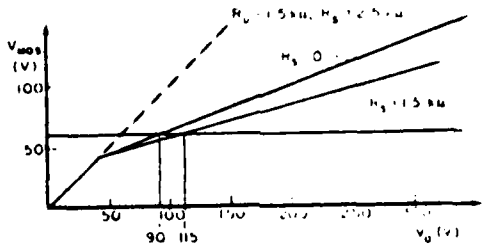
EXAMPLE (O): DIODE PROTECTION WITH ADDITIONAL RESISTANCE: TO ENSURE A MINIMUM VALUE OF EFFECTIVE SOURCE RESISTANCE, A RESISTANCE "R_S' " CAN BE ADDED IN SERIES WITH THE GATE AND THE PROTECTION DIODE AS ILLUSTRATED IN FIGURE 10.20. THIS INTRODUCES AN ADDITIONAL TERM INTO THE VOLTAGE DIVIDER RATIO:

$$V_{MOS} = V_B + (V_o - V_B) \frac{R_D}{R_S + R_S' + R_D} \text{ FOR } V_o \geq V_B$$

HOWEVER, THERE IS A MAXIMUM VALUE OF THIS RESISTANCE, "R_S'" GIVEN BY THE SPEED REQUIREMENT OF THE PROTECTIVE DEVICE OR THE CIRCUIT. IF A 2.5 K RESISTOR IS PUT IN SERIES WITH THE ABOVE MENTIONED 2 MIL DIAMETER DIODE THE SLOPE OF THE V_{MOS} VERSUS V_o CURVE IS ONLY SLIGHTLY REDUCED, AS ILLUSTRATED IN FIGURE 10.18. *WITH THE ADDITIONAL RESISTANCE BUT GIVES PROTECTION* WHEN THE SOURCE RESISTANCE IS VERY LOW (E.G., R_S = 0).



(a)



(b)

FIGURE 10.20: (a) DIODE PROTECTION WITH ADDITIONAL RESISTANCE, R_S'
(b) VOLTAGE V_{MOS} ACROSS MOS DEVICE VERSUS SOURCE VOLTAGE

THE SIMPLEST METHOD OF IMPLEMENTING THE EXTRA SERIES RESISTANCE IS BY USE OF A DIFFUSED RESISTOR WHICH COMBINES BOTH THE RESISTANCE AND DIODE BREAKDOWN FUNCTIONS IN ONE DEVICE. BECAUSE OF ITS DISTRIBUTED CHARACTER, THE COMBINATION IS MORE EFFECTIVE THAN ITS PARTS. THE DISTRIBUTED RESISTOR-DIODE NETWORK CHARACTERISTICS OF THE DIFFUSED RESISTOR IS SHOWN IN FIGURE 10.21 WHERE "r_s'" IS THE RESISTANCE PER UNIT LENGTH AND "r_d" IS THE DYNAMIC RESISTANCE PER UNIT LENGTH.

THE VOLTAGE ACROSS THE MOS DEVICE IS GIVEN BY:

$$V_{MOS} = V_B + (V_o - V_B) \frac{\sqrt{r_s' r_d}}{R_S + \sqrt{r_s' r_d}} \text{ COSH } (\sqrt{r_s'/r_d})\ X_r]^{-1}$$

FOR $V_o \geq V_B$

WHERE $\sqrt{r_s' v_d}$ IS THE INPUT IMPEDANCE AND X_r IS THE LENGTH OF THE RESISTOR.

FOR $(\sqrt{r_s'/r_d})\ X_r^{-1} \gg 1$

$$[\text{COSH } (\sqrt{r_s'/r_d})\ X_r]^{-1} \cong 2 \text{ EXP } [-(\sqrt{r_s'/r_d})\ X_r]$$

THEREFORE:

$$V_{MOS} = V_B + (V_o - V_B) \frac{\sqrt{r_s' r_d}}{R_S + \sqrt{r_s' r_d}} 2 \text{ EXP } [-(\sqrt{r_s'/r_d})\ X_r]$$

FROM THE ABOVE EXPRESSION WE SEE THAT $\sqrt{r_d/r_s'}$ IS A CHARACTERISTIC LENGTH OVER WHICH THE OVERVOLTAGE $(V_o - V_B)$ IS ATTENUATED BY A FACTOR OF "e". THIS EXPONENTIAL ATTENUATION, WHICH IS TYPICAL FOR DISTRIBUTED NETWORKS, IS THE BASIS FOR THE SUPERIORITY OF THE DISTRIBUTED RESISTOR DIODES. BECAUSE OF THE EXPONENTIAL RELATIONSHIP, THE DEPENDENCE OF THE PROTECTION ON THE DYNAMIC RESISTANCE IN BREAKDOWN IS EVEN STRONGER THAN FOR DIODE PROTECTION.

EXAMPLE (P): ADVANTAGE OF DIFFUSED RESISTOR OVER DIODE: AS AN EXAMPLE, FOR THE USE OF DISTRIBUTED RESISTOR CONSIDER A .4 X 10 MIL RESISTOR WHICH REQUIRES ABOUT THE SAME ACTIVE AREA AS THE 2 MIL DIAMETER DIODE USED FOR DIODE PROTECTION (EXAMPLE (N)). USING A SHEET RESISTANCE OF 100 Ω/SQ., WE FIND r_s' = 250 Ω/MIL WHERE (R_s' = 2.5 KΩ). ASSUMING A 5 Ω-CM SUBSTRATE, THE RESISTANCE "r_d" IS 2 KΩ/MIL (REFERENCE 38). FROM THIS WE CALCULATE THE INPUT IMPEDANCE $\sqrt{r_s' \cdot r_d}$ WHICH IS 700 Ω AND THE CHARACTERISTIC LENGTH $\sqrt{r_d / r_s'}$ WHICH IS 2.5 MIL. THIS WILL RESULT IN AN ATTENUATION OF THE OVERVOLTAGE BY A FACTOR OF 55. AS ILLUSTRATED IN FIGURE 10.21 THE MAXIMUM VOLTAGE THAT CAN NOW BE APPLIED WITHOUT DAMAGE IS 1140 V AS OPPOSED TO 80 V FOR DIODE PROTECTION AND 115 V FOR DIODE PROTECTION WITH ADDITIONAL RESISTANCE. IT CAN BE CONCLUDED THAT WITH REASONABLE VALUES FOR DIFFUSED SERIES RESISTANCE, VERY GOOD PROTECTION CAN BE OBTAINED EXCEPT FOR HIGH FAN-IN DIGITAL CIRCUITRY.

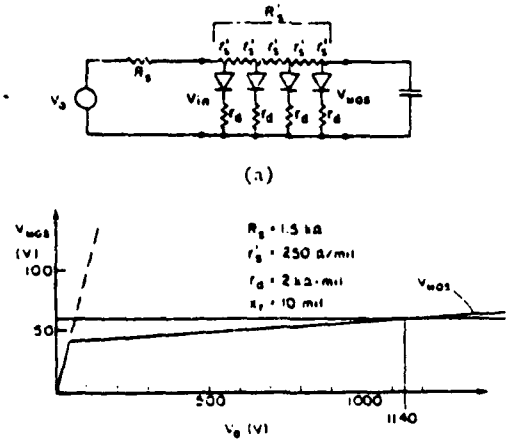


FIGURE 10.21: RESISTOR PROTECTION: (A) EQUIVALENT CIRCUIT; (B) VOLTAGE V_{MOS} ACROSS MOS DEVICE VERSUS SOURCE VOLTAGE V_0

XI. ESD HANDLING PRECAUTIONS AND PROCEDURES

A. GENERAL HANDLING PRECAUTIONS

THE NUMBER OF POTENTIALLY DAMAGING ESDs CAN BE SIGNIFICANTLY REDUCED BY SIMPLE IMPROVEMENTS IN THE WAY ITEMS ARE HANDLED. THE GENERAL GUIDELINES FOR HANDLING ESDS ITEMS ARE:

(1) PERSONNEL HANDLING ESDS ITEMS SHOULD BE TRAINED IN ESD PRECAUTIONARY PROCEDURES, TESTED FOR COMPETENCY, AND CERTIFIED. UNTRAINED PERSONNEL SHOULD NOT BE ALLOWED TO HANDLE ESDS ITEMS WHEN THEY ARE OUTSIDE OF THEIR PROTECTIVE PACKAGING.

(2) WHEN NOT ACTIVELY WORKING WITH ESDS ITEMS (E.G., TESTING, INSERTING PARTS INTO A PRINTED CIRCUIT BOARD (PCB) OR ASSEMBLIES IN AN EQUIPMENT) ESDS ITEMS SHOULD BE CONTAINED IN ESD PROTECTIVE COVERING. FOR SHORT TERM STORAGE AT A GROUNDED WORK STATION ESDS ITEMS CAN BE PROTECTED WITH SHORTING BARS, CLIPS OR CONDUCTIVE (NON-CORROSIVE) FOAM. PROTECTIVE PACKAGING SHOULD PROTECT THE PART FROM TRIBOELECTRIC GENERATION, DIRECT DISCHARGE AND ELECTROSTATIC FIELDS. WHEN INSERTING PART LEADS INTO PCB TERMINAL HOLES OR MAKING CONNECTIONS TO PART LEADS SHORTING BARS, CLIPS OR CONDUCTIVE FOAM SHOULD BE INSERTED OVER THE CONNECTOR TERMINALS AT THE PCB OR HIGHER ASSEMBLY LEVEL. FOR ESD PROTECTION FROM ELECTROSTATIC FIELDS, CONDUCTIVE WRAPPING SHOULD BE USED. THIS IS ESPECIALLY CRITICAL FOR ESDS ITEMS BEING TRANSPORTED OUTSIDE OF ESD PROTECTED AREAS.

(3) PERSONNEL MAINTAINING EQUIPMENT IN SITUATIONS WHERE PERSONNEL GROUND STRAPS CANNOT BE USED SHOULD GROUND THEMSELVES PRIOR TO REMOVING ESDS ITEMS FROM THEIR PROTECTIVE PACKAGING. THIS CAN BE ACCOMPLISHED BY TOUCHING THE METAL FRAME OF THE EQUIPMENT. ESDS ITEMS SHOULD NEVER BE HANDLED BY THEIR LEADS OR TERMINALS.

(4) THE LEADS OR CONNECTOR TERMINALS OF ESDS ITEMS SHOULD NOT BE PROBED BY MULTIMETERS (VOM) OR TEST EQUIPMENT LEADS UNLESS PRECAUTIONS ARE TAKEN TO GROUND THE LEADS PRIOR TO PROBING AN ESDS ITEM.

(5) TOOLS AND TEST EQUIPMENT USED IN ESD PROTECTIVE AREAS SHOULD BE PROPERLY GROUNDED; TOOLS WITH INSULATED HANDLES SHOULD BE TREATED WITH AN ANTISTAT. GROUNDING OF ELECTRICAL TEST EQUIPMENT SHOULD BE VIA A GROUNDED PLUG, NOT THROUGH THE CONDUCTIVE SURFACE OF THE ESD GROUNDED WORK STATION.

(6) WHEN TRANSFERRING ESDS PARTS FROM ONE CARRIER TO ANOTHER, THE TWO CARRIERS SHOULD BE ELECTRICALLY CONNECTED DURING THE TRANSFER.

(7) WORK INSTRUCTIONS, TEST PROCEDURES, OR DRAWINGS USED IN ESD PROTECTED AREAS SHOULD NOT BE COVERED IN COMMON PLASTIC SHEETING OR CONTAINERS. THIS IS A COMMONLY OVERLOOKED VIOLATION OF BRINGING PRIME ESD SOURCES INTO ESD PROTECTED AREAS.

(8) PART AND ASSEMBLY DRAWINGS FOR ESDS ITEMS SHOULD BE MARKED WITH THE ESD SENSITIVE ELECTRONIC SYMBOL AND REFERENCE OR SPECIFY ESD HANDLING PROCEDURES.

(9) MANUFACTURING, PROCESS, ASSEMBLY AND INSPECTION WORK INSTRUCTIONS SHOULD IDENTIFY ESDS ITEMS AND REFERENCE ESD PROCEDURES TO THE EXTENT NEEDED FOR ESD CONTROL THROUGHOUT THE MANUFACTURING PROCESS.

(10) PERSONNEL HANDLING ESDS ITEMS SHOULD AVOID PHYSICAL ACTIVITIES WHICH ARE STATIC PRODUCING IN THE VICINITY OF ESDS ITEMS (E.G., REMOVING OR PUTTING ON SMOCKS, WIPING FEET).

(11) PERSONNEL HANDLING ESDS ITEMS SHOULD WEAR ESD PROTECTIVE (E.G., VIRGIN COTTON) SMOCKS, OR ANTI-STATICALLY TREATED CLOTHING. SUCH CLOTHING SHOULD BE MONITORED PERIODICALLY WITH STATIC METERS. CLOSE-FITTING,

SHORT-SLEEVED "STREET" GARMENTS ARE ALSO ACCEPTABLE PROVIDED THEY DO NOT CONTACT ESDS ITEMS DIRECTLY. SYNTHETIC CLOTHING, NOT ANTI-STATICALLY TREATED SHOULD BE REGARDED AS A STATIC HAZARD AND WORK HABITS DEVELOPED THAT PREVENT CONTACTING ESDS ITEMS. GLOVES AND FINGER COTS, IF USED, SHOULD BE OF VIRGIN COTTON OR OF AN ESD PROTECTIVE MATERIAL.

(12) CONTINUITY AND RESISTIVITY CHECKS OF ALL ESD GROUNDING CABLES SHOULD BE PERFORMED PERIODICALLY WITH A MEGOHMETER TO ASSURE CONTINUITY AND CONFORMANCE TO SAFETY GROUNDING REQUIREMENTS.

(13) PLACE PACKAGED ESDS ITEMS ON AN ESD GROUNDED WORK BENCH SURFACE TO REMOVE ANY CHARGE PRIOR TO OPENING THE PACKAGING MATERIAL. ALTERNATELY, CHARGES CAN BE REMOVED BY GROUNDED PERSONNEL TOUCHING THE PACKAGING AND WORK BENCH TOP SIMULTANEOUSLY, DISSIPATING CHARGES THROUGH THE GROUND STRAP.

(14) REMOVE ESD PROTECTIVE COVERING OR SHORTING MATERIAL FROM ESDS ITEM ONLY FOR USE SUCH AS CONNECTION OF ESDS ITEM TO TEST EQUIPMENT OR FOR WIRING INTO A HIGHER ASSEMBLY.

(15) TEST CHAMBERS USING CARBON DIOXIDE OR NITROGEN GAS FOR COOLING SHOULD BE EQUIPPED WITH GROUNDED BAFFLES AND SHELVES TO DISSIPATE ELECTROSTATIC CHARGES CREATED BY THE FLOW OF THE GAS. IN-LINE IONIZERS ARE NEEDED WHEN THE CHAMBERS HAVE INSULATING SURFACES.

(16) ONLY BRUSHES WITH NATURAL BRISTLES SHOULD BE USED FOR CLEANING ESDS ITEMS, AND IONIZED AIR BLOWERS SHOULD BE DIRECTED OVER THE CLEANING AREA TO DISSIPATE ANY GENERATED STATIC CHARGES. ALL AUTOMATIC CLEANING EQUIPMENT SHOULD BE GROUNDED IF PRACTICABLE, AND LEADS AND CONNECTORS OF ESDS ITEMS SHOULD BE SHORTED TOGETHER DURING THE CLEANING OPERATION. CONDUCTIVE CLEANING SOLVENTS SHOULD BE USED WHERE PRACTICABLE.

(17) THE USE OF SOLVENTS SUCH AS ACETONE AND ALCOHOL CAN REDUCE THE EFFECTIVENESS OF SOME ESD PROTECTIVE MATERIALS, ESPECIALLY HYGROSCOPIC TYPES, AND SHOULD BE USED WITH CAUTION.

XII. MONITORING OF ESD CONTROL PROGRAMS

A. GENERAL

THE IMPLEMENTATION OF ESD CONTROLS SHOULD BE MONITORED PERIODICALLY BY THE IMPLEMENTER AND THE ACQUIRING ACTIVITY. THE MONITORING METHODS PROVIDED BY THE DOD-STD-1686 INCLUDE THE FOLLOWING:

- MONITORING OF IN-HOUSE ESD CONTROL PROGRAM REQUIREMENTS.
- MONITORING AND AUDITING OF SUBCONTRACTOR ESD CONTROL PROGRAM REQUIREMENTS.
- AUDITS AND REVIEWS BY THE ACQUIRING ACTIVITY INCLUDING THE REVIEW OF ESD CONTROL PROGRAM STATUS AT ESD DESIGN AND PROGRAM REVIEWS.

AN EFFECTIVE ESD CONTROL PROGRAM REQUIRES THE COORDINATION AND INTEGRATION OF VARIOUS ORGANIZATIONS OR FUNCTIONS WITHIN A FACILITY. ORGANIZATIONS AFFECTED INCLUDE:

- PROCUREMENT
- DESIGN ENGINEERING
- RELIABILITY ENGINEERING
- QUALITY ASSURANCE
- MANUFACTURING
- TEST/FIELD ENGINEERING
- PACKAGING AND SHIPPING

FROM A FUNCTIONAL STANDPOINT ESD OPERATING PROCEDURES APPLY TO:

- BUYING
- DESIGN/DRAFTING
- INSPECTION
- TEST

- MANUFACTURING/PROCESSING
- ASSEMBLY
- MAINTENANCE/REPAIR/REWORK (CONTRACTOR, FIELD, TENDER, DEPOT)
- PACKAGING AND MARKING
- STORAGE AND STOWAGE
- INSTALLATION
- TRANSPORTATION
- FAILURE ANALYSIS

B. ESD PROGRAM MONITORING AND AUDITS

(1) ESD PROGRAM MONITORING

ESD PROGRAM MONITORING SHOULD COVER ALL ASPECTS OF AN ESD CONTROL PROGRAM. THIS SHOULD BE A CONTINUING EFFORT OF THE CONTRACTORS' IN-HOUSE ESD QUALITY CONTROL FUNCTION AND SHOULD COVER THE IN-HOUSE ESD CONTROLS AND SUBCONTRACTORS' ESD CONTROL PROGRAMS. TO ASSIST IN PERFORMING THIS MONITORING, AN ESD CONTROL PROGRAM CHECKLIST IS PROVIDED IN TABLE XII-A.

(2) CERTIFICATION OF ESD PROTECTED AREAS AND GROUNDED WORK BENCHES

DOD-STD-1686 REQUIRES CERTIFICATION OF ESD PROTECTED AREAS BY THE CONTRACTOR. CERTIFICATION SHOULD CONSIDER THE FOLLOWING:

(a) THE USE OF ESD PROTECTIVE MATERIALS WHEREVER ESDS ITEMS NORMALLY COME IN CLOSE PROXIMITY (E.G., 1 METER) OF ESDS ITEMS. THIS INCLUDES: PARTS TRAYS, BINS, CARRIERS, CARTS, TOTE BOXES, PACKAGING, WORK SURFACES AND WORK STOOLS.

(b) THE INCORPORATION OF PERSONNEL GROUNDING SYSTEMS.

(c) THE INCORPORATION OF GROUNDING OR IONIZING SYSTEMS FOR PROCESSING MACHINERY.

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Procurement	1. Are personnel trained in ESD awareness? 2. Do standard ESD contract requirements exist for inclusion of ESD control requirements in procurement? 3. Have pre-award and in-process audits of subcontractors been performed to assure suppliers have effective ESD control programs? 4. Is a list maintained of subcontractors and suppliers who have established adequate ESD control programs (based on ESD control program audits)? 5. Are all items to be procured identified by engineering as ESDS (or non-ESDS) so that the proper ESD control program requirements clauses can be included in the subcontracts or purchase orders? 6. Are ESD program requirements incorporated for all procurements of ESDS items? 7. Are subcontractors/suppliers required to certify that ESDS items were manufactured, handled and packaged under ESD controls?		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Engineering/ Design Services	1. Are personnel trained in ESD awareness?		
	2. Are all electrical parts in the design classified as either ESDS or non-ESDS?		
	3. Are parts selected that have the greatest immunity from ESDS?		
	4. Are less sensitive ESDS items used where they will meet performance requirements?		
	5. Is protective circuitry incorporated at the lowest practicable assembly level to protect sensitive ESDS items at the assembly and equipment levels?		
	6. Has analysis been performed to verify the adequacy of protective circuitry?		
	7. Parasitic devices:		
	a. Are power supplies controlled to prevent parasitic device conditions in MOS and other types of semiconductors?		
	b. Are power supply currents limited to prevent damage from parasitic and/or other unintended modes of operation?		
	8. Do all drawings of ESDS items identify the item as ESDS; are they marked with sensitive electronic device symbol of MIL-STD-129 and ESD caution; do they reference applicable ESD precautionary procedures; and do they identify the sensitive pins or terminals of assemblies and equipment?		
	9. Does all procurement documentation of subcontractor ESDS items specify the requirements of an ESD control program?		
	(Continued)		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Engineering/ Design Services (Continued)	10. Does the drawing or specification require ESD classification testing when the ESD sensitivity of the item is unknown?		
	11. Do the drawings show the requirements for proper ESD marking of ESDS assemblies and equipment located so that it can be readily seen by maintenance personnel prior to removing/replacing the ESDS item?		
	12. Do design engineers assist in failure analysis of ESDS items and implementation of corrective action?		
	13. Are ESD design considerations and conformance to ESD requirements included in all design reviews?		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Equipment/System Test and Integration	1. Are personnel trained in ESD awareness? 2. Is testing performed in ESD protected areas which limit static voltages to 4000 volts or less? 3. Are ESD precautionary procedures provided for personnel who install ESDS equipment? 4. Are test chambers grounded, equipped with grounded baffles, ionizers, etc. to assure high static voltages are not generated within the chambers? 5. Are ESDS items enclosed in ESD protective covering prior to transfer out of the ESD protected area?		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Production: Receiving Inspection	1. Are all personnel who handle (e.g., inspect) ESDS items trained in ESD awareness?		
	2. Is the receiving area equipped as an ESD protective area where packages of ESDS items are opened?		
	3. Are ESD precautionary procedures provided for personnel who handle ESDS items out of their protective packaging?		
	4. Are ESDS items identified on shipping documents and labeled as ESDS by the supplier?		
	5. Are ESDS items removed from their ESD protective packaging for inspection or test, repackaged in ESD protective material after inspection?		
Processing, Assembly, Inspection, Repair and Rework	1. Are all personnel who handle (process, assemble, test, repair, rework, etc.) trained in ESD awareness?		
	2. Are functions involving ESDS items outside of their protective packaging performed only in ESD protected areas?		
	3. Is all processing machinery properly grounded or equipped with ionizers or other means to limit static to safe levels?		
	4. Are carts or wagons used to transport ESDS items throughout the plant equipped with conductive wheels to control the buildup of unsafe static charges?		
	(Continued)		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Processing, Assembly, Inspection, Repair and Rework (Continued)	5. Are all part carriers (tote boxes/ trays, etc.) used to transport ESDS items made of ESD protective (preferably conductive) materials?		
	6. Are ESD precautionary procedures provided for all personnel who handle ESDS items during the production operation?		
	7. Do all work instructions identify ESDS items and the precautionary procedures to be implemented for each process?		
	8. Do ESDS items and parts trays, bins, etc. containing ESDS items have ESDS identification?		
	9. Are ESDS items enclosed in ESD protective covering material after completion of assembly and test?		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Packaging and Shipping	1. Are personnel trained in ESD awareness? 2. Is handling and packaging performed in ESD protected areas? 3. Are ESD precautionary handling and packaging procedures provided for personnel who package the ESDS item(s) for delivery? 4. Does packaging provide protection against: a. Triboelectric generation? b. Direct discharge from a charged person or object? c. Electrostatic fields? 5. Are packaging containers properly marked with the MIL-STD-129 electronic device sensitive symbol and ESD caution?		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Quality Assurance/Reliability	1. Are all inspectors and quality control engineers who handle or maintain the ESD control program requirements trained in ESD awareness?		
	2. Are all inspection areas where ESDS items are handled, inspected or tested, ESD protected?		
	3. Are ESD precautionary procedures provided for all quality functions and documented in the contractor's quality assurance manual?		
	4. Has Quality Assurance certified the ESD protected areas?		
	5. Does quality inspection include the proper ESD marking of hardware (assembly and equipment levels)?		
	6. Does quality control ensure drawings and specifications provide adequate identification of ESDS items and sensitive terminals, ESD caution markings and reference to ESD precautionary procedures?		
	7. Does quality control review procurement drawings, specifications and subcontracts for adequate ESD control program requirements?		
	8. Do quality assurance personnel (with the assistance of procurement personnel) perform pre-award surveys of contractor's ESD control programs and maintain lists of qualified suppliers?		
	9. Do quality assurance personnel periodically audit in-house ESD controls?		
	(Continued)		

TABLE XII-A

ESD CONTROL PROGRAM - SURVEY CHECKLIST

FUNCTION	RESPONSIBILITY	ADEQUATE	
		YES	NO
Quality Assurance/Reliability	10. Do quality assurance personnel monitor and perform periodic audits of subcontractor ESD control programs?		
	11. Are failure analysis laboratories equipped with ESD protected areas?		
	12. Do failure analysis equipment, failure analysis processes and techniques lend themselves to evaluation of ESD failure mechanism?		
	13. Are updated listings of ESDS parts and sensitivity levels maintained for use by engineering?		
	14. Does reliability review the ESD control program design requirements and the adequacy of ESD protective circuitry?		
	15. Does reliability maintain a data bank of failures related to ESD to determine ESD failure trends, causes and needed corrective actions?		
	16. Does the contractor have the equipment to perform ESD classification testing in accordance with the DOD-STD-1686?		

(d) THE CONTROL OF STATIC BELOW THE SENSITIVITY LEVEL OF ESDS ITEMS BEING HANDLED IN AN ESD PROTECTED AREA.

(e) ABSENCE OF PRIME STATIC SOURCES IN OR NEAR THE ESD PROTECTED AREA.

(f) GROUNDING OF POWER TOOLS (E.G., SOLDERING IRONS, SOLDER POTS, ETC.) AND TEST EQUIPMENT USED IN ESD PROTECTED AREAS.

(g) AVAILABILITY OF ESD PROTECTIVE PERSONNEL APPAREL FOR USE IN ESD PROTECTED AREAS INCLUDING CONDUCTIVE SHOES OR HEEL GROUNDERS WHERE CONDUCTIVE FLOORS ARE USED.

(h) RESISTANCE MEASUREMENTS OF ALL GROUNDING TO ASSURE THAT RESISTANCES ARE LOW ENOUGH TO LIMIT RESIDUAL ESD VOLTAGES AND HIGH ENOUGH TO PROTECT PERSONNEL FROM NEARBY VOLTAGE SOURCES.

(i) EFFECTIVENESS OF THE ESD PROTECTED AREA AND GROUNDED WORK BENCHES TO LIMIT ELECTROSTATIC VOLTAGES TO SAFE LEVELS USING ELECTROSTATIC METERS OR DETECTORS.

(j) EFFECTIVENESS OF ESD PROTECTIVE EQUIPMENT SUCH AS IONIZERS, BUILT-IN DETECTORS/ALARMS AND HUMIDITY CONTROL WHERE USED.

C. FORMAL REVIEWS

ANOTHER STEP IN REVIEWING AND MONITORING THE ADEQUACY OF ESD CONTROL PROGRAMS IS BY MEANS OF FORMAL CUSTOMER-CONTRACTOR REVIEWS. THESE REVIEWS ARE DESIGNATED AS: DESIGN REVIEWS WHICH TAKE PLACE DURING THE DESIGN/DEVELOPMENT PHASE, AND PROGRAM REVIEWS WHICH COVER THE TRANSITION FROM DESIGN TO PRODUCTION.

(1) ESD DESIGN REVIEWS

THE DESIGN DECISIONS RELATING TO THE ESD CONTROL PROGRAM ARE TO BE PRESENTED AT DESIGN REVIEWS AND MUST INCLUDE THE FOLLOWING:

(a) IDENTIFICATION OF ESDS ITEMS.

(b) RESULTS OF CLASSIFICATION CIRCUIT ANALYSIS FOR ASSEMBLIES AND EQUIPMENT.

(c) PROTECTIVE CIRCUITRY METHODOLOGY FOR ESDS ITEMS AND EXTERNAL INTERFACES.

(d) ESD MARKING OF DOCUMENTATION.

(e) ESD MARKING OF ESDS ITEMS.

(f) PROBLEM AREAS AND PROPOSED CORRECTIVE ACTIONS.

(2) ESD PROGRAM REVIEWS

PROGRAM REVIEWS INCLUDE THE FOLLOWING REVIEW TOPICS:

(a) ESD PRECAUTIONARY PROCEDURES FOR HANDLING ESDS ITEMS.

(b) GENERAL DESIGN, CONSTRUCTION AND MAINTENANCE OF ESD PROTECTED AREAS.

(c) METHODS AND PROCEDURES FOR CERTIFYING ESD PROTECTIVE AREAS.

(d) QUALITY ASSURANCE METHODS AND PROCEDURES FOR MONITORING THE CONTINUED EFFECTIVENESS OF ESD PROTECTIVE AREAS.

(e) QUALITY ASSURANCE MONITORING OF THE COMPLETE ESD CONTROL PROGRAM FUNCTIONS.

(f) ESD AWARENESS TRAINING.

(g) PACKAGING AND LABELING OF ESDS ITEMS.

(h) PROBLEM AREAS AND PROPOSED CORRECTIVE ACTIONS.

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