Practical Design of Buck Converter

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Cal Poly
Learn by Doing

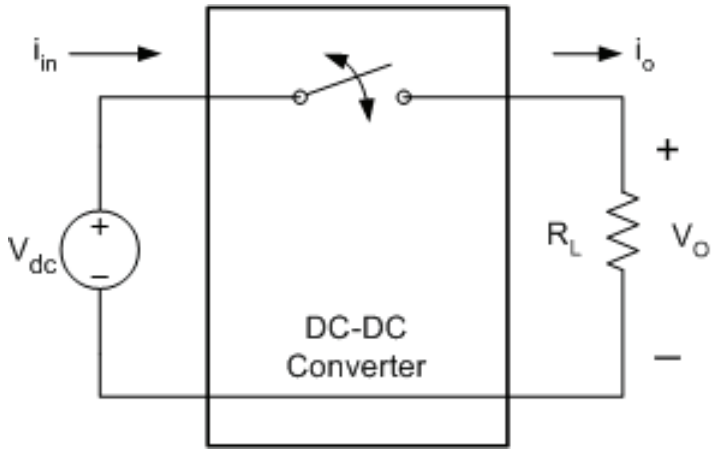
Tutorial Outline

- Brief Review of DC-DC Converter
- Design Equations
- Loss Considerations
- Layout Considerations
- Efficiency Improvement
- Synchronous Buck
- Resonant Buck
- PWM Controller
- Multiphase

Review: DC-DC Converter Basics

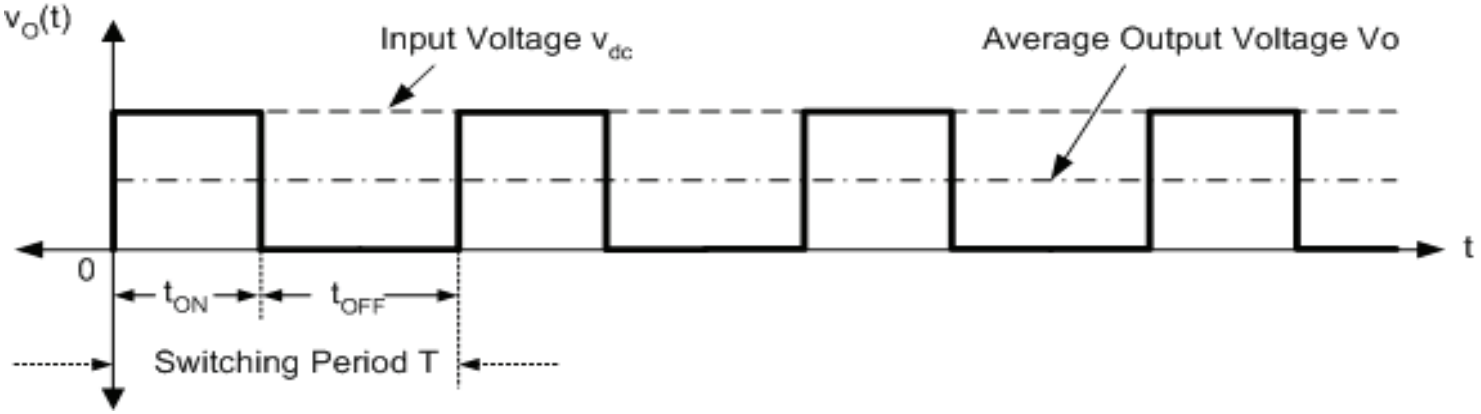
- A circuit employing switching network that converts a DC voltage at one level to another DC voltage
- Two basic topologies:
  - Non-Isolated
    - Buck, Boost, Buck-Boost, Cuk, SEPIC
  - Isolated
    - Push-pull, Forward, Flyback, Half-Bridge, Full-Bridge

Review: DC-DC Converter Basics



- When ON: The output voltage is the same as the input voltage and the voltage across the switch is 0.
- When OFF: The output voltage is zero and there is no current through the switch.
- Ideally, the Power Loss is zero since output power = input power
- Periodic opening and closing of the switch results in pulse output

Review: DC-DC Converter Basics

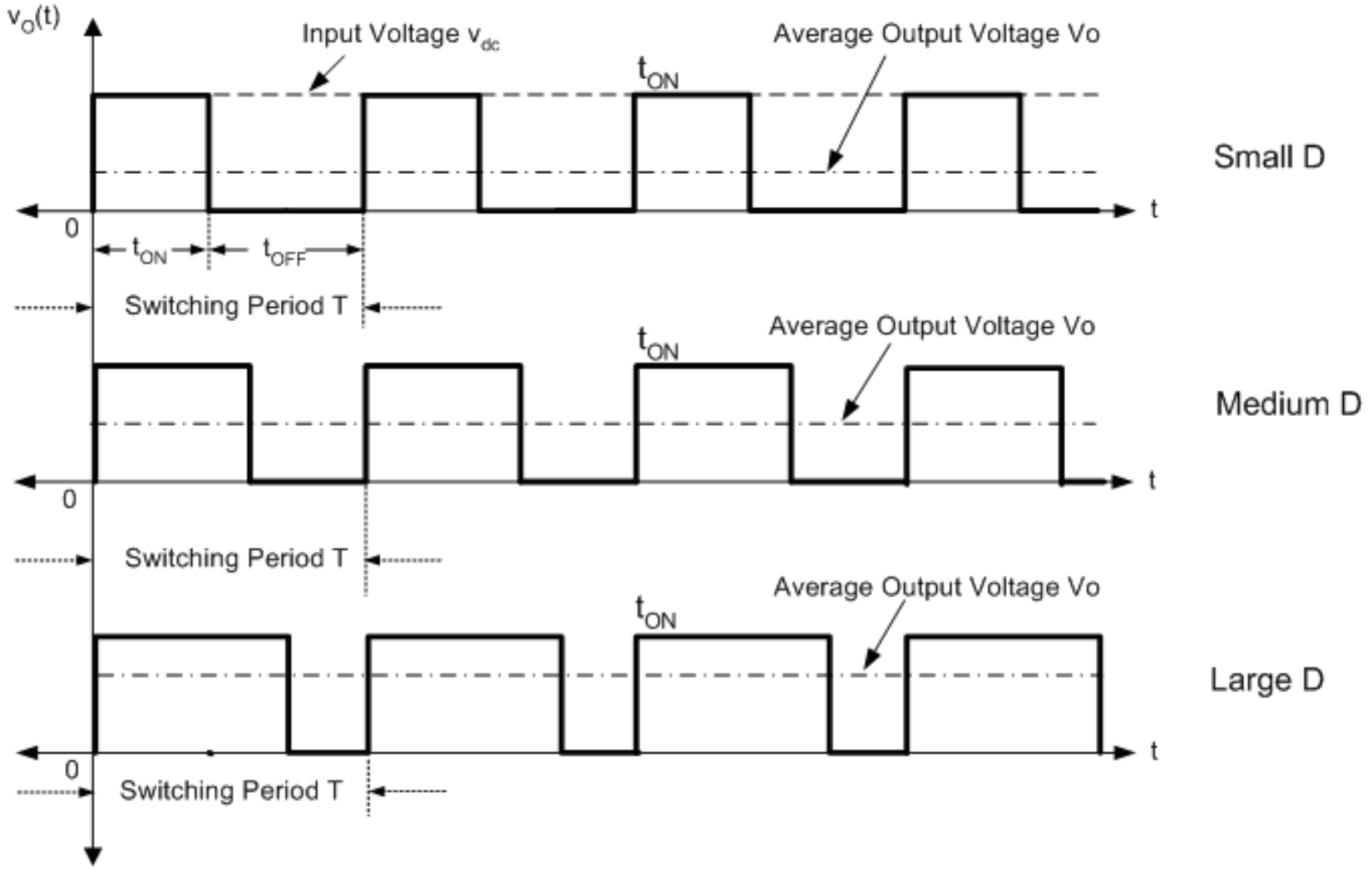


$$\overline{V}_0 = \frac{1}{T}\int_0^T v_o(t)\,dt = \frac{1}{T}\int_0^{DT} V_i\,dt = V_i D$$

$$Dutycycle = D = t_{on} f_s = \frac{t_{on}}{T}$$

- Duty Cycle range: 0 < D < 1
- Two ways to vary the average output voltage:
  - Pulse Width Modulation (PWM), where ton is varied while the overall switching period T is kept constant
  - Pulse Frequency Modulation (PFM), where ton is kept constant while the switching period T is varied

Review: DC-DC Converter Basics



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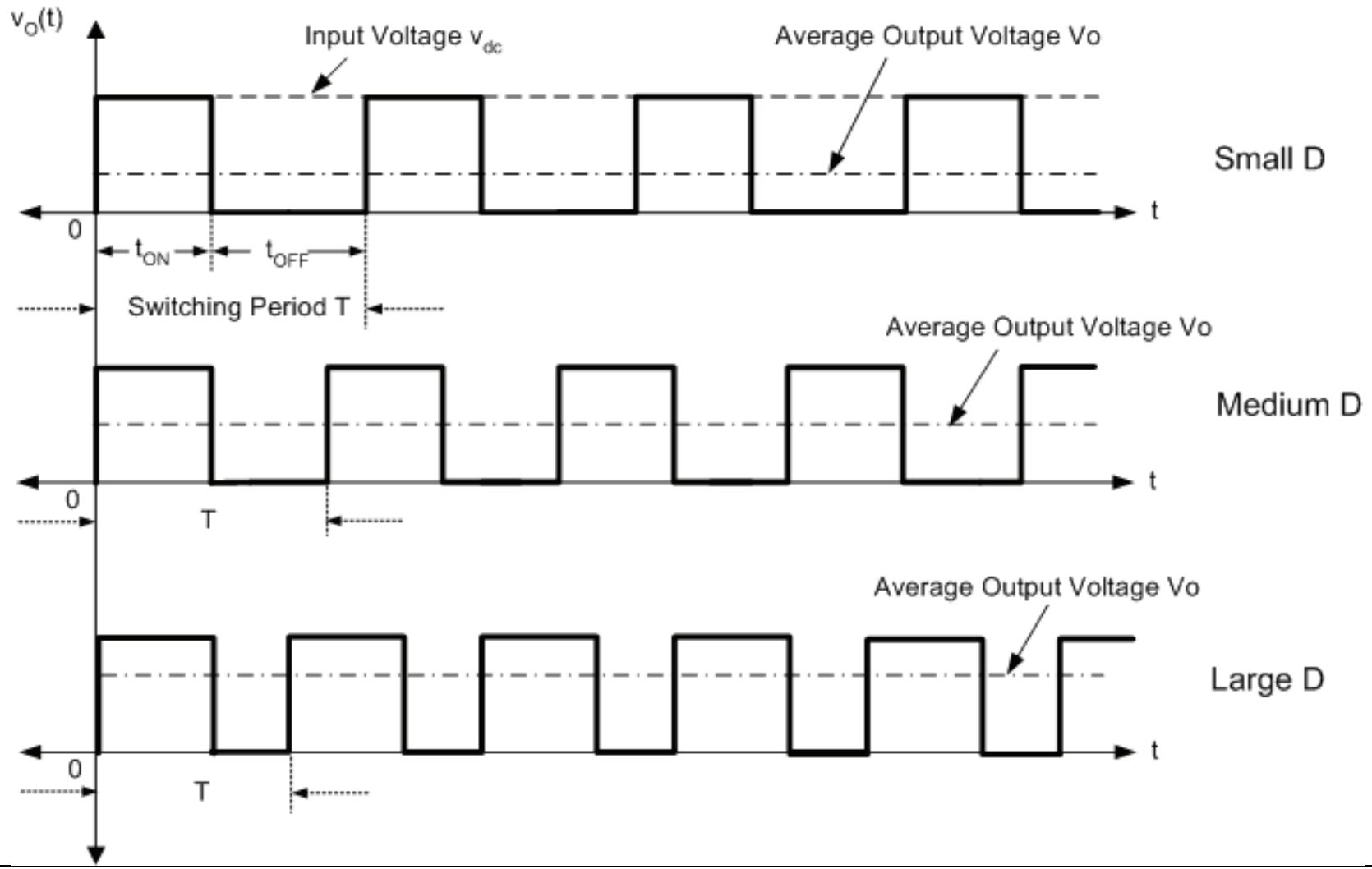

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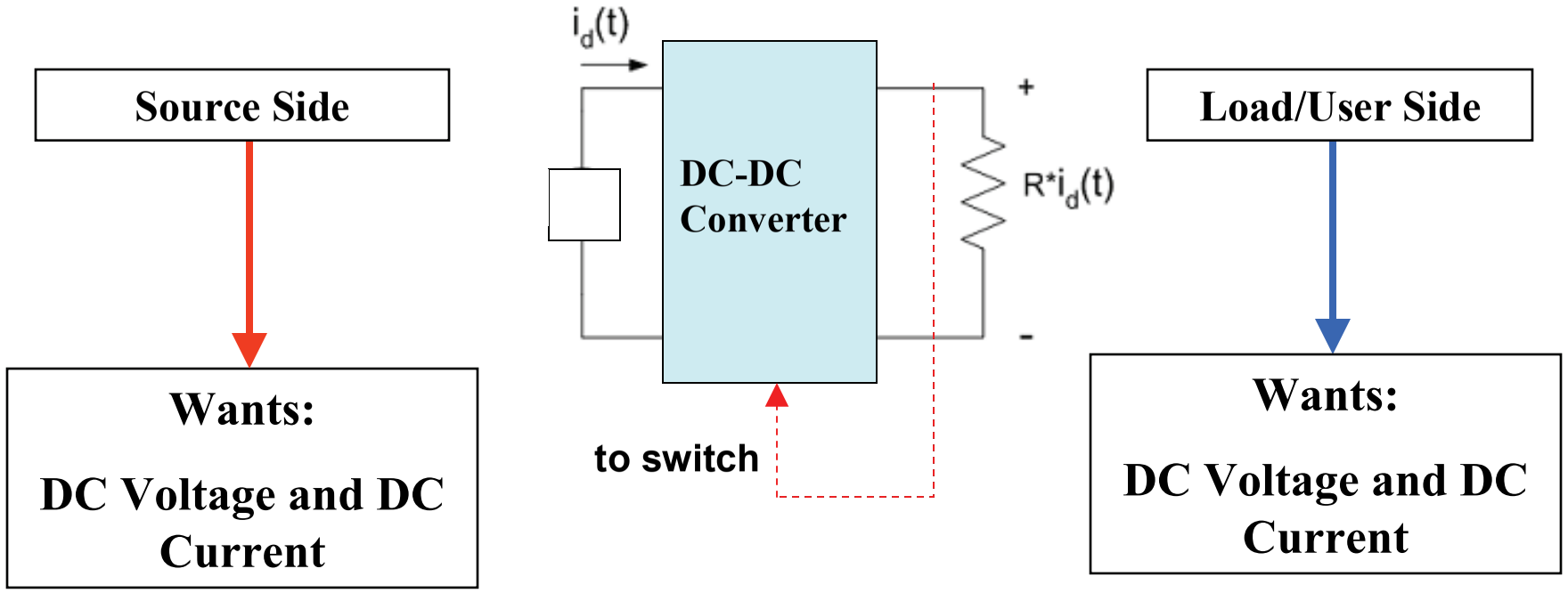
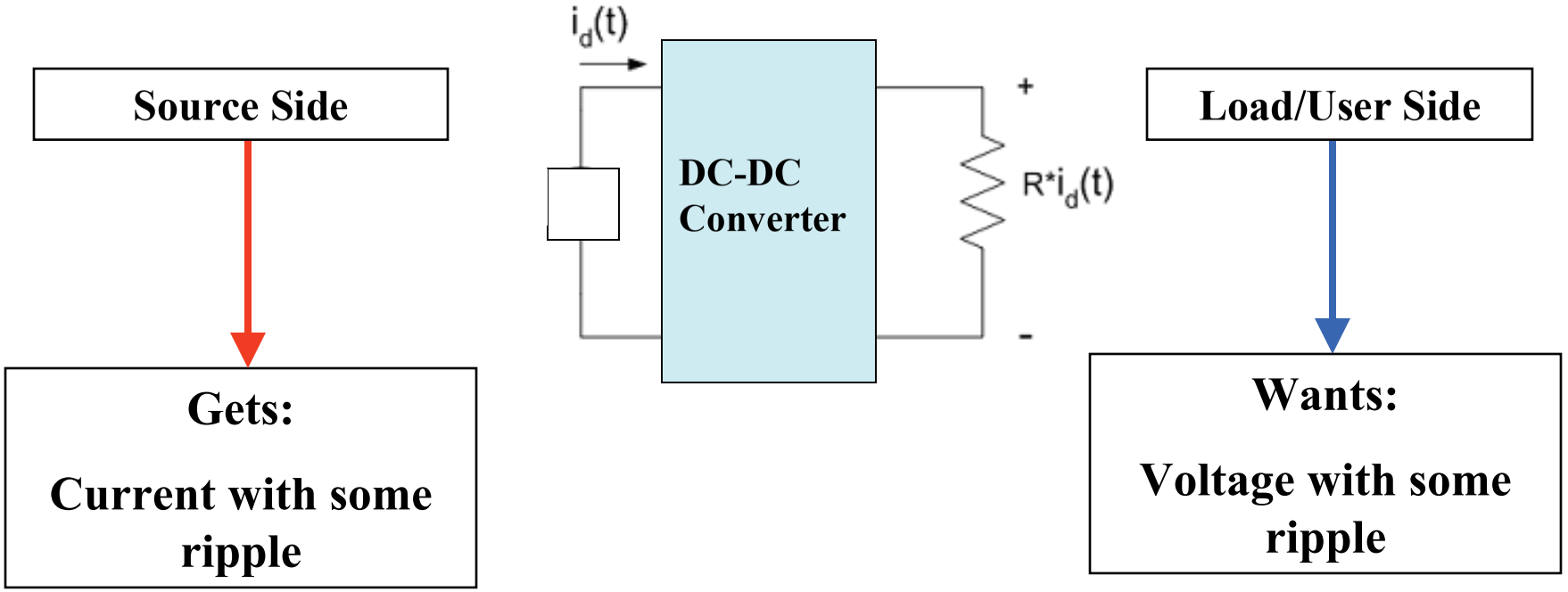


Wants:

No AC Component

No Harmonics

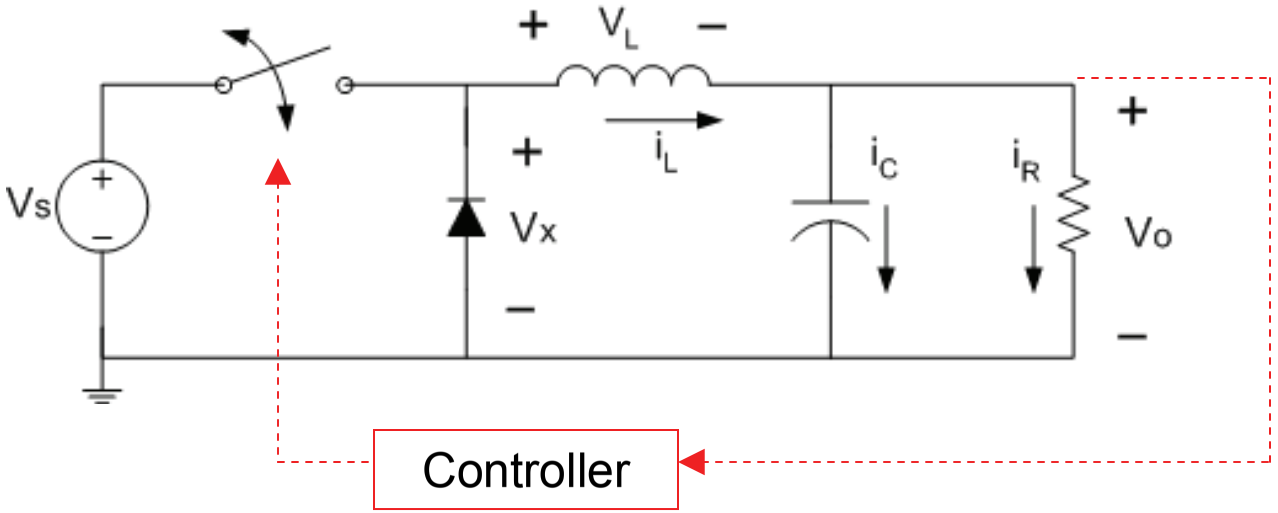
Review: DC-DC Converter Basics



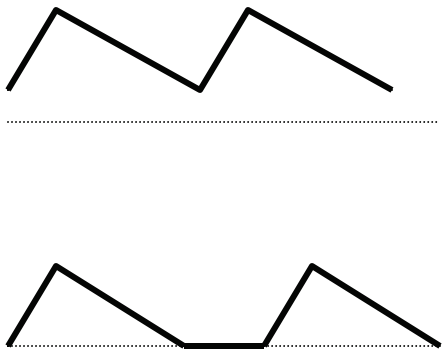
What is Buck Converter?

- A dc-dc converter circuit that steps down a dc voltage at its input
- Non-isolated hence ideal for board-level circuitry where local conversion is needed
  - Cell-phones, PDAs, fax machines, copiers, scanners, computers, anywhere when there is the need to convert DC from one level (battery) to other levels
- Widely used in low voltage low power applications
- Synchronous version and resonant derivatives provide improved converter's efficiency
- Multiphase version supports low voltage high current applications

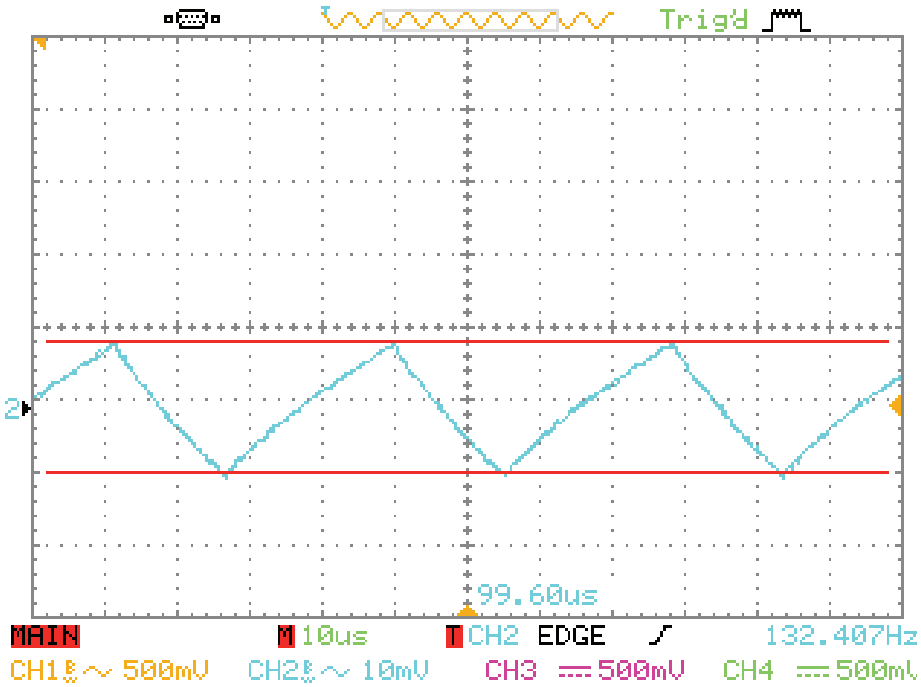
The Basic Topology

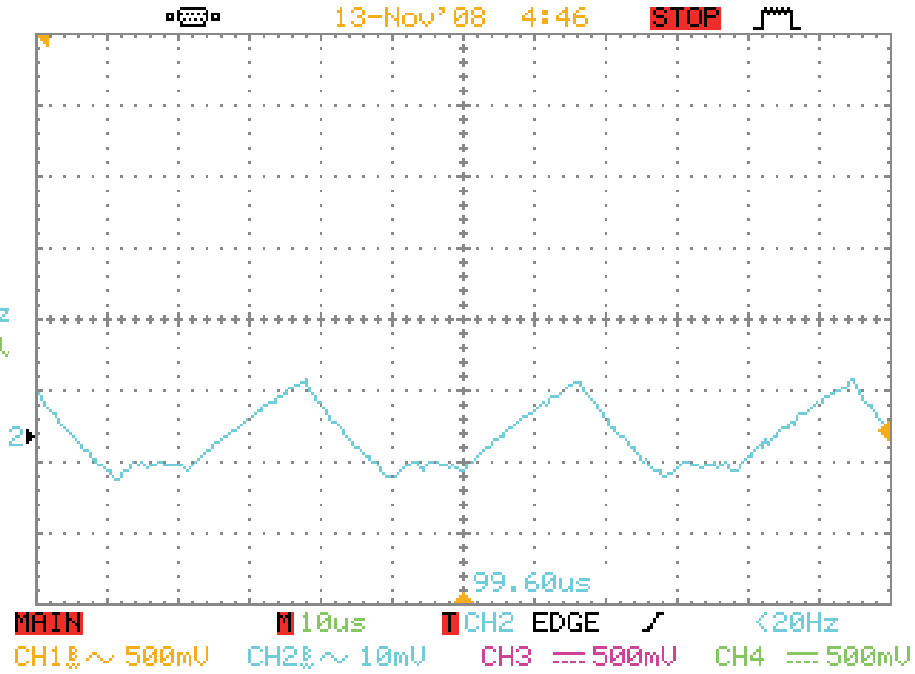


- Two types of Conduction Modes
  - Continuous Conduction Mode (CCM) where Inductor current remains positive throughout the switching period
  - Discontinuous Conduction Mode (DCM) where Inductor current remains zero for some time in the switching period

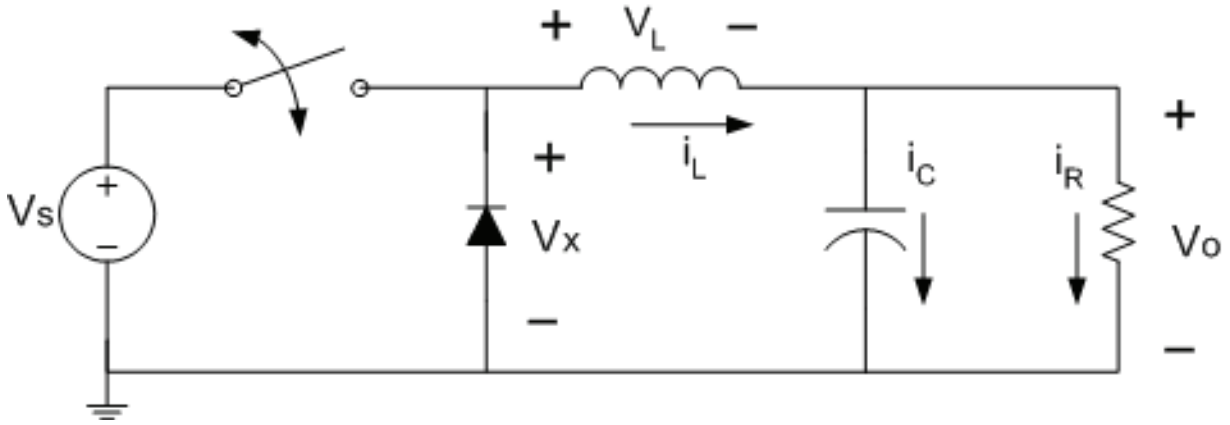


The Basic Topology





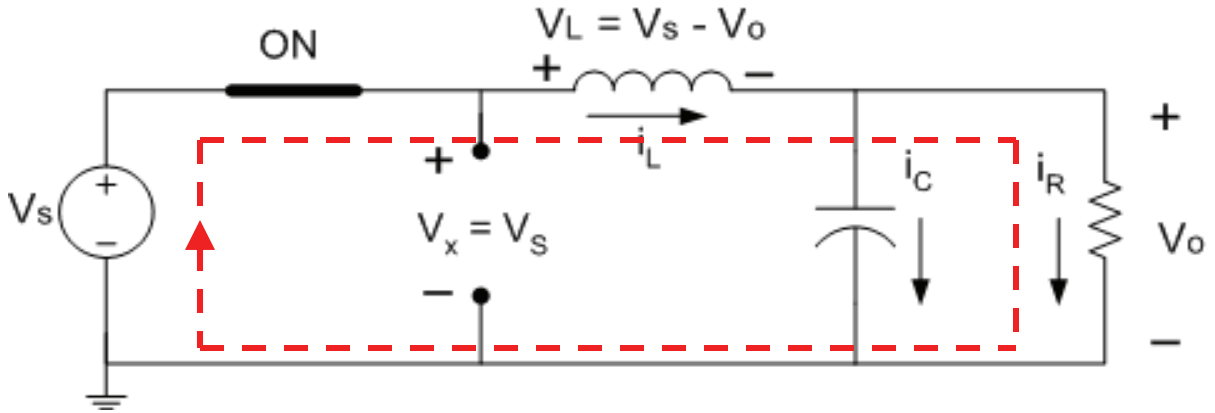
Steady State Analysis of CCM Buck: Transfer Function



- Inductor is the main storage element
- Transfer function may be derived from Volt Second Balance:
  - Average Voltage across Inductor is Zero in steady state
  - Inductor looks like a short to a DC

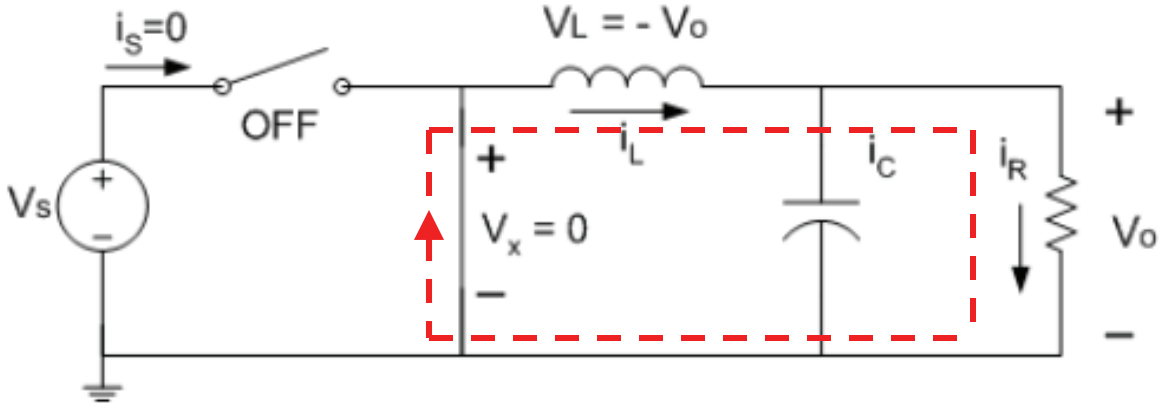
$$\overline{V_L} = v_{Lon} t_{on} + v_{Loff} t_{off} = 0$$

CCM Buck: Transfer Function



- When the switch is **closed** or **ON**
  - Diode is reverse biased since
    - Cathode (at Positive of Input) more positive than Anode (at 0 volt)
  - Voltage across inductor: $v_{Lon} = V_S - V_O$
  - Recall that: $D = t_{on}/T$
  - Then, duration of *on time*, t_{on}: $t_{on} = DT$

CCM Buck: Transfer Function



- When the switch is **OPEN** or **OFF**
  - Inductor discharges causing its voltage to reverse polarity
  - Diode conducts since
    - Anode (0 volt) is more positive than the Cathode (at some negative voltage)
  - Voltage across inductor: $v_{Loff} = -V_O$
  - Recall that: $t_{off} = T - t_{on} = T - DT$ ➔ $t_{off} = (1-D)T$

CCM Buck: Transfer Function

$$v_{Lon}t_{on} + v_{Loff}t_{off} = 0$$

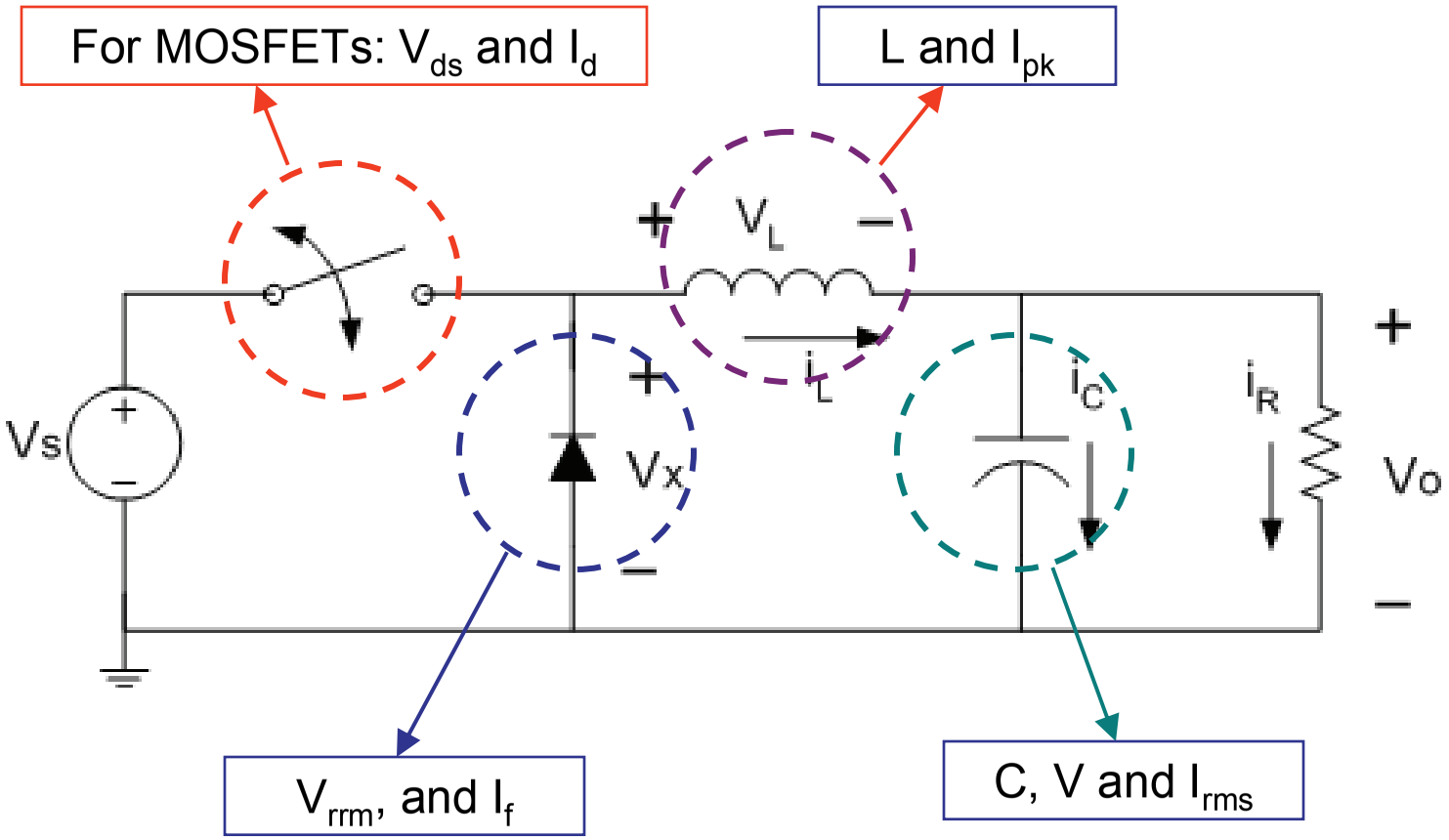
$$(V_S - V_O)DT + (-V_O)(1-D)T = 0$$

$$V_S D - V_O D - V_O + V_O D = 0$$

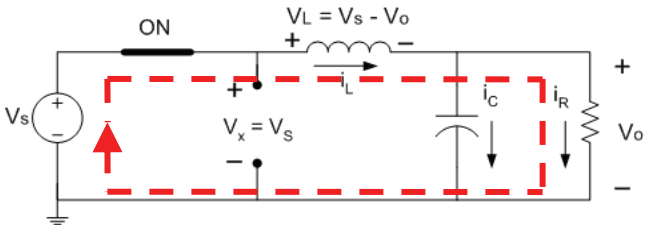
$$\boxed{V_O = DV_S}$$

- Average output voltage is LESS than Input Voltage

CCM Buck: Sizing Components



CCM Buck: Inductor Current

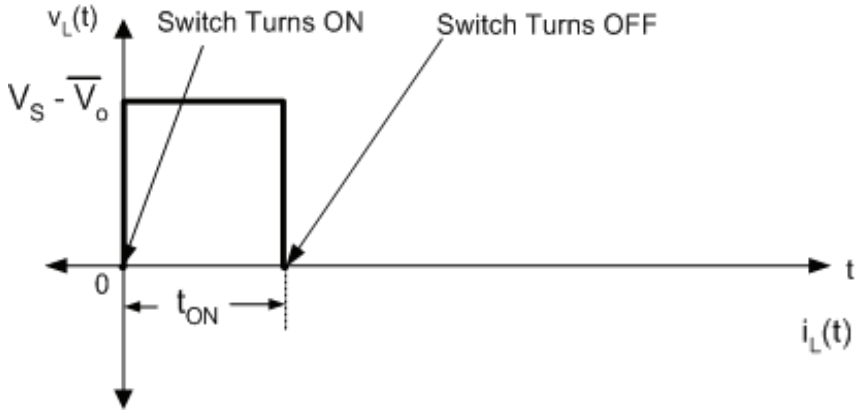


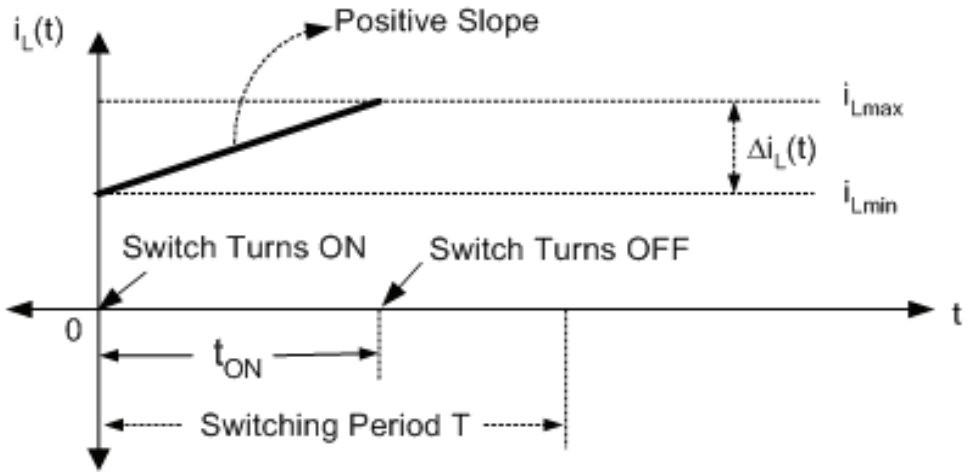
- When switch is ON, Inductor is *charging*:

$$v_L = V_S - V_O = L\frac{di_L}{dt} \Rightarrow \frac{di_L}{dt} = \frac{V_S - V_O}{L} = \oplus$$

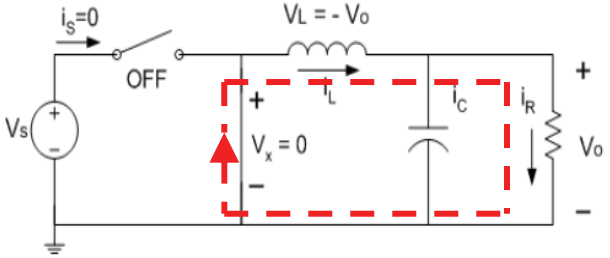
$$\Delta i_{Lon} = \frac{V_S - V_O}{L}\Delta t_{on}$$

$$\Delta i_{Lon} = \frac{V_S - V_O}{L} DT$$





CCM Buck: Inductor Current

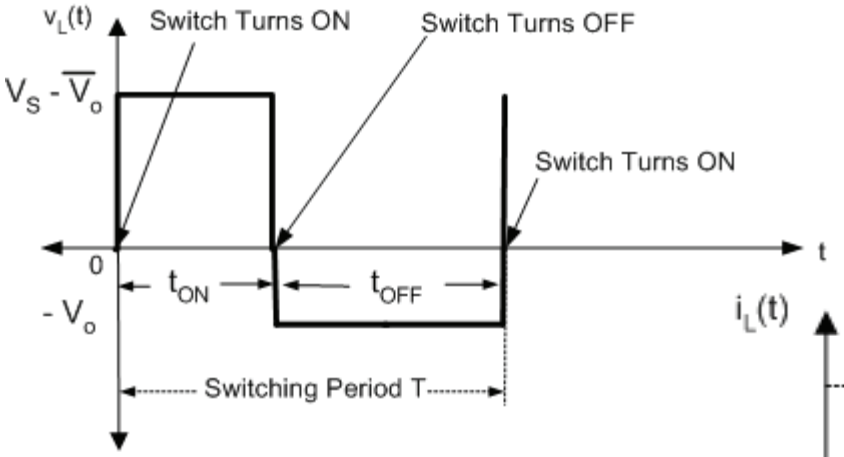


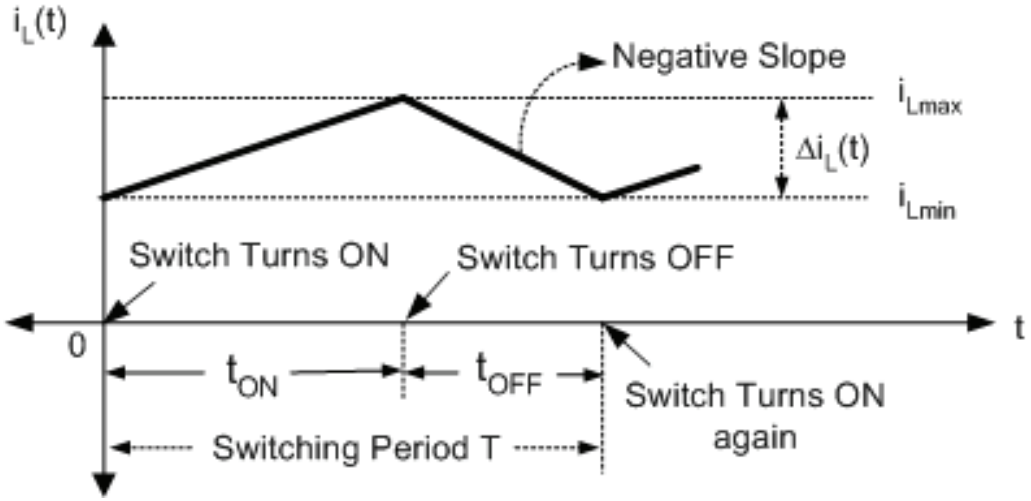
- When switch is OFF, Inductor is *discharging*:

$$v_L = -V_O = L\frac{di_L}{dt} \quad \Rightarrow \quad \frac{di_L}{dt} = \frac{-V_O}{L} = \boxed{-}$$

$$\Delta i_{Loff} = \frac{-V_O}{L}\Delta t_{off}$$

$$\Delta i_{Loff} = \frac{-V_O}{L}(1-D)T$$





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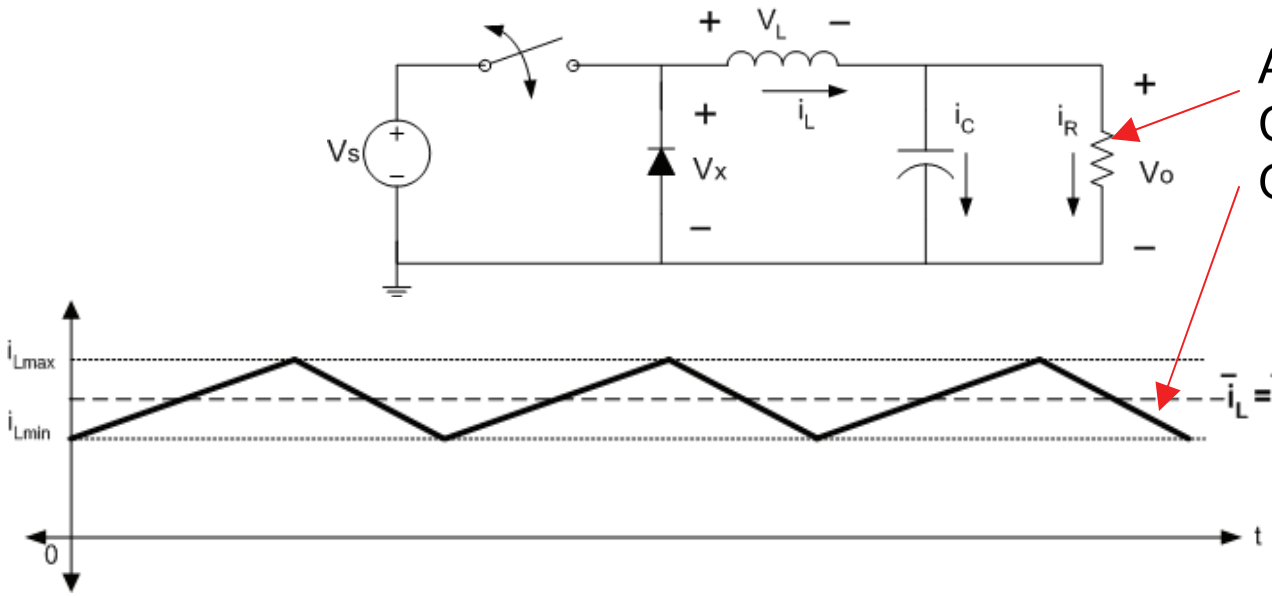


Average Inductor Current = Average Output Current = Vo/R

- We can then determine I_{Lmin} and I_{Lmax}

$$I_{L\min} = \overline{I_L} - \frac{|\Delta i_L|}{2} = \frac{V_0}{R} - \frac{1}{2}\left[\frac{V_0}{L}(1-D)T\right] = V_0\left[\frac{1}{R} - \frac{(1-D)}{2Lf}\right]$$

$$I_{L\max} = \overline{I_L} + \frac{|\Delta i_L|}{2} = \frac{V_0}{R} + \frac{1}{2}\left[\frac{V_0}{L}(1-D)T\right] = V_0\left[\frac{1}{R} + \frac{(1-D)}{2Lf}\right]$$

Sizing Inductor: Critical Inductance

Minimum Load
(output current)

- I_{Lmin} is used to determine the Critical Inductance (Minimum Inductance value at which the inductor current reaches Boundary Conduction Mode)
- Any inductance lower than critical inductance will cause the buck to operate in Discontinuous Conduction Mode
- Requirement is set either by means of maximum Δi_L or by specifying the minimum percentage load where converter still maintains CCM
- Set I_{Lmin} = 0, then solve for L = L_C, then choose L > 1.05*L_C

$$I_{L\min} = 0 = \overline{I_L} - \frac{|\Delta i_L|}{2} = V_0\left[\frac{1}{R_{\max}} - \frac{(1-D)}{2L_C f}\right] \quad \Rightarrow \quad L_C = \frac{(1-D_{\max})R_{\max}}{2f}$$

Sizing Inductor: Critical Inductance

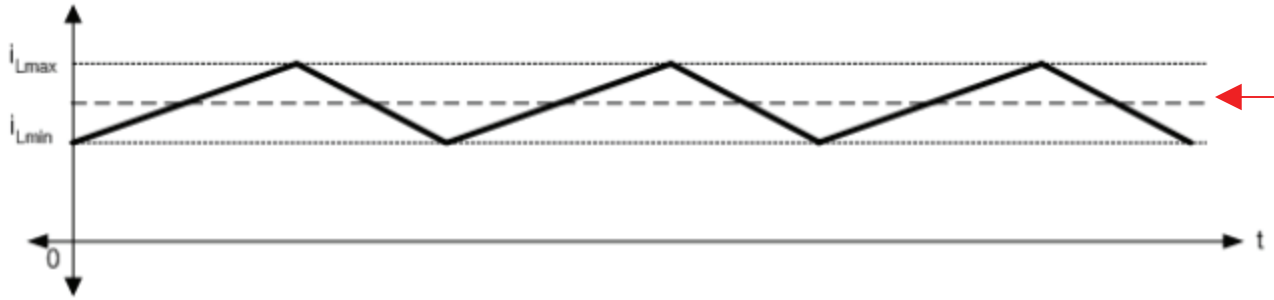
$$L_C = \frac{(1 - D_{\max})R_{\max}}{2f}$$

Calculated at Minimum Input Voltage

- Switching frequency normally chosen by the designer
- The higher the switching frequency, the smaller the required critical inductance, i.e. beneficial for reducing size of Buck

- Calculated at Minimum Output Current = $R_{max} = V_o/I_{omin}$
- Iomin is either given as percentage of load to maintain CCM, e.g. 10% load with CCM
- Or, Iomin is calculated as specified by maximum Δi_L, such that Iomin = $\Delta i_L/2$

Sizing Inductor: Peak Current



Maximum Load
(output current)

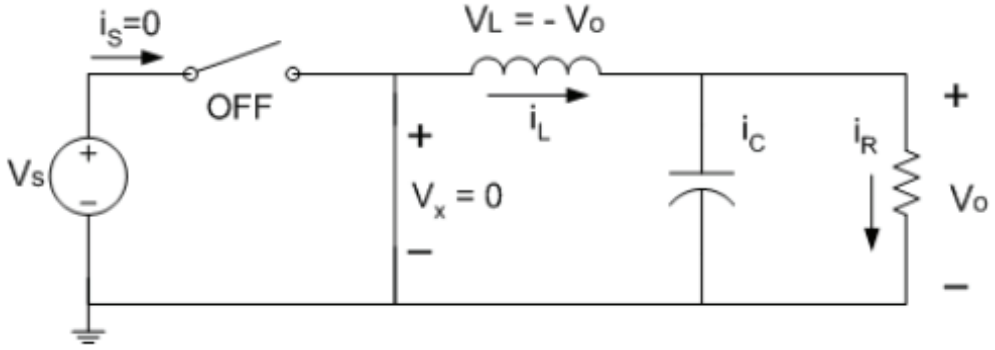
- I_{Lmax} is used to determine peak current rating of Inductor
- Worst case maximum inductor current occurs at maximum load ➔ Maximum output power rating per specified required output voltage

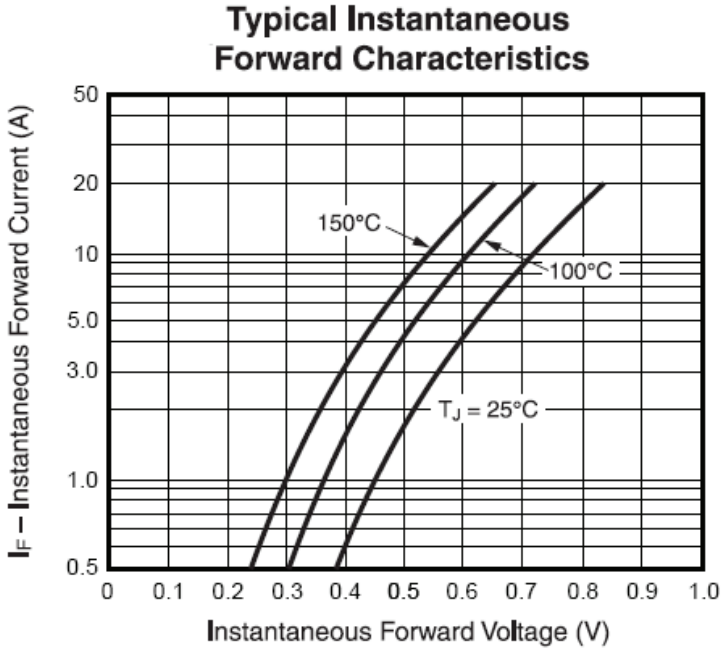
$$I_{L\max} = \overline{I_L} + \frac{|\Delta i_L|}{2} = V_0 \left[\frac{1}{R_{\min}} + \frac{(1 - D_{\min})}{2Lf} \right]$$

Calculated from Highest Input Voltage

Chosen inductance value as discussed previously

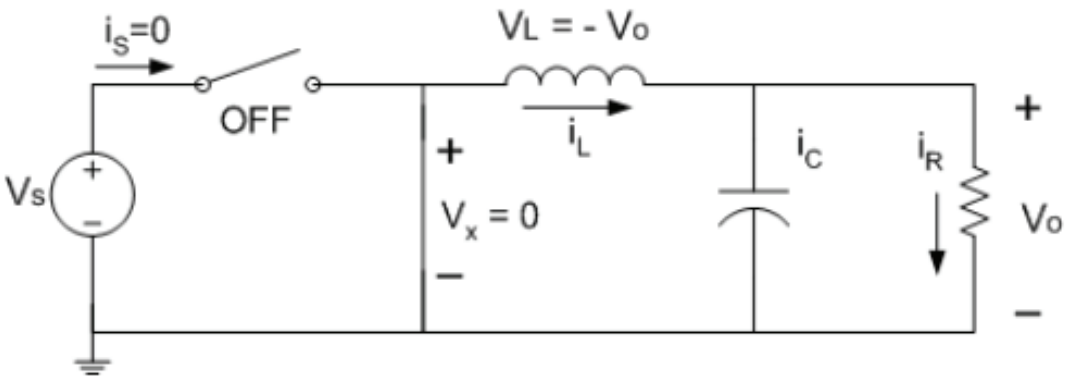
Sizing Switch: Voltage Rating





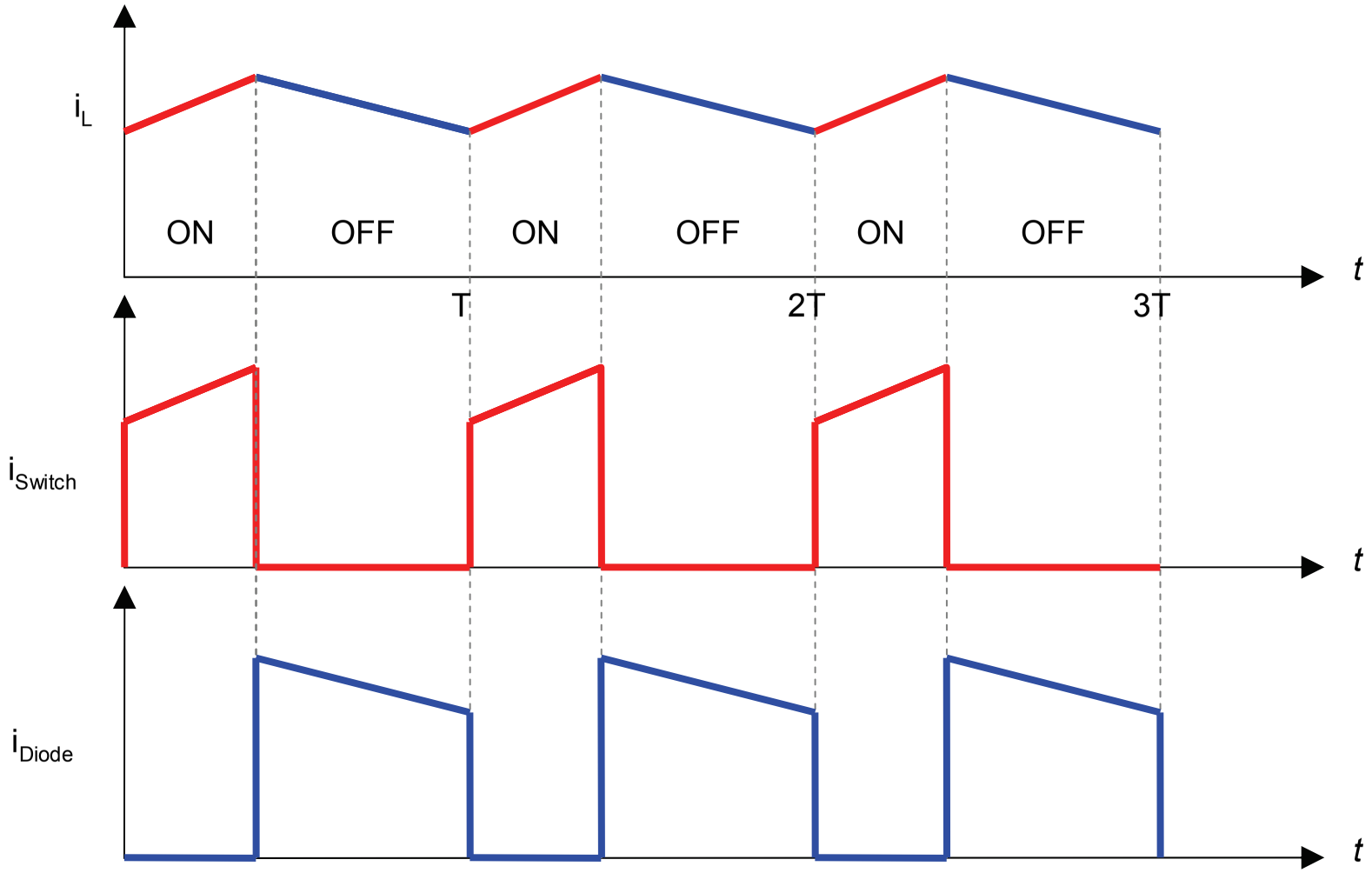
- With ideal diode, the $V_{switch\text{-}max} = V_{inmax}$
- For non-ideal diode, $V_{switch\text{-}max} = V_{inmax} + V_F$ where V_F is the maximum forward drop across the diode (calculated at maximum load current)
- Use safety factor of at least 20%
- For MOSFET, the rating would be V_{DSmax}

Sizing Switch: Current Rating

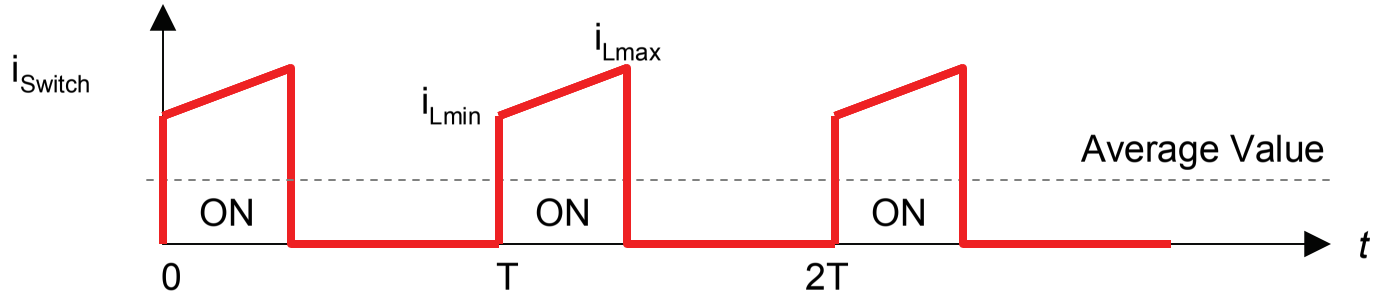


- Switch current rating is calculated based on average value
- Draw switch current waveform and then compute the average value
- By KCL, Inductor Current = Switch Current + Diode Current
- During t_{ON}, Inductor current equals switch current
- During t_{OFF}, Inductor current equals diode current

Switch Current Waveform



Switch Current Waveform for Current Rating



$$\overline{I_{Switch}} = \frac{\left(i_{L\min} + i_{L\max}\right)\cdot t_{on}}{2\cdot T}$$

$$\overline{I_{Switch}} = \frac{\left(\left[i_{L\max} - \Delta i_L\right] + i_{L\max}\right)\cdot DT}{2\cdot T} = \frac{\left(2i_{L\max} - \Delta i_L\right)\cdot D}{2}$$

$$\overline{I_{Switch}} = \left(i_{L\max} - \frac{\Delta i_L}{2}\right)D = \overline{I_L}\cdot D = \overline{I_o}\cdot D$$

$$\overline{I_{Switch-\max}} > \overline{I_{o\max}}\cdot D_{\max}$$

MOSFET Rating Example

14A, 500V, 0.400 Ohm, N-Channel Power MOSFET

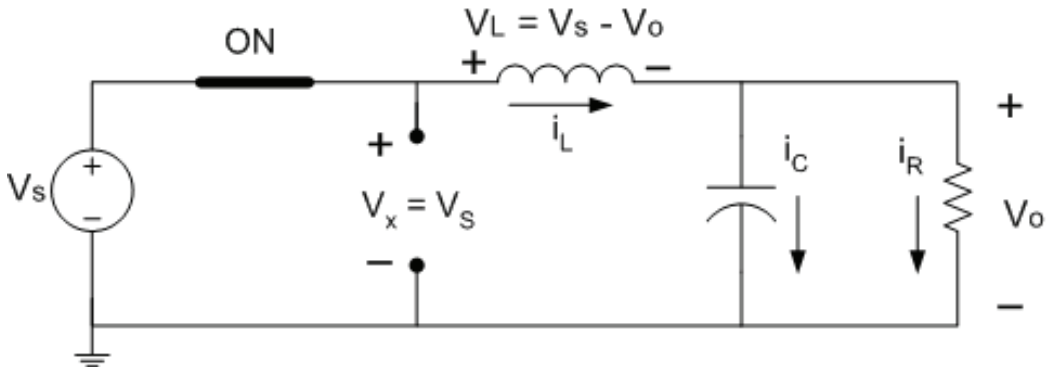
This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17435.

Features

- 14A, 500V
- $r_{DS(ON)} = 0.400\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

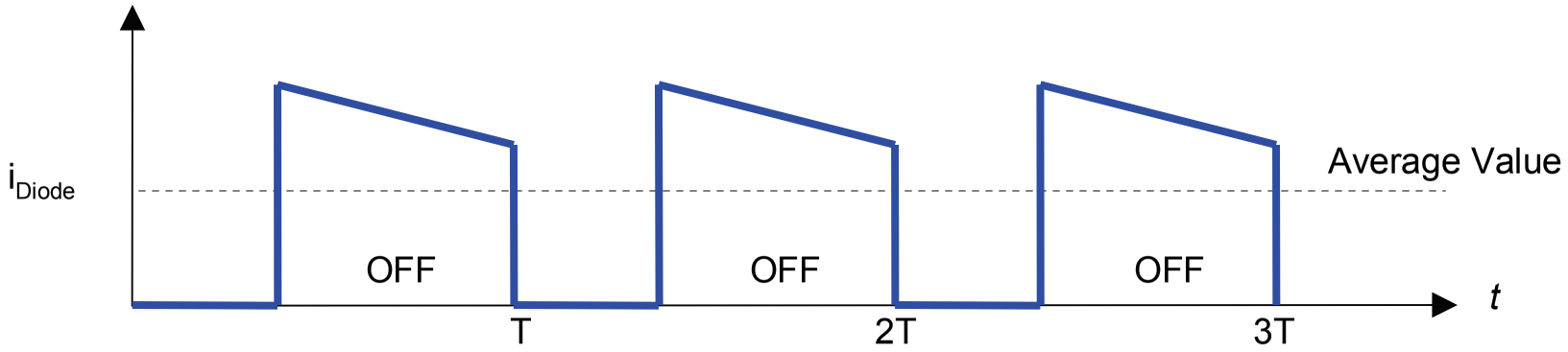
Sizing Diode (Schottky): Voltage Rating



- Known as PIV (Peak Inverse Voltage) or V_{RRM} is the maximum voltage across the diode
- With ideal switch, the $V_{RRM} = V_{inmax}$
- For non-ideal diode, $V_{RRM} = V_{inmax} + V_{SW}$ where V_{SW} is the maximum forward drop across the switch (calculated at maximum load current)
- Allow at least > 20% safety factor

Sizing Diode (Schottky): Current Rating

- Same approach as that for the switch current



$$\overline{I_F} = \frac{\left(i_{L\min} + i_{L\max}\right)\cdot t_{off}}{2\cdot T}$$

$$\overline{I_F} = \frac{\left(\left[i_{L\max} - \Delta i_L\right] + i_{L\max}\right)\cdot(1-D)T}{2\cdot T} = \frac{\left(2i_{L\max} - \Delta i_L\right)\cdot(1-D)}{2}$$

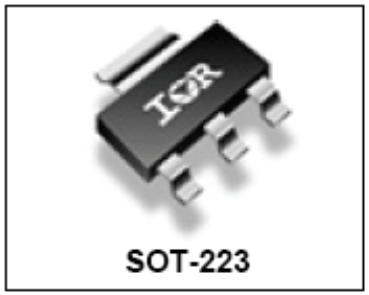
$$\overline{I_F} = \overline{I_L}\cdot(1-D) = \overline{I_o}\cdot(1-D)$$

$$\overline{I_F} > \overline{I_{o\max}}\cdot\left(1-D_{\min}\right)$$

Schottky Diode Rating Example

SCHOTTKY RECTIFIER

2 Amp



SOT-223

Major Ratings and Characteristics

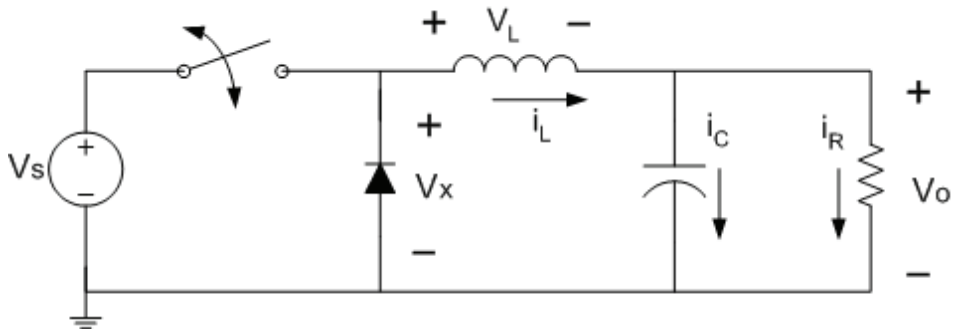
Characteristics			Units
$I_{F(AV)}$	Rectangular waveform	2.0	A
V_{RRM}		45	V
I_{FSM}	@ tp = 5 µs sine	390	A
V_F	@1 Apk, T_J = 125°C (per leg)	0.50	V
T_J	range	-55 to 150	°C

Description/Features

The surface mount Schottky rectifier series has been designed for applications requiring very low forward drop and very small foot prints. Typical applications are in portables, switching power supplies, converters, automotive system, free-wheeling diodes, battery charging, and reverse battery protection.

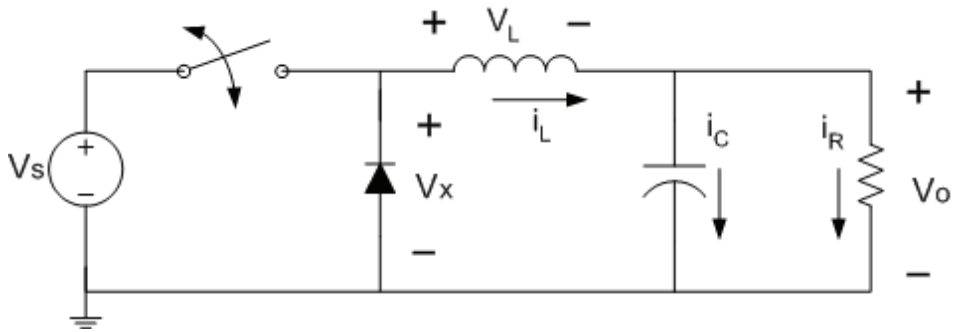
- Small footprint, surface mountable
- Low profile
- Very low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Common cathode

Sizing Output Capacitor: Voltage Rating

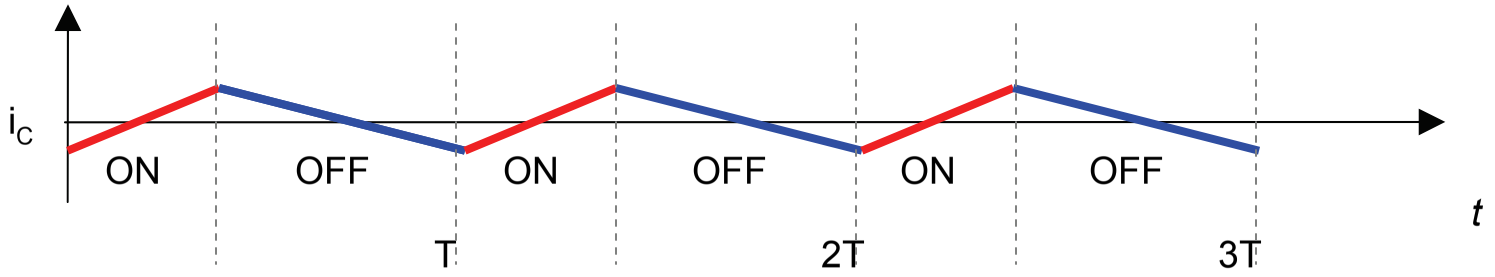


- Capacitor Voltage should withstand the maximum output voltage
  - Ideally: $V_{cmax} = V_o + \Delta V_o/2$
  - More realistic: Capacitor has ESR (Equivalent Series Resistance) which worsens ΔV_o
  - Output voltage ripple contributed by ESR is (ESR * ΔI_L)
  - Suppressing ripple contribution from ESR
    - Reduce ESR (Paralleling Caps, Low ESR Caps)
    - Reduce ΔI_L by increasing L or increasing switching frequency

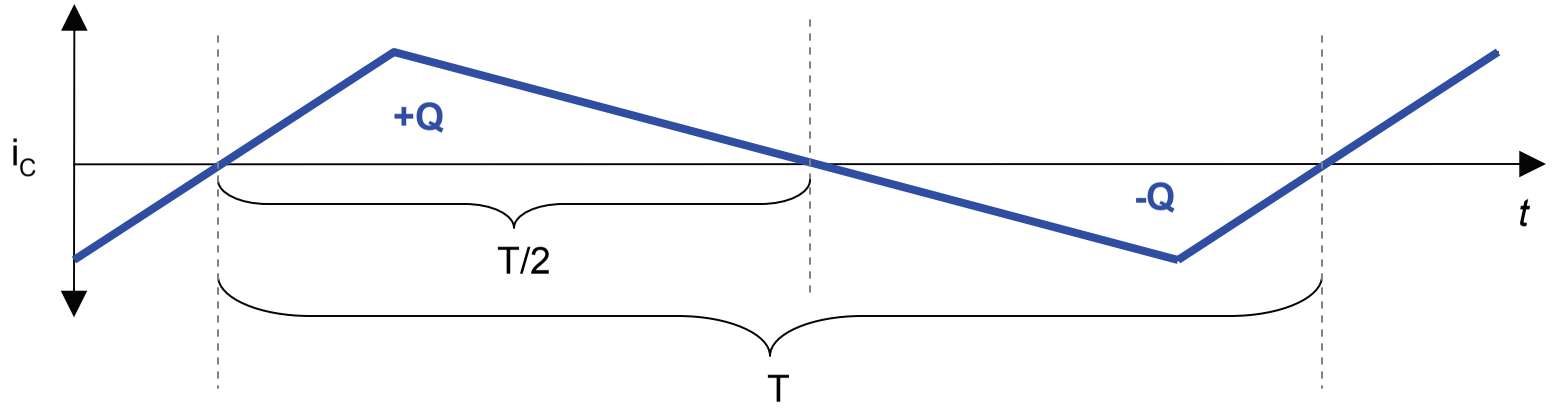
Sizing Output Capacitor: Minimum Capacitance



- The AC component (ripple) of inductor current flows through the capacitor, leaving the average flowing through the load
- Capacitor current waveform will look like:



Sizing Output Capacitor: Minimum Capacitance



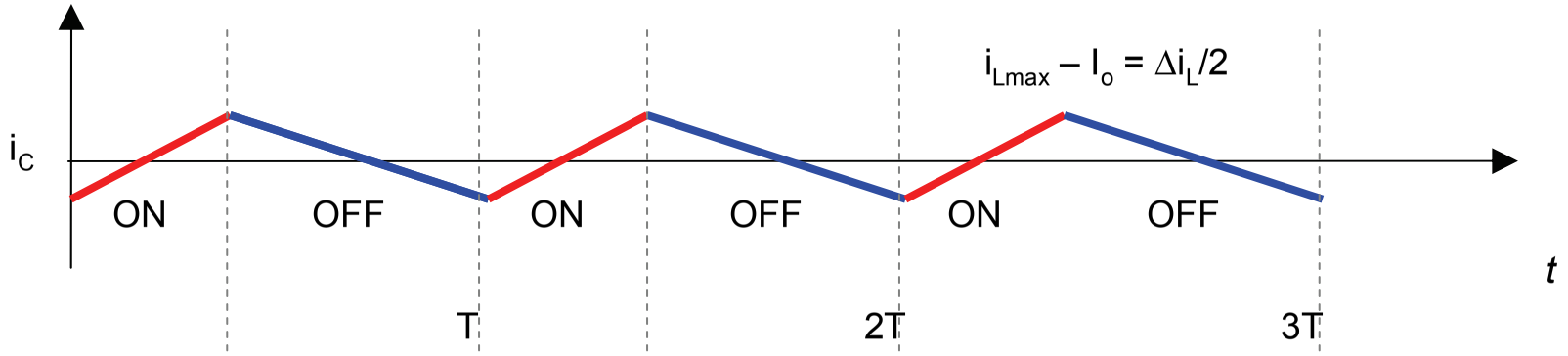
$$q = Area \cdot \Delta = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{\Delta i_L}{8f} = \frac{\frac{V_O}{L}(1-D)T}{8f} = \frac{(1-D)V_O}{8Lf^2}$$

$$q = C \cdot \Delta V_o \Rightarrow C = \frac{q}{\Delta V_o} = \frac{(1-D)V_O}{8Lf^2\Delta V_o} = \frac{(1-D)}{8Lf^2(\Delta V_o / V_O)}$$

$$C = \frac{(1-D_{\min})}{8Lf^2(\Delta V_o / V_O)}$$

Percent V_{opp}

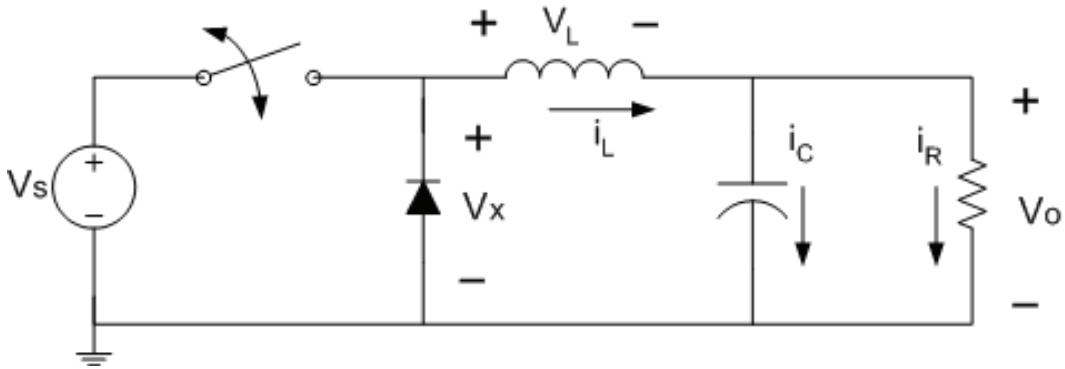
Sizing Output Capacitor: RMS Current Rating



$$i_{Crms} = \frac{i_{Cpk}}{\sqrt{3}} = \frac{\Delta i_L/2}{\sqrt{3}} = \frac{(1-D)V_O}{2\sqrt{3}Lf}$$

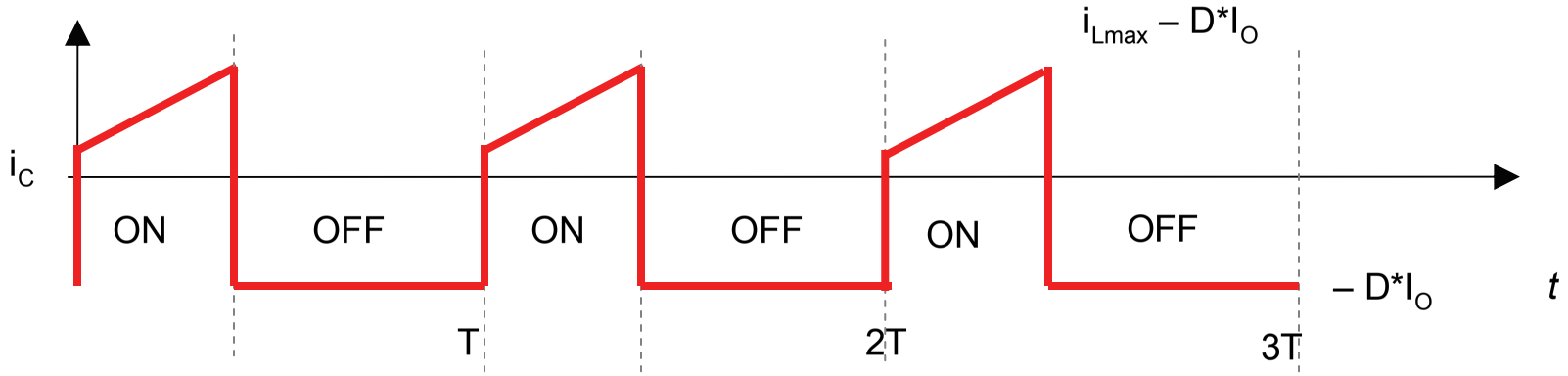
$$i_{Crms} = \frac{(1-D_{\min})V_O}{2\sqrt{3}Lf}$$

Sizing Input Capacitor: Voltage Rating



- Capacitor Voltage should withstand the maximum input voltage
  - Ideally: $V_{cmax} = V_{inmax}$
  - More realistic: Capacitor has ESR (Equivalent Series Resistance) contributes to capacitor loss
  - Minimizing loss contribution from ESR
    - Reduce ESR (Paralleling Caps, Low ESR Caps)

Sizing Input Capacitor: Minimum Capacitance

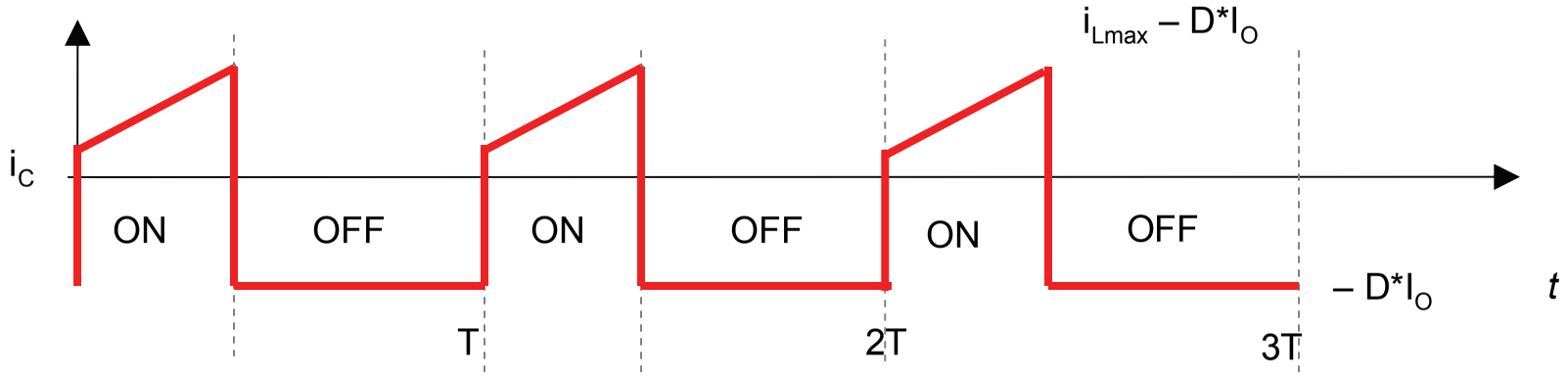


$$q = Area \cdot \square = t_{off} \cdot D \cdot I_O = (1-D)T \cdot D \cdot I_O = \frac{(1-D) \cdot D \cdot I_O}{f}$$

$$q = C \cdot \Delta V_{in} \Rightarrow C = \frac{q}{\Delta V_{in}} = \frac{\frac{(1-D) \cdot D \cdot I_O}{f}}{\Delta V_{in}} = \frac{(1-D) \cdot D \cdot I_O}{f \Delta V_{in}}$$

$$C = \frac{(1-D) \cdot D \cdot I_{O\max}}{f \Delta V_{in}}$$

Sizing Input Capacitor: RMS Current Rating



$$I_{Crms} = \sqrt{\left(I_{Switch-rms}\right)^2 - \left(I_{switch-avg}\right)^2}$$

$$I_{Crms} = \sqrt{\left(I_o\sqrt{D}\sqrt{\left(1+\left[\frac{\Delta i_L}{2\cdot I_o}\right]\right)}\right)^2 - \left(D\cdot I_o\right)^2}$$

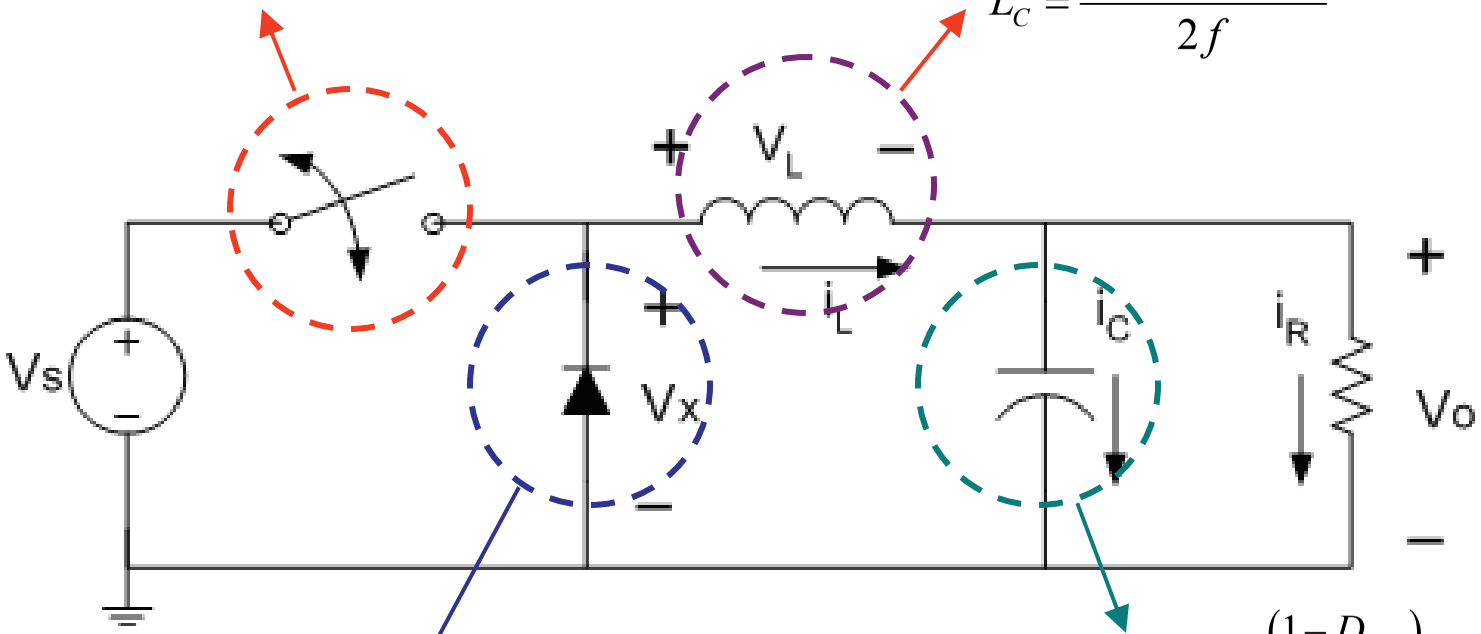
To Summarize

$$\overline{I_{Switch-\max}} > \overline{I_{o\max}} \cdot D_{\max}$$

$V_{switch\text{-}max} = V_{inmax}$

$$I_{L\max} = V_0 \left[\frac{1}{R_{\min}} + \frac{(1-D_{\min})}{2Lf} \right]$$

$$L_C = \frac{(1-D_{\max})R_{\max}}{2f}$$



$$\overline{I_F} > \overline{I_{o\max}} \cdot (1-D_{\min})$$

$V_{RRM} = V_{inmax}$

$$C = \frac{(1-D_{\min})}{8Lf^2(\Delta V_o/V_O)}$$

$V_{cmax} = V_o + \Delta V_o/2$

$$i_{Crms} = \frac{(1-D_{\min})V_O}{2\sqrt{3}L}$$

Simple Buck Design: 12V to 2.5V 1A

Given:

$Vs := 12V$ $Vo := 2.5V$ $Iomax := 1A$

$Ioccm := 0.1A$ $\%Vo := 1\%$ $f := 50kHz$

Solution:

$$D := \frac{Vo}{Vs} \qquad D = 0.208$$

Inductor:

$$Lcrit := \frac{(1 - D)}{2 \cdot f} \cdot \frac{Vo}{Ioccm} \qquad Lcrit = 1.979 \times 10^{-4} H$$

Choose: $L := 200 \cdot 10^{-6} H$

$$ILmax := Iomax + \frac{(1 - D) \cdot Vo}{2 \cdot L \cdot f} \qquad ILmax = 1.099\ A$$

$$\Delta IL := \frac{(1 - D) \cdot Vo}{L \cdot f} \qquad \Delta IL = 0.198\ A$$

Simple Buck Design: 12V to 2.5V 1A

MOSFET:

$Vds := Vs$ $\quad Vds = 12\,V$

$Id := D \cdot Iomax$ $\quad Id = 0.208\,A$

Diode:

$Vrrm := Vs$ $\quad Vrrm = 12\,V$

$If := (1 - D) \cdot Iomax$ $\quad If = 0.792\,A$

Capacitor:

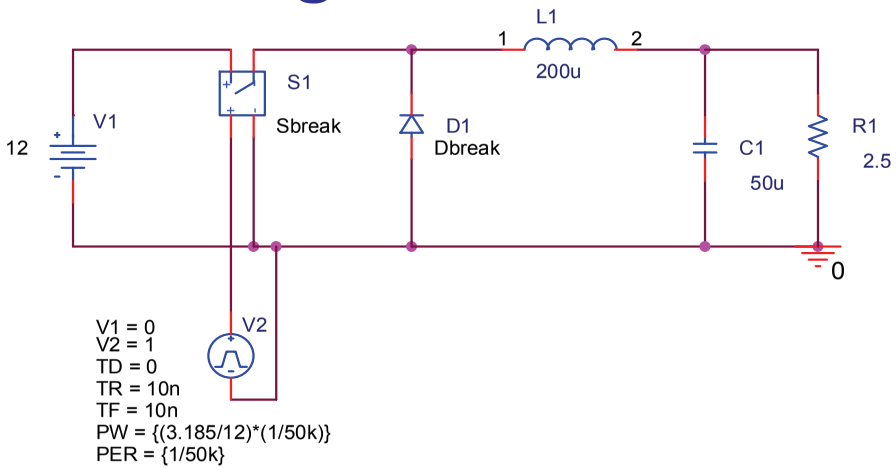
$$Vcmax := Vo + \frac{\%Vo \cdot Vo}{2} \qquad Vcmax = 2.513\,V$$

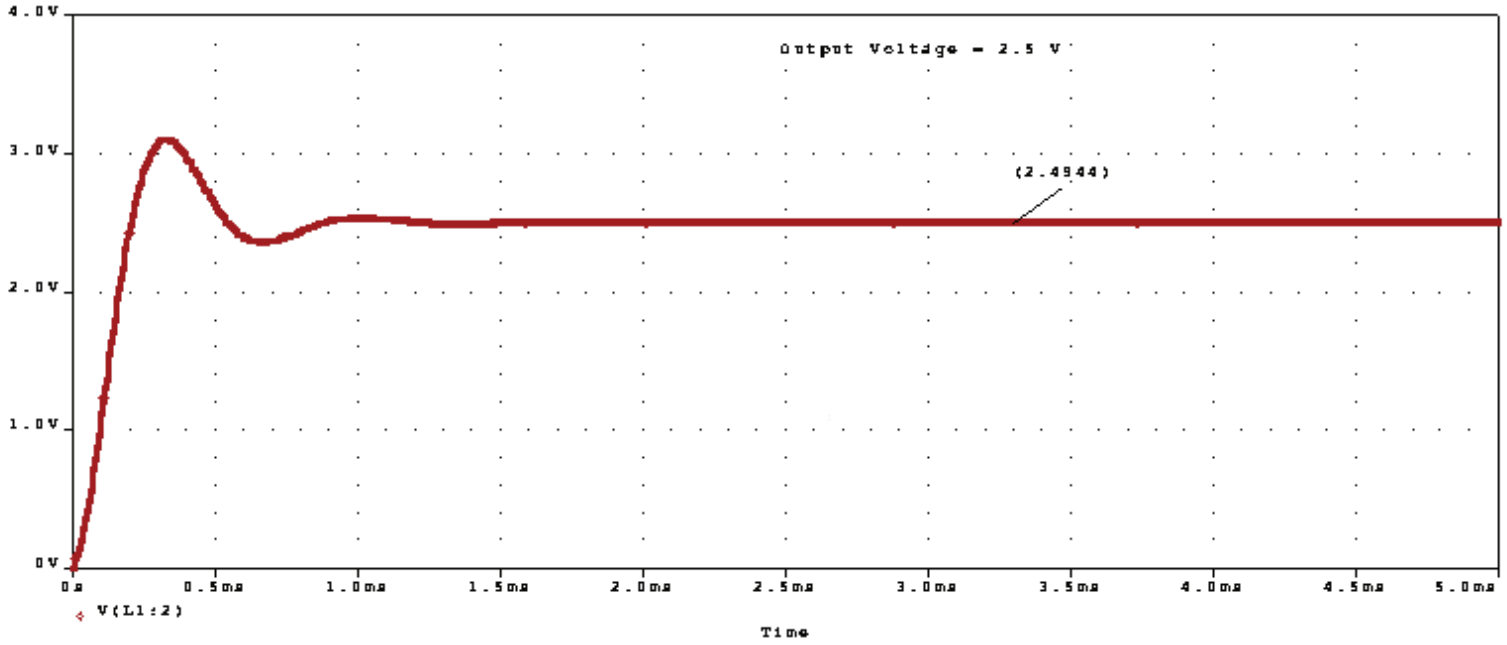
$$C := \frac{(1 - D)}{8 \cdot L \cdot f^2} \cdot \frac{1}{\%Vo} \qquad C = 1.979 \times 10^{-5}\,F$$

Choose $Co := 50 \cdot 10^{-6}\,F$

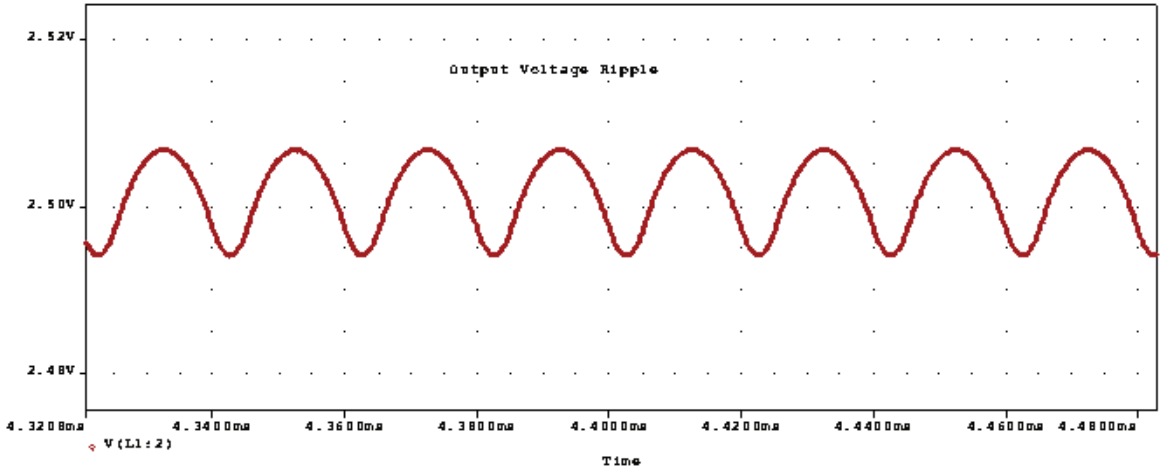
$$\%Vo := \frac{(1 - D)}{8 \cdot L \cdot f^2 \cdot Co} \qquad \%Vo = 0.396\,\%$$

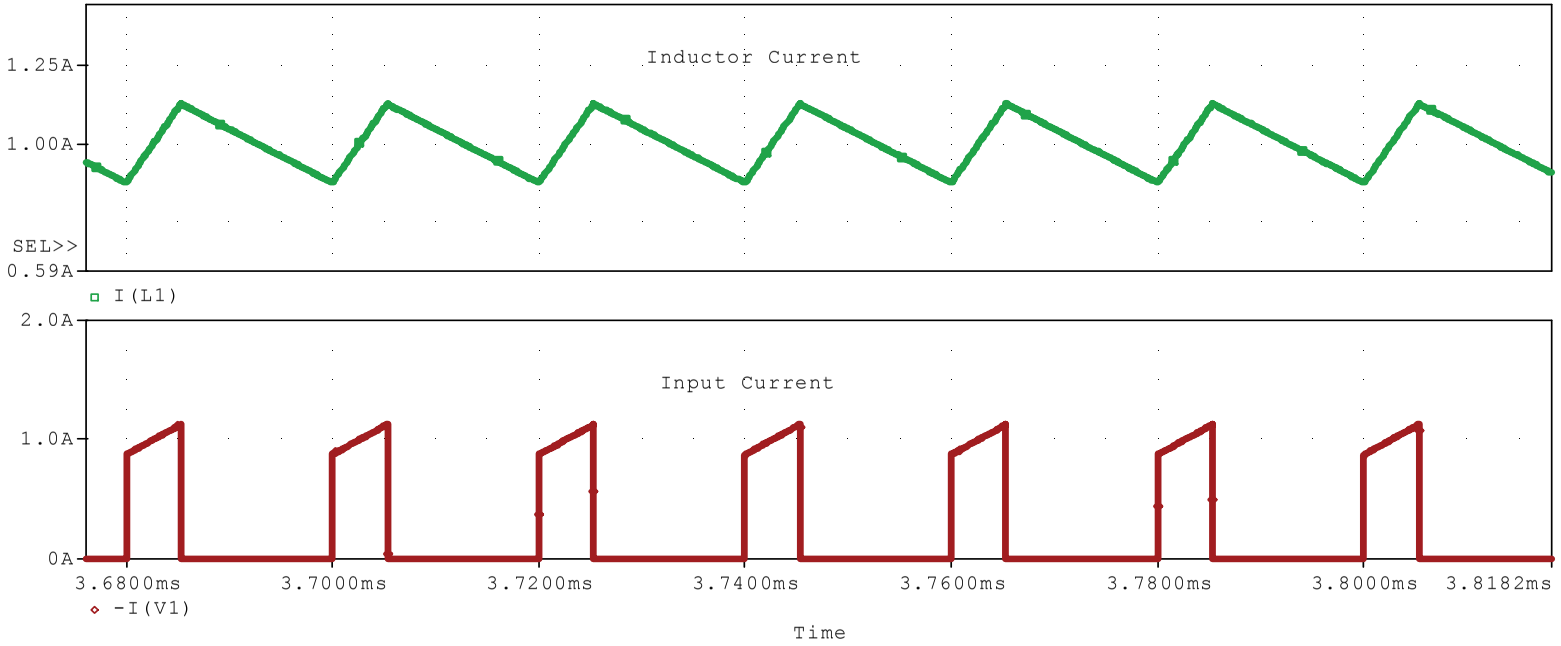
Simple Buck Design: 12V to 2.5V 1A





Simple Buck Design: 12V to 2.5V 1A



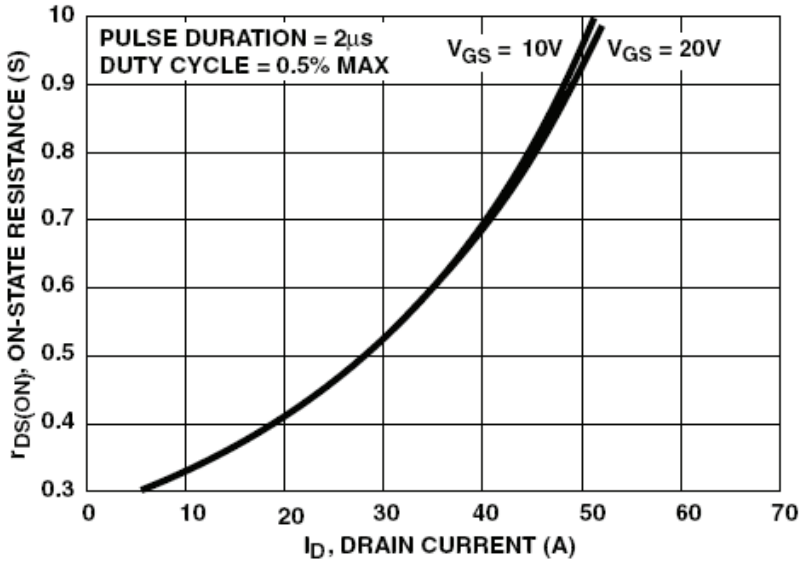


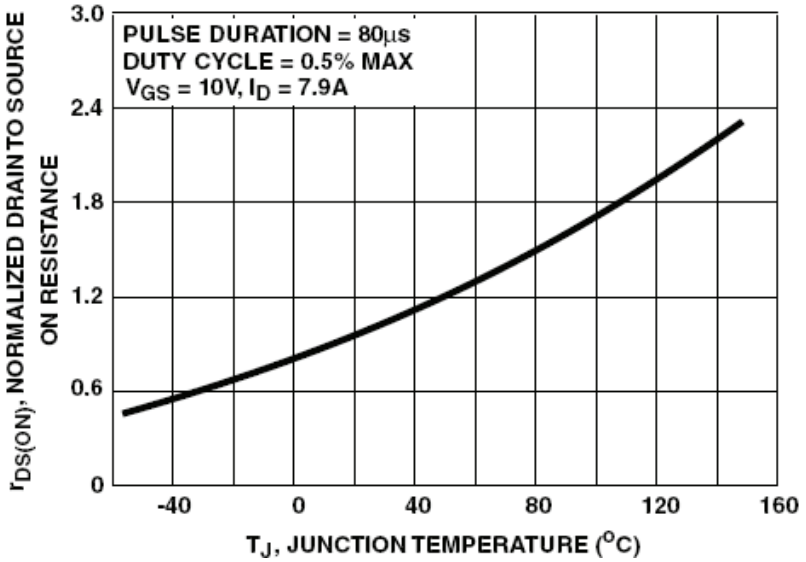
Non-ideal Buck: Loss Considerations

- When efficiency estimation is required in the design, losses in Buck circuit should be considered
- Several major losses to consider:
  - Static loss of MOSFET
  - Switching loss of MOSFET
  - MOSFET Gate Drive Losses
  - Static loss of diode
  - Switching loss of diode
  - Inductor's copper loss
  - Capacitor's ESR loss

Static Loss of MOSFET

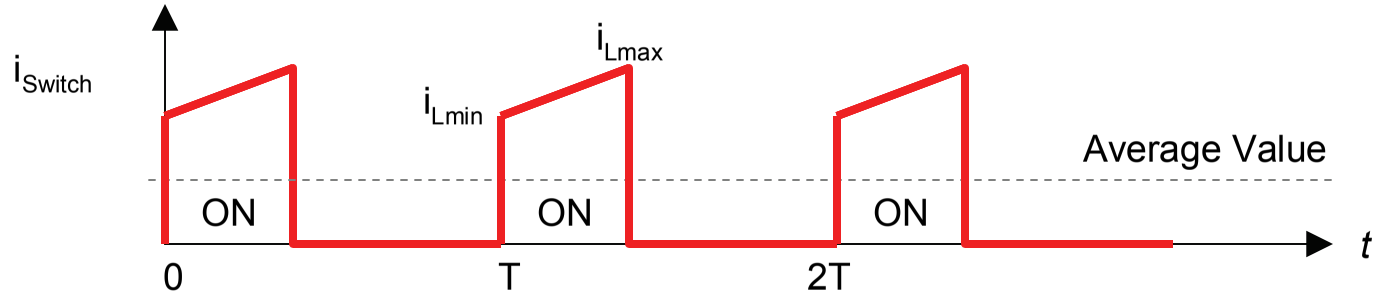
- With MOSFET, its on resistance R_{DSon} directly impacts the static loss
- R_{DSon} depends on applied gate voltage and MOSFET's junction temperature





Static Loss of MOSFET

- Recall, switch current:



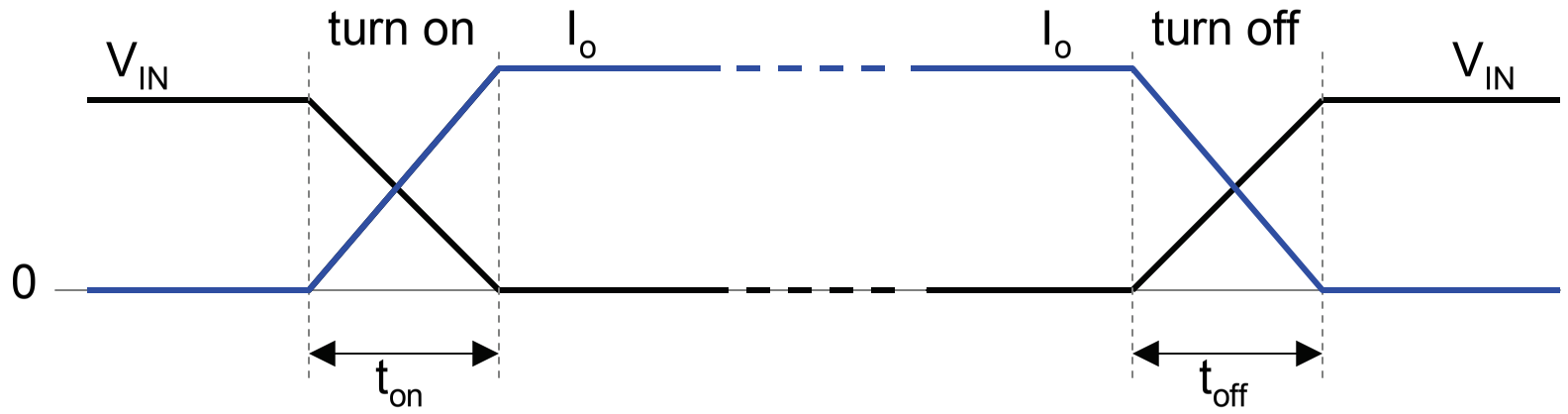
- Static loss for MOSFET with R_{DSon}:

$$P_{static} = I_{switch-rms}^2 \cdot R_{DSon}$$

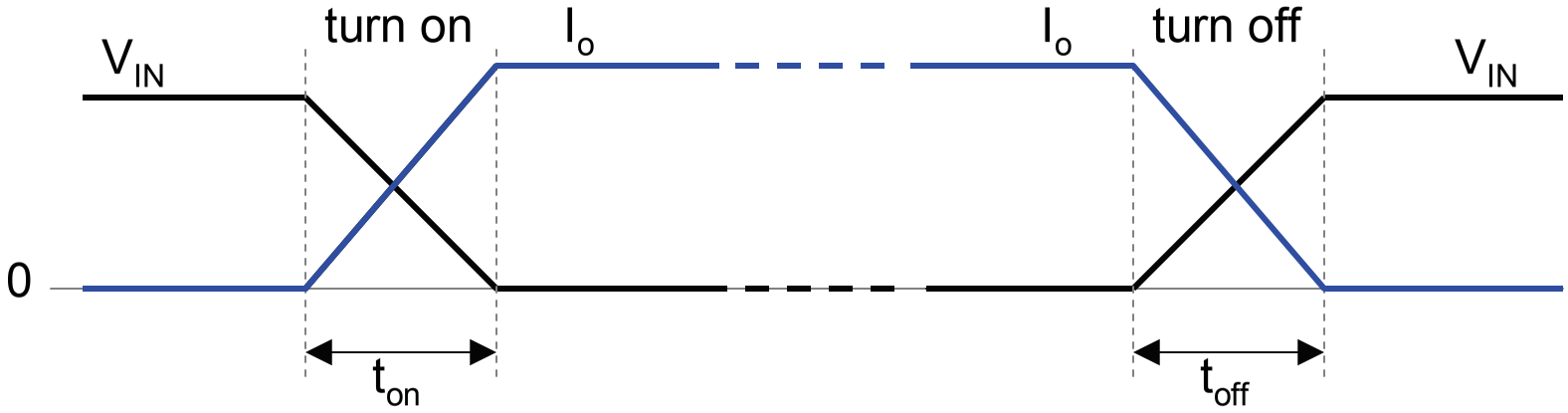
$$P_{static} = \left(I_o \sqrt{D} \sqrt{\left(1 + \left[\frac{\Delta i_L}{2 \cdot I_o} \right] \right)} \right)^2 \cdot R_{DSon}$$

Switching Loss of MOSFET

- The switching loss depends on how the voltage and current overlaps
- May be approximated with a scenario where voltage and current start moving simultaneously and reach their endpoints
- The overlap causes power loss (V x I)
- Will assume to occur both at turn-on and turn-off transitions



Switching Loss of MOSFET



$$P(t_{on}) = \frac{I_o V_{in} t_{on}}{6T} \qquad P(t_{off}) = \frac{I_o V_{in} t_{off}}{6T}$$

$$P_{switching} = P(t_{on}) + P(t_{off}) = \frac{I_o V_{in} t_{on}}{6T} + \frac{I_o V_{in} t_{off}}{6T}$$

$$P_{switching} = \frac{I_o V_{in}}{6T}\left(t_{on} + t_{off}\right)$$

Switching Loss of MOSFET & Gate Drive Loss

- When MOSFET is off, its output capacitance C_{oss} is being charged ➔ translates to loss

$$P_{Coss} = \frac{1}{2} C_{OSS} V_{in}^2 f$$

- Gate drive loss comes from the total gate charge Q_{gate} and the gate drive voltage V_{gate} used

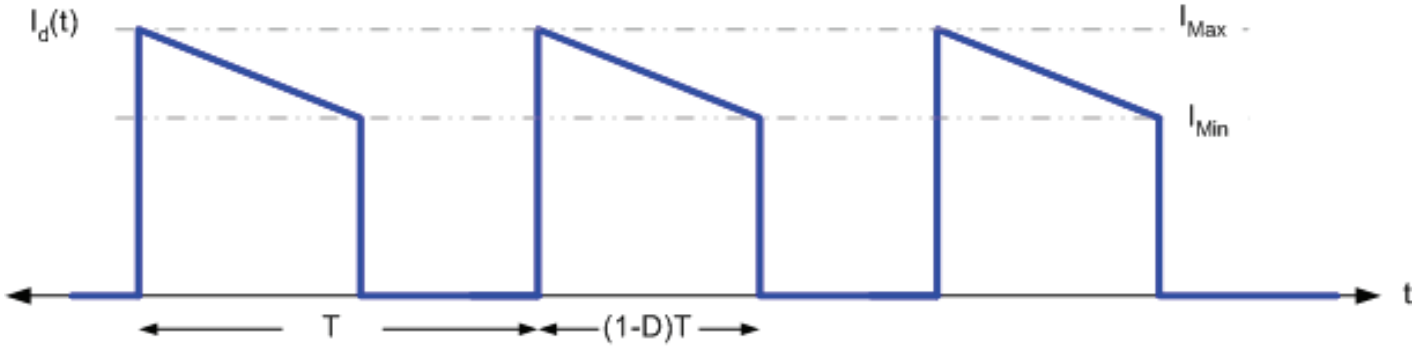
$$P_{gate} = \frac{1}{2} Q_{gate} V_{gate} f$$

Static Loss of Diode: Forward Loss

- Losses that occur during diode's fully on (forward loss) and fully off (reverse loss) conditions
- Forward loss come from the product of diode's forward voltage (V_F) and forward current (I_F), in addition to the rms loss due to diode dynamic resistance, r_d

$$P_{forward} = V_f \cdot \overline{I_f} + \widetilde{I_f^2} \cdot r_d$$

Static Loss of Diode: Forward Loss



From datasheet

$$P_{forward} = V_f \cdot \overline{I_f} + \widetilde{I_f^2} \cdot r_d$$

$$\overline{I_f} = (1-D) \cdot \overline{I_o}$$

$$\widetilde{I_f} = \sqrt{\frac{(1-D)}{3}\left[I_{\max}^2 + I_{\min}^2 + I_{\max} \cdot I_{\min} \right]}$$

Static Loss of Diode: Reverse Loss

- Loss occurs when the diode is in the fully off or non-conducting condition

$$P_{reverse} = V_r \cdot I_r \cdot (1 - D)$$

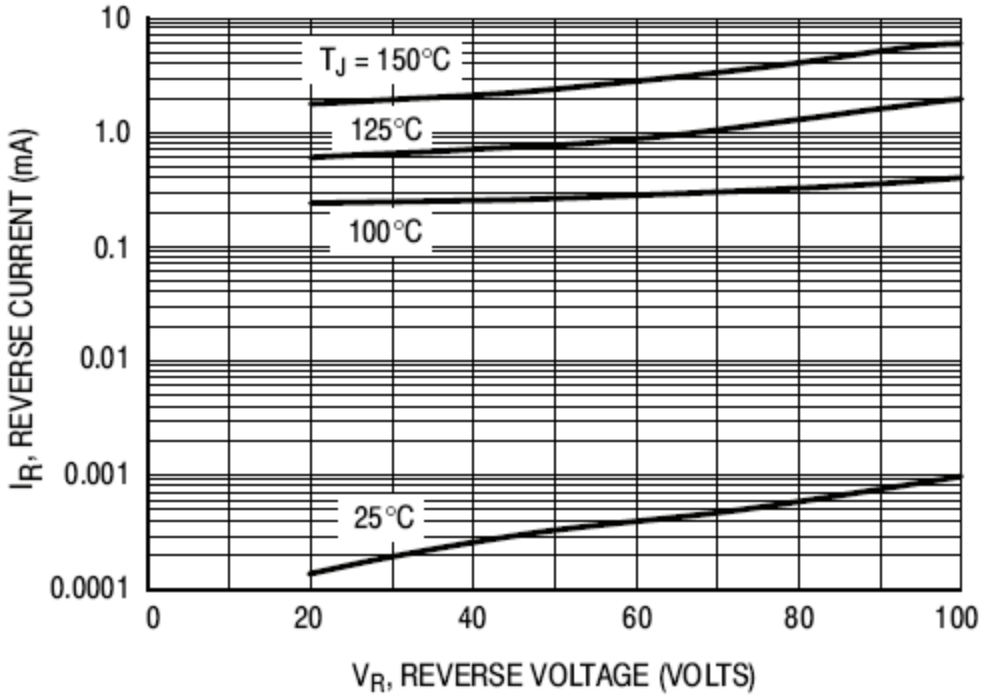
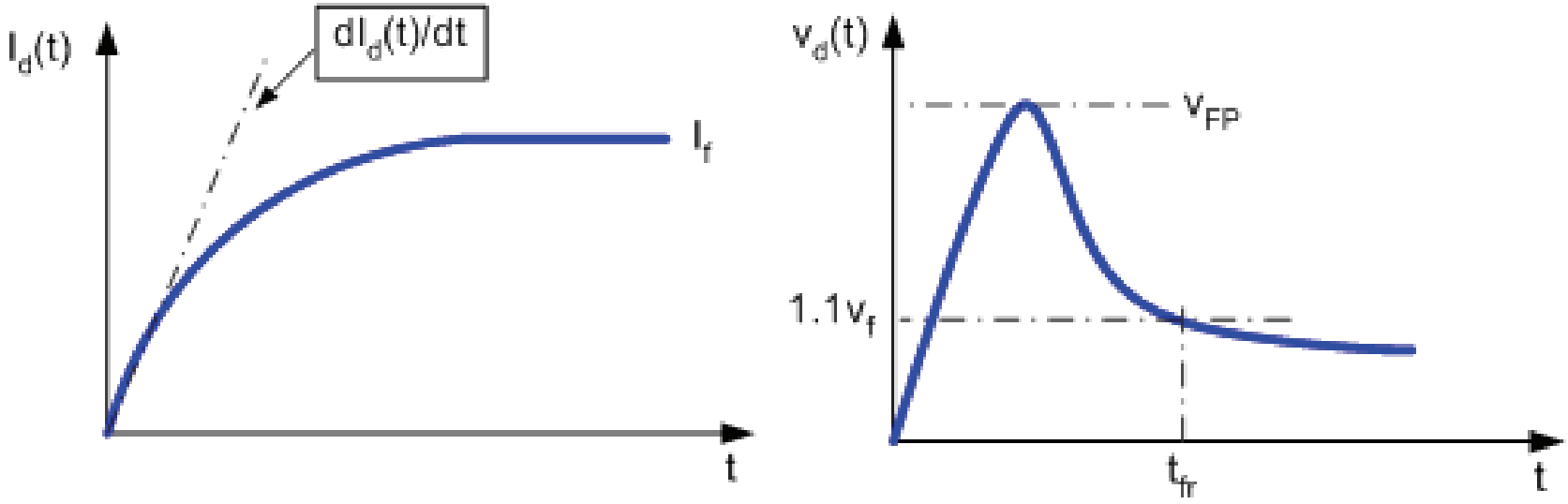


Figure 2. Typical Reverse Current Per Diode

Switching Loss of Diode: Turn On Loss

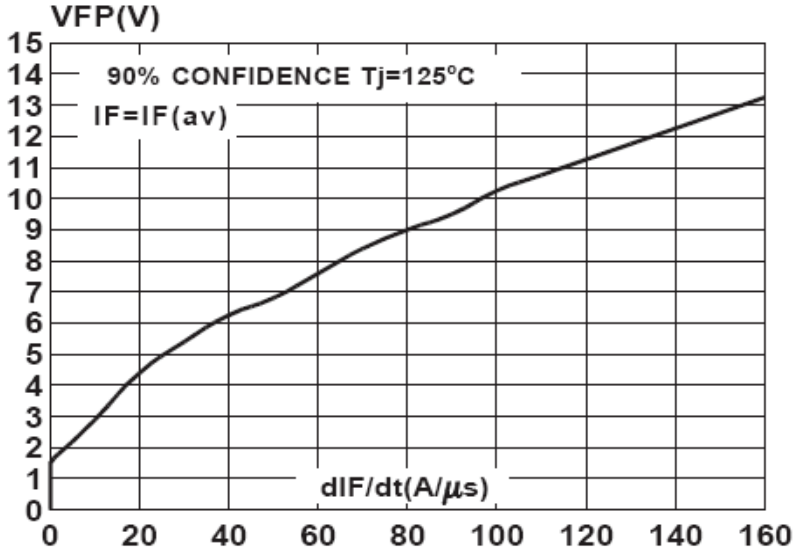
- The switching behavior at turn-on is characterized by a low value of peak forward voltage (V_{FP}) and forward recovery time (t_{fr})



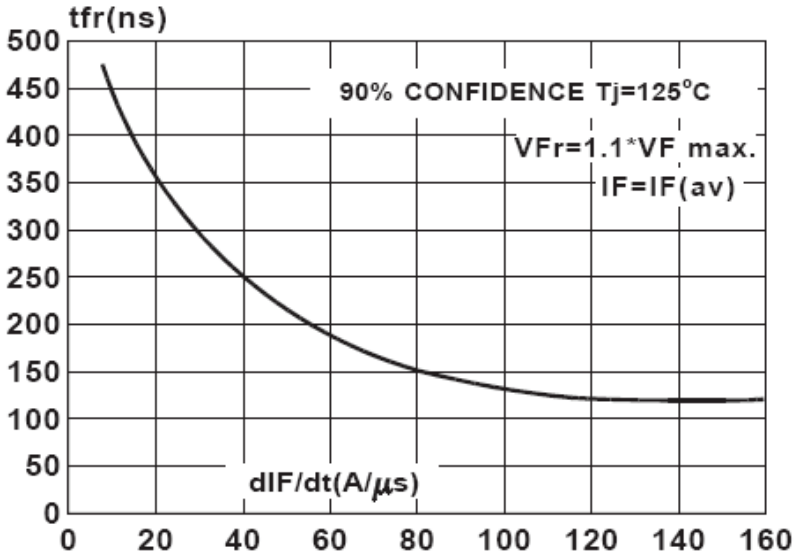
$$P_{ON} = 0.4 \cdot \left(V_{FP} - V_f\right) \cdot t_{fr} \cdot I_f \cdot f$$

Switching Loss of Diode: Turn On Loss

- Both V_{FP} and t_{fr} are normally plotted against $dI_d(t)/dt$ in the datasheet, whereas $dI_d(t)/dt$ itself is also available in the datasheet for a given set of conditions



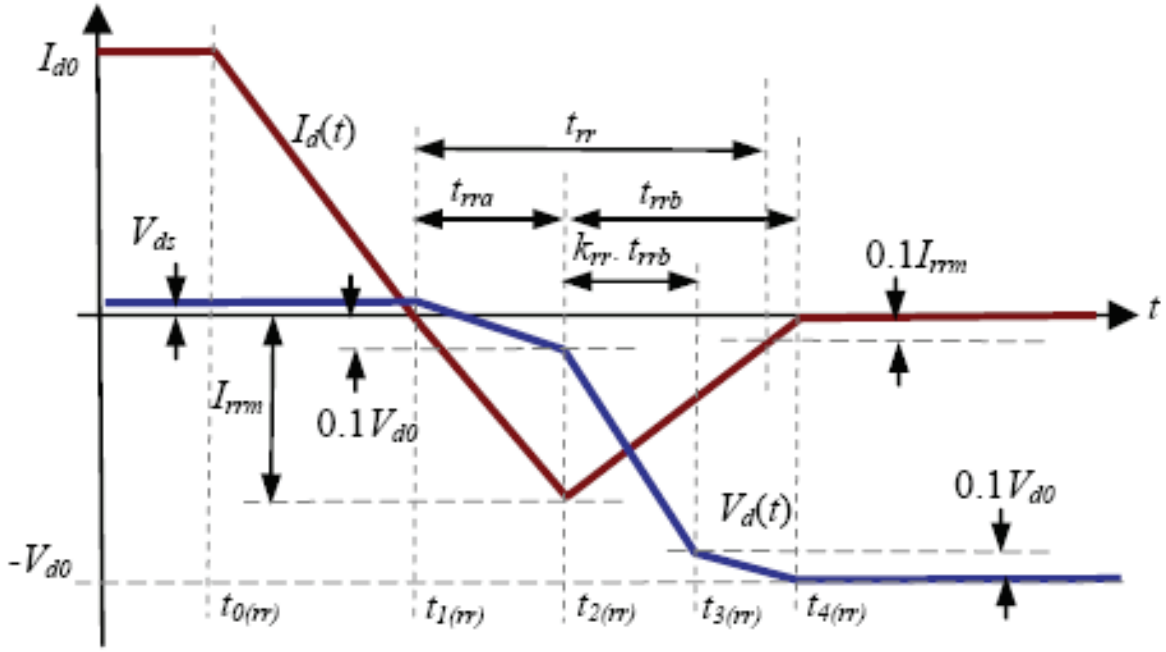
TURN-ON SWITCHING



Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{fr}	Forward recovery time	Tj = 25°C I_F = 8 A, dI_F/dt = 64 A/µs measured at, 1.1 × $V_F$max			500	ns
V_{Fp}	Peak forward voltage	Tj = 25°C I_F = 8A, dI_F/dt = 64 A/µs			10	V

Switching Loss of Diode: Turn Off Loss

- Turn-off loss constitutes appreciable switching losses due to the overlapping of diode voltage and current at turn-off with its associated reverse-recovery time



$$t_{rra} = I_{rrm} \Big/ \left(\frac{I_{d0}}{\left. \frac{dI_d}{dt} \right|_{t_{1(rr)}}} \right)$$

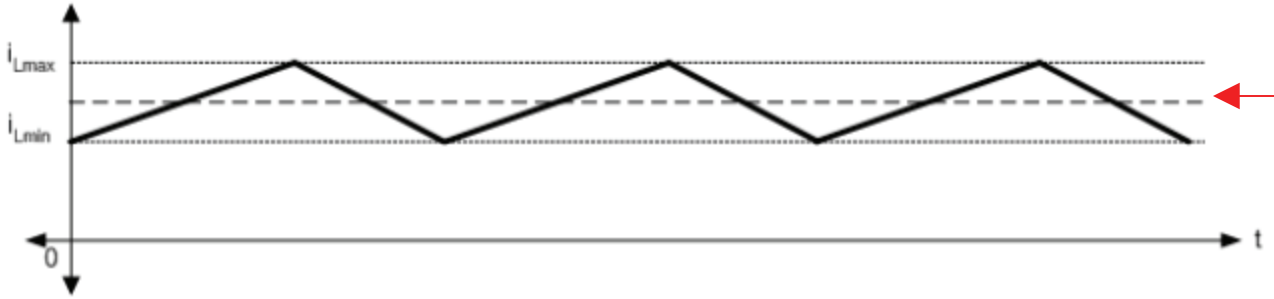
$$t_{rrb} = 1.11 \cdot \left(t_{rr} - t_{rra} \right)$$

$$\left[t_{2rr}, t_{3rr} \right] = k_{rr} \cdot t_{rrb}$$

$$P_{off} = 0.5 V_{ds} I_{d0} \left(\frac{I_{d0}}{\left. \frac{dI_d}{dt} \right|_{t_{1(rr)}}} \right) + 0.033 V_{d0} I_{rrm} t_{rra} + V_{d0} I_{rrm} \left(0.467 - 0.433 k_{rr} + 0.15 k_{rr}^2 \right) t_{rrb}$$

Inductor's Copper Loss

- Inductor's winding is made of copper and hence inherently it will have resistive loss



- With inductor's dc resistance of R_L and inductor's rms current, the copper loss of inductor is:

$$P_L = \tilde{I}_L^{\,2} R_L$$

$$\tilde{I}_L = I\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_L}{2I}\right)^2}$$

Inductor's Core Loss

- Factors affecting core loss: switching frequency F, temperature, flux swing B
- General form:

Core Loss = Core Loss/Unit Volume x Volume

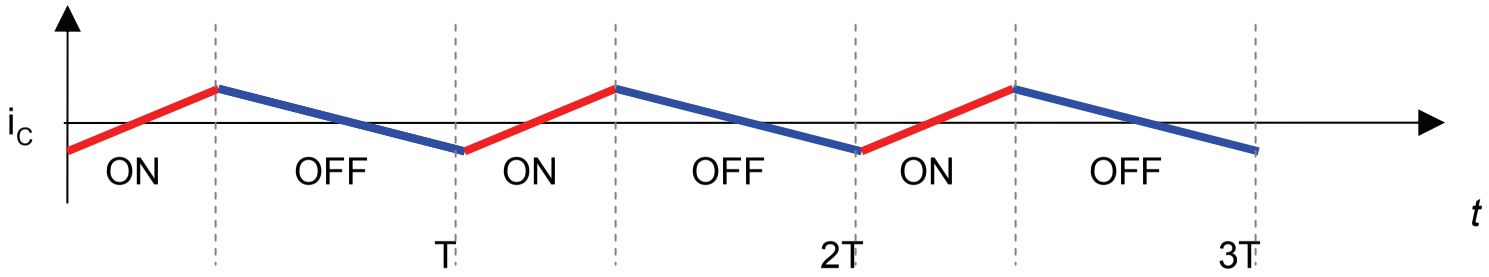
Where,

Core Loss/Unit = $k1 \times B^{k2} \times F^{k3}$

- Constants k1, k2, and k3 are normally provided by the core manufacturers

Capacitor's ESR Loss

- Real world capacitors posses ESR (Equivalent Series Resistance)
- ESR can measured with, for example, Capacitor Wizard



- Loss due to Capacitor's ESR is:

$$P_{ESR} = \widetilde{I}_C^{\,2} ESR$$

$$\widetilde{I}_C = \frac{\Delta i_L}{2\sqrt{3}}$$

Buck Design With Losses

Buck Design with Losses

Taufik

Maximum Output Power: $Pomax := 120W$

Nominal Output Voltage: $Vonom := 12V$

Nominal Input Voltage: $Vinom := 24V$

Switching Frequency: $Fs := 250kHz$

Minimum Percent CCM: $Iccm := 10\%$

Maximum Ripple Percentage: $Vopp := 2\%$

$\mu \equiv 1 \cdot 10^{-6}$

$m \equiv 1 \cdot 10^{-3}$

Design Calculations and Sizing Components:

Nominal Duty Cycle:

$$D := \frac{Vonom}{Vinom} = 0.5$$

Critical Inductance:

$$Lc := \frac{(1 - D) \cdot \left(\frac{Vonom^2}{Iccm \cdot Pomax} \right)}{2 \cdot Fs} = 12.000H \cdot \mu$$

Choose L > Lc $Lo := 200\mu H$ with assumed DC resistance of: $RLo := 100m\Omega$

Peak Inductor Current:

$$ILopk := Vonom \cdot \left[\frac{1}{\frac{Vonom^2}{Pomax}} + \frac{(1 - D)}{2 \cdot Lo \cdot Fs} \right] = 10.06A$$

Switch Voltage: $Vswmax := Vinom = 24V$

Switch Current:

$$Id := D \cdot \frac{Pomax}{Vonom} = 5A$$

Choose MOSFET IRF7471 40V 10A Rdson 13mO

Diode Vrrm: $Vrrm := Vinom = 24V$

Diode Forward Current: $If := (1 - D)\cdot\frac{Pomax}{Vonom} = 5A$

Choose MBR3040

Capacitor Voltage Rating: $Vcap := Vonom + \left(\frac{Vopp\cdot Vonom}{2}\right) = 12.12V$

Capacitance: $Co := \frac{(1 - D)}{8\cdot Lo\cdot Fs^2\cdot Vopp} = 250\times 10^{-3} F\cdot\mu$

RMS Current Rating: $Icaprms := \frac{(1 - D)\cdot Vonom}{2\sqrt{3}\cdot Lo\cdot Fs} = 0.035A$

Choose a 25V 50uF capacitor

Power Loss Calculations

MOSFET Loss Calculations: $Rdson := 13m\cdot\Omega$ $n := 0..11$

$Load_n :=$

0.01
5
10
20
30
40
50
60
70
80
90
100

Output Current Array: $Io_n := \left(\frac{\frac{Load_n}{100}\cdot Pomax}{Vonom}\right)$

Static Loss:

$Idrms_n := Io_n\cdot\sqrt{D}\cdot\sqrt{1 + Iccm}$

$Pmos1_n := \left(Io_n\cdot\sqrt{D}\cdot\sqrt{1 + Iccm}\right)^2 Rdson$

Switching Loss: $ton1 := 12ns$ $toff1 := 15ns$ $Coss := 700pF$ $Qg := 21nC$

$$Pmos2_n := \frac{Io_n \cdot Vinom \cdot (ton1 + toff1) \cdot Fs}{6}$$

$Vg := 12V$

$$Pcoss := \frac{1}{2} \cdot Coss \cdot Vinom^2 \cdot Fs = 0.05W$$

$$Pgate := \frac{1}{2} \cdot Qg \cdot Vg \cdot Fs = 0.032W$$

$$Pmostot_n := Pmos1_n + Pmos2_n + Pcoss + Pgate$$

Diode Loss Calculations

$$Ifavg_n := Io_n \cdot (1 - D)$$

From Diode Datasheet:

$Vf_n :=$

0.02V
0.46V
0.5V
0.58V
0.61V
0.64V
0.66V
0.68V
0.7V
0.71V
0.73V

Dynamic Resistance:

$$Rd := \frac{0.62V - 0.4V}{4A - 0.5A} = 0.063\Omega$$

Peak to peak Inductor Current

$$\Delta IL := \frac{Vonom \cdot (1 - D)}{Lo \cdot Fs} = 0.12A$$

$$Ifrms_n := \sqrt{\frac{(1 - D)}{3} \cdot \left[\left(Io_n + \frac{\Delta IL}{2} \right)^2 + \left(Io_n - \frac{\Delta IL}{2} \right)^2 + \left(Io_n - \frac{\Delta IL}{2} \right) \cdot \left(Io_n + \frac{\Delta IL}{2} \right) \right]}$$

$$Pd1_n := Vf_n \cdot Ifavg_n + \left(Ifrms_n \right)^2 Rd$$

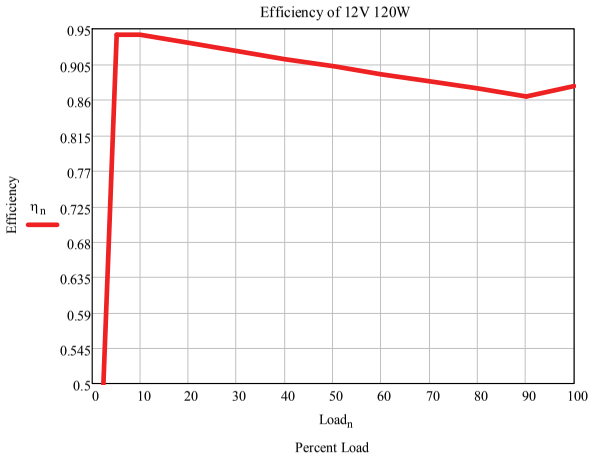
From Datasheet: $Vr := Vinom - Vonom$ $Ir := 0.00015A$

$$Pd2 := Vr \cdot Ir \cdot (1 - D) = 0.001W$$

Assume: $tfr := 500ns$ $Vfp := 10V$

$$Pd3_n := 0.4 \cdot \left(Vfp - Vf_n\right) \cdot tfr \cdot Ifavg_n \cdot Fs$$

$$Pdtot_n := Pd1_n + Pd2 + Pd3_n$$



Inductor Loss Calculation

$$ILrms_n := Io_n \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta IL}{2 \cdot Io_n}\right)^2} \qquad PLo_n := \left(ILrms_n\right)^2 \cdot RLo$$

Capacitor Loss Calculation

Assume: $ESR := 150m \cdot \Omega$

$$Icrms := \frac{\Delta IL}{2\sqrt{3}} = 0.035A \qquad Pc := Icrms^2 \cdot ESR$$

Total Loss Calculation

$$Ptotal_n := Pmostot_n + Pdtot_n + PLo_n + Pc \qquad Po_n := Vonom \cdot Io_n$$

Efficiency ==> $$\eta_n := \frac{Po_n}{Po_n + Ptotal_n}$$

Another Example

DESIGN EXAMPLE: BUCK REGULATOR

The following example illustrates the design of an ideal Buck Regulator in Continuous Conduction Mode which is maintained down to 10% of the full load current of 5A

Given Parameters

Input Voltage	$Vin := 48V$
Output Voltage	$Vo := 12V$
Switching Frequency	$fs := 100kHz$
Full Load Current	$Iomax := 10A$
Percent minload-CCM	$ccm := 10\%$
Output Vpp-ripple	$\Delta Vo := 10 \cdot 10^{-3} V$

Hence $Ts := \frac{1}{fs}$

Parameter dan Design Calculations

The ideal ON-time of the switch $ton := \frac{Vo}{Vin} \cdot Ts$ $ton = 2.5 \times 10^{-6} s$

Minimum Output Current while still maintaining CCM

$Iomin := ccm \cdot Iomax$ $Iomin = 1\,A$

Determine the Critical Inductance $Lc := \frac{Vin - Vo}{2 \cdot Iomin} \cdot ton$ $Lc = 4.5 \times 10^{-5} H$

Choose a bigger inductor (say 10% bigger) $L := 1.1 \cdot Lc$ $L = 4.95 \times 10^{-5} H$

With the chosen Inductor, the minimum output current can now be recomputed

$Iomin := \frac{Vin - Vo}{2 \cdot L} \cdot ton$ $Iomin = 0.909A$

<u>Next we will determine ILmin and ILmax at Full load</u>

Initial Guesses for ILmin and ILmax $ILmin := 1A$ $ILmax := 1A$

Given TWO equations in terms of ILmin and ILmax

Given

$$\frac{ILmax + ILmin}{2} = Iomax$$

$$ILmax - ILmin = \frac{Vin - Vo}{L} \cdot ton$$

$$\begin{pmatrix} ILmin \\ ILmax \end{pmatrix} := find(ILmin, ILmax)$$

Hence, at **FULL** load

$ILmin = 9.091A$ $ILmax = 10.909A$

$\Delta IL := ILmax - ILmin$ $\Delta IL = 1.818A$

Next we will determine ILmin and ILmax at Minimum load

Initial Guesses for ILmin and ILmax $ILmin1 := 1A$ $ILmax1 := 1A$

Given TWO equations in terms of ILmin and ILmax

Given

$$\frac{ILmax1 + ILmin1}{2} = Iomin$$

$$ILmax1 - ILmin1 = \frac{Vin - Vo}{L} \cdot ton$$

$$\begin{pmatrix} ILmin1 \\ ILmax1 \end{pmatrix} := Find(ILmin1, ILmax1)$$

Hence, at MINIMUM load

$ILmin1 = 0\,A$ $\quad$ $ILmax1 = 1.818A$

$\Delta IL1 := ILmax1 - ILmin1$ $\quad$ $\Delta IL1 = 1.818A$

Finding Output Capacitor Value

Compute approximate value of ESR $\quad ESR := \frac{\Delta Vo}{\Delta IL}$ $\quad ESR = 5.5 \times 10^{-3}\,\Omega$

Assume we will be using Electrolytic Capacitor whose ESR*C=65us

$$Co := \frac{65 \cdot 10^{-6}\,s}{ESR} \qquad Co = 0.012F$$

Choose next standard value of the capacitor $\quad Co := 15 \cdot 10^{-3}\,F$

Recalculate ESR with the chosen capacitor

$$ESR := \frac{65 \cdot 10^{-6} s}{Co} \qquad ESR = 4.333 \times 10^{-3}\,\Omega$$

Ripple due to Capacitor charge and discharge

$$\Delta Vc := \frac{\Delta IL \cdot Ts}{8Co} \qquad \Delta Vc = 1.515 \times 10^{-4}\,V$$

Ripple due to Capacitor's ESR

$$\Delta Vesr := \Delta IL \cdot ESR \qquad \Delta Vesr = 7.879 \times 10^{-3}\,V$$

Total Ripple $\quad \Delta Vtot := \Delta Vc + \Delta Vesr \qquad \Delta Vtot = 8.03 \times 10^{-3}\,V$

STOP! Check to see if ΔVtot meets the RIPPLE requirement

Next we compute RMS capacitor current

Equation of IL during ON time $$IL1(t) := ILmin + \frac{\Delta IL}{ton} \cdot t$$

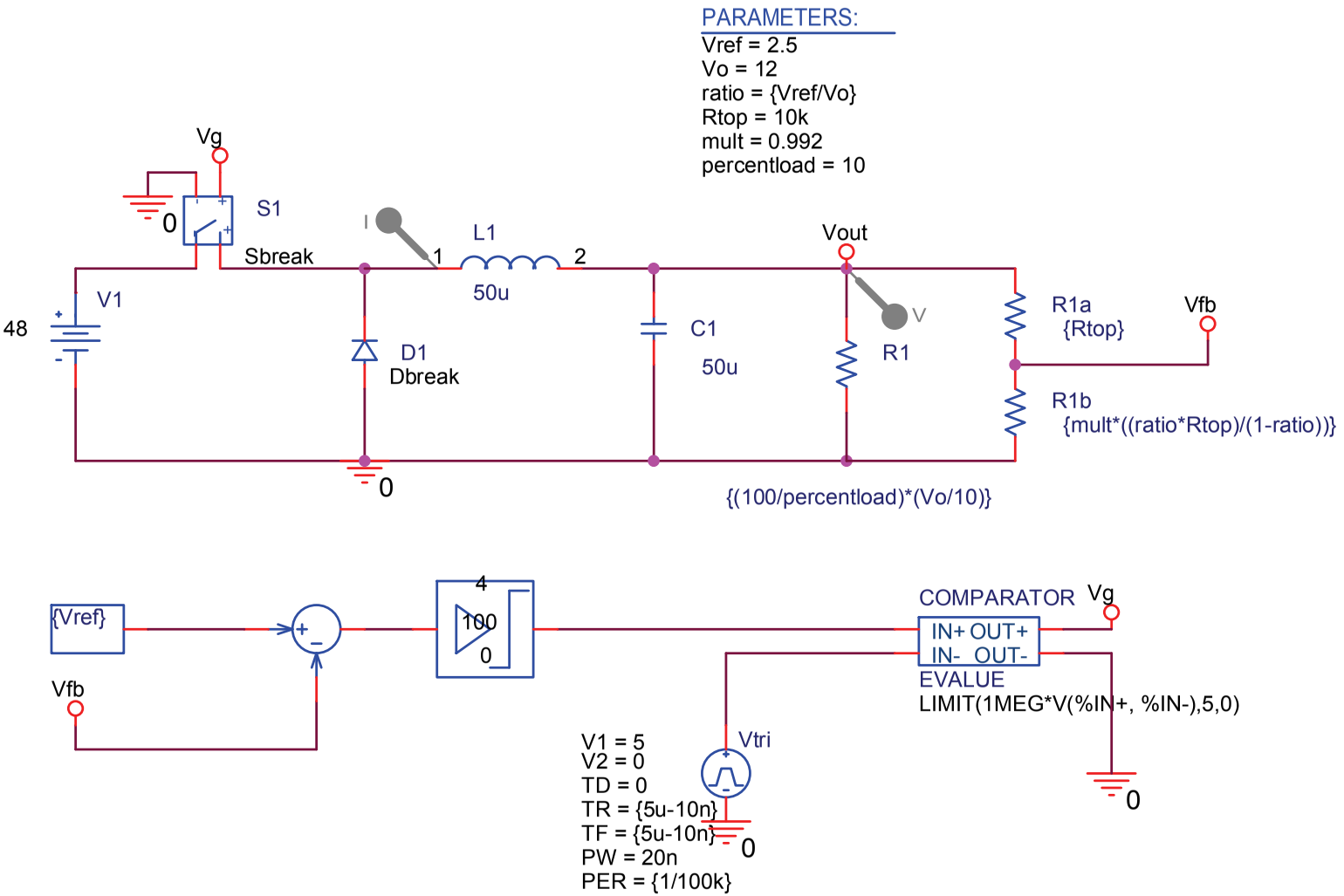
Equation of IL during OFF time $$IL2(t) := ILmax + \frac{-\Delta IL}{Ts - ton} \cdot t$$

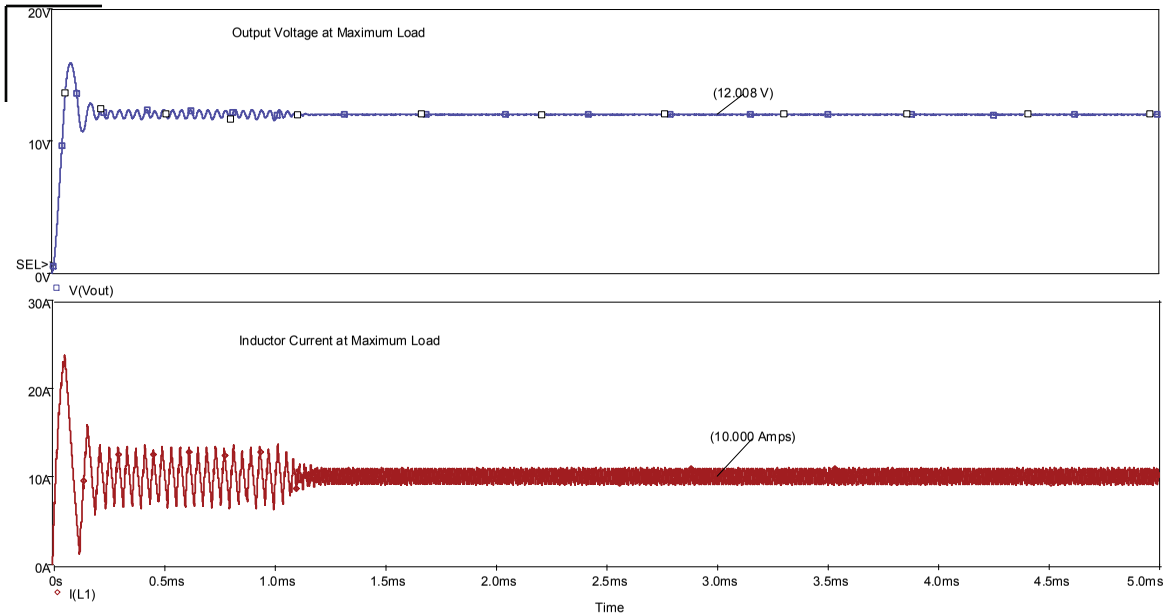
$$Icrms := \sqrt{\frac{1}{Ts} \cdot \left[\int_{0s}^{ton} (IL1(t) - Iomax)^2 \, dt + \int_{ton}^{Ts} (IL2(t) - Iomax)^2 \, dt \right]}$$

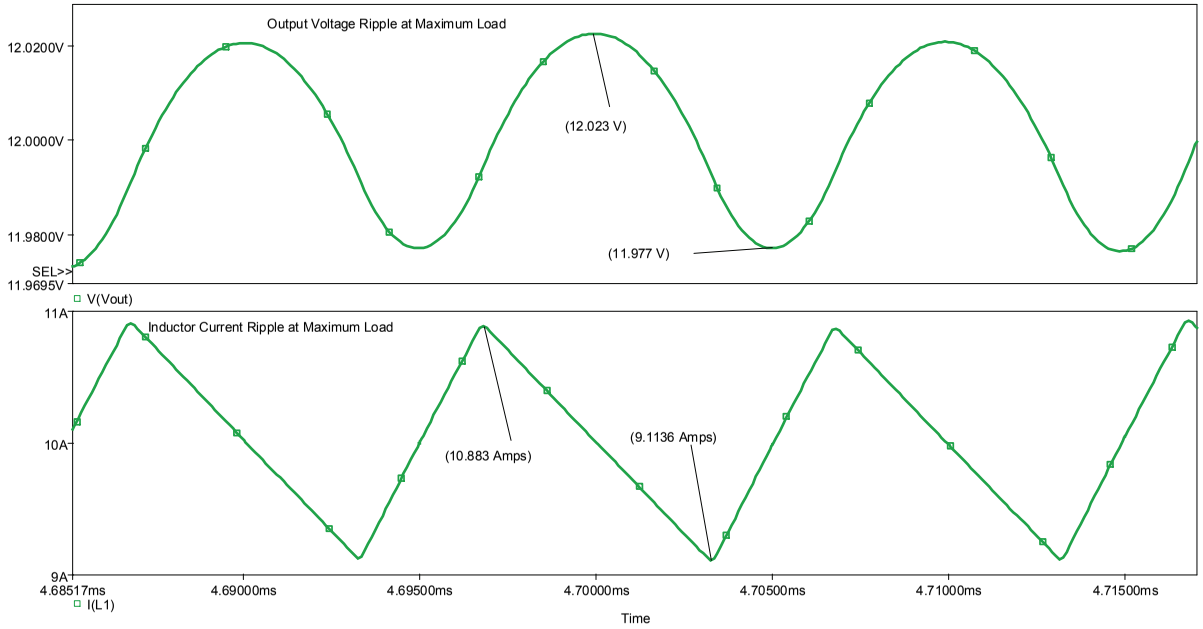
$$Icrms = 0.742A$$

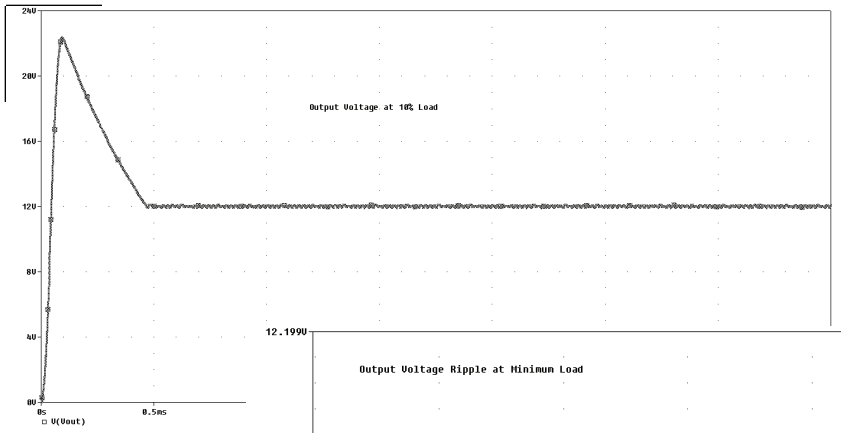
Power Loss in the Capacitor

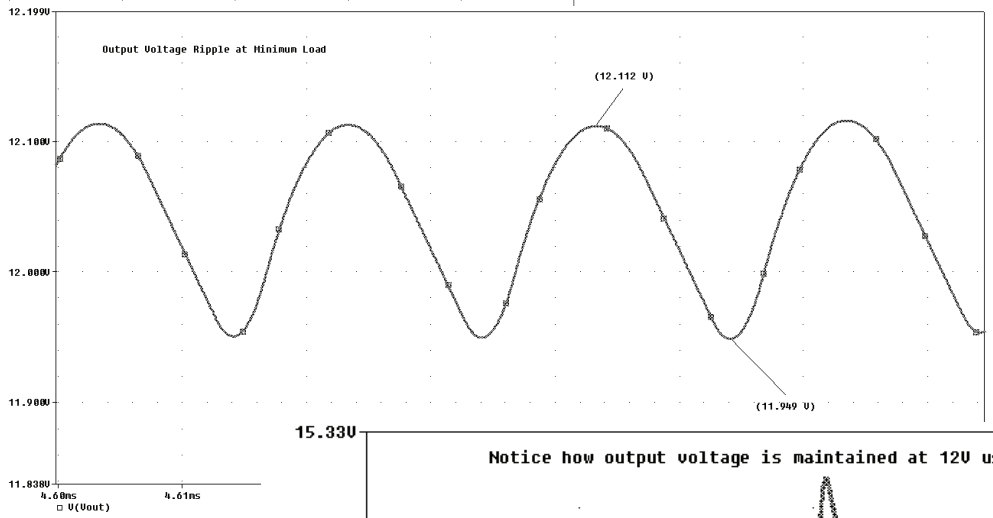
$$Pcap := Icrms^2 ESR \qquad Pcap = 2.388 \times 10^{-3} W$$

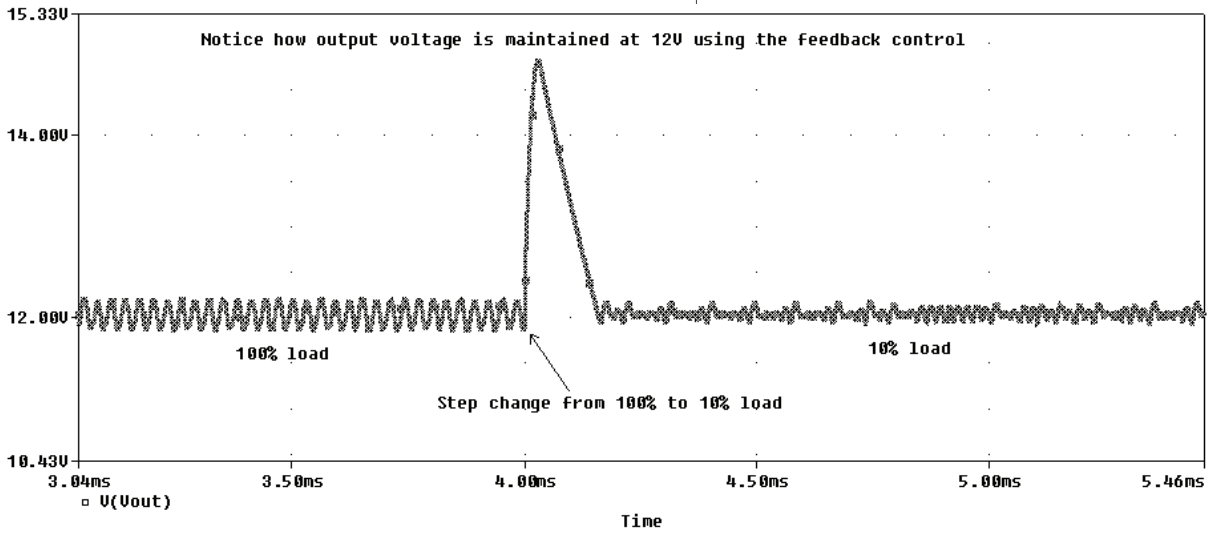

PARAMETERS:
Vref = 2.5
Vo = 12
ratio = {Vref/Vo}
Rtop = 10k
mult = 0.992
percentload = 10
Vg
S1
Sbreak
0
L1
50u
Vout
V1
48
D1
Dbreak
C1
50u
R1
R1a
{Rtop}
Vfb
R1b
{mult*((ratio*Rtop)/(1-ratio))}
{(100/percentload)*(Vo/10)}
{Vref}
Vfb
4
100
0
COMPARATOR
IN+ OUT+
IN- OUT-
EVALUE
LIMIT(1MEG*V(%IN+, %IN-),5,0)
V1 = 5
V2 = 0
TD = 0
TR = {5u-10n}
TF = {5u-10n}
PW = 20n
PER = {1/100k}
Vtri


Output Voltage at Maximum Load
(12.008 V)
20V
10V
SEL>
0V
V(Vout)
Inductor Current at Maximum Load
(10.000 Amps)
30A
20A
10A
0A
0s
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms
I(L1)
Time


Output Voltage Ripple at Maximum Load
(12.023 V)
(11.977 V)
12.0200V
12.0000V
11.9800V
SEL>>
11.9695V
V(Vout)
Inductor Current Ripple at Maximum Load
(10.883 Amps)
(9.1136 Amps)
11A
10A
9A
4.68517ms
4.69000ms
4.69500ms
4.70000ms
4.70500ms
4.71000ms
4.71500ms
I(L1)
Time


Output Voltage at 10% Load
24V
20V
16V
12V
8V
4V
0V
0s
0.5ms
V(Vout)


Output Voltage Ripple at Minimum Load
(12.112 V)
(11.949 V)
12.199V
12.100V
12.000V
11.900V
11.838V
4.60ms
4.61ms
V(Vout)


Notice how output voltage is maintained at 12V using the feedback control
15.33V
14.00V
12.00V
10.43V
100% load
10% load
Step change from 100% to 10% load
3.04ms
3.50ms
4.00ms
4.50ms
5.00ms
5.46ms
V(Vout)
Time

Efficiency Improvement

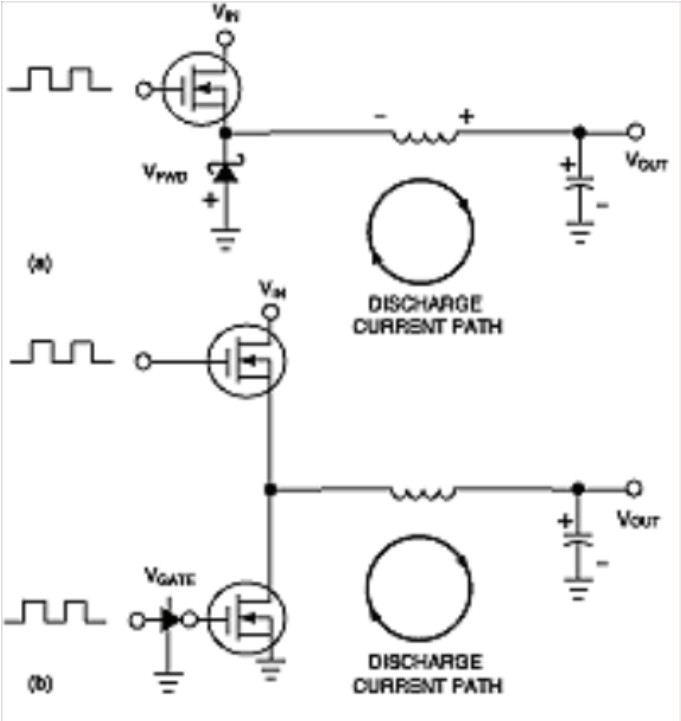
- Ways to improve converter's efficiency:
  - MOSFET
    - Low R_{dson} for High Duty Cycle
    - Low Gate Charge for Low Duty Cycle
    - Paralleling for High Current
  - Schottky Diode
    - Low forward drop
    - Short recovery time
  - Inductor
    - Multiple parallel winding such as Bifiliar (two windings), Trifiliar (three windings)

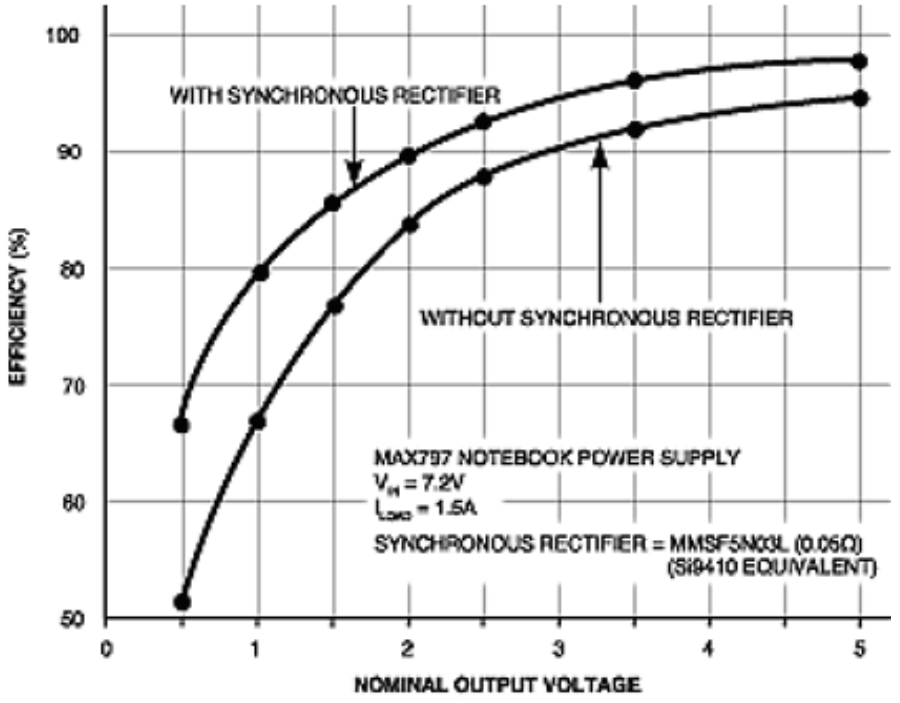
Efficiency Improvement

- Capacitors
  - Low ESR
  - Paralleling caps (increasing capacitance while reducing ESRs)
- Lower inductor current ripple
  - Reduce rms loss (inductor and output capacitor)
  - Increase switching frequency or inductance
    - Switching loss and real-estate trade off
- Lower gate drive voltage
- Use of Synchronous MOSFET in place of diode, especially for low voltage and high current output

Synchronous Rectification

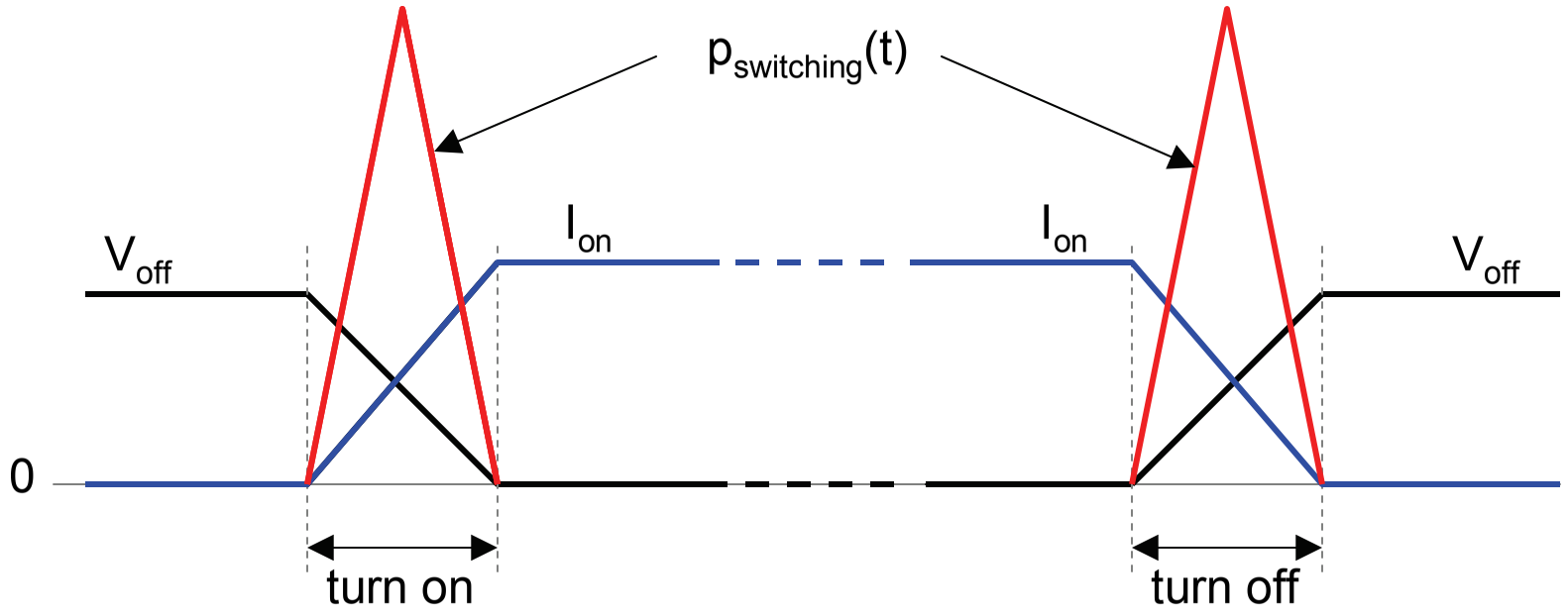
- Replaces freewheeling schottky with MOSFET
- Especially beneficial on low duty cycle and high current applications
- Due to required dead time and slow MOSFET's body diode, a Schottky is connected across the Synchronous MOSFET
- MOSFET + Schottky = FETKY combo such as IRF7326D2





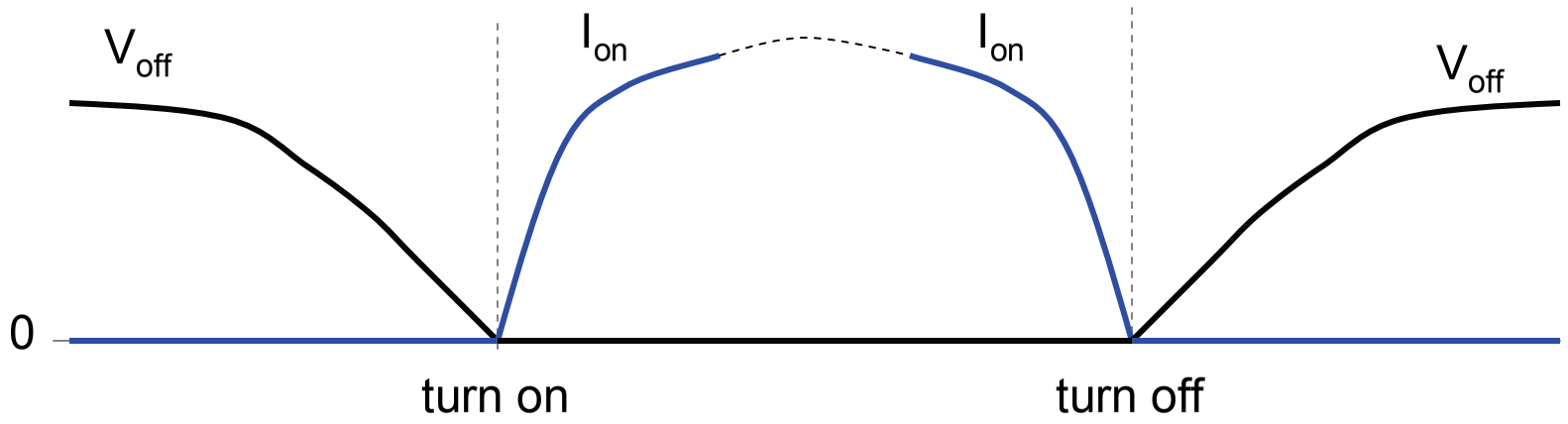
Soft-Switching

- Prevents hard-switching or the overlapping of switch's voltage and current during turn-on and turn-off transitions
  - switching losses which is proportional to switching frequency
- Use of resonant circuit to shape switch voltage and/or current waveforms to inherently go to zero at which switching transition is initiated ➔ zero switching loss



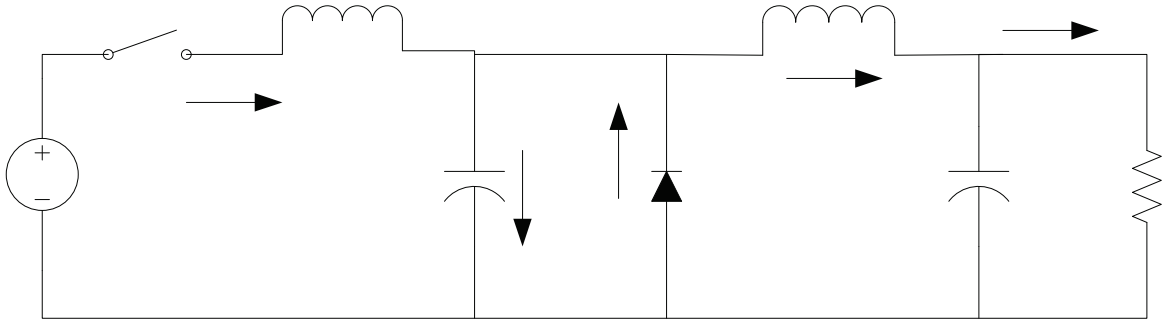
Soft-Switching

- Quasi-resonant buck topologies such as Zero-Voltage and Zero Current Resonant Switch Buck converter
- Needs constant-on or constant-off controllers such as UC1865 - UC1868, UC1861 – UC1864, MC34067 and MC33067, TDA4605-3, TDA4605-2

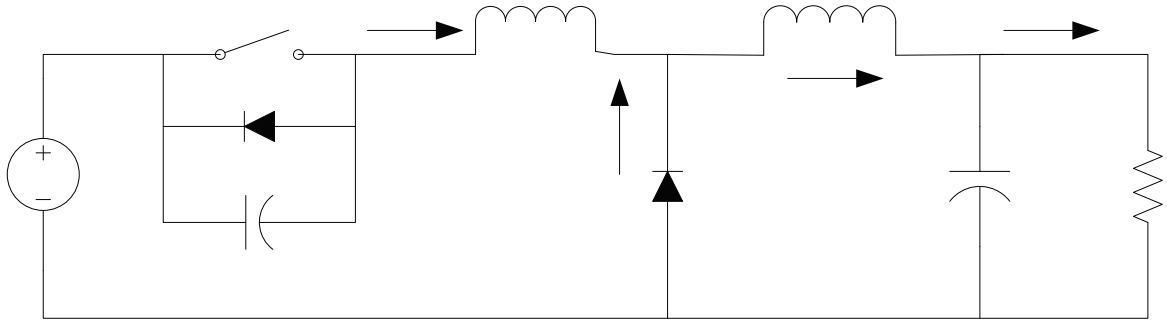


Soft-Switching

- Zero-Current Resonant Switch Buck
  - Turns switch OFF at zero current



- Zero-Voltage Resonant Switch Buck
  - Turns switch ON at zero voltage



PWM Controller

- Current Mode Controller will be used due to many of its advantages
  - Easy Compensation
    - With voltage-mode, the sharp phase drop after the filter resonant frequency requires a type III compensator to stabilize the system
    - Current-mode control looks like a single-pole system, since the inductor has been controlled by the current loop
    - Improves the phase margin, makes the converter much easier to control
    - A type 2 compensator is adequate, greatly simplifies the design process
    - With voltage-mode control, crossover has to be well above the resonant frequency, or the filter will ring.
  - CCM and DCM Operation
    - It is not possible to design a compensator with voltage-mode that can provide good performance in both CCM and DCM
    - With current-mode, crossing the boundary between the two types of operation is not a problem
    - Having optimal response in both modes is a major advantage, allowing the power stage to operate much more efficiently
  - Line Rejection
    - Closing the current loop gives a lot of attenuation of input noise
    - Even with only a moderate gain in the voltage feedback loop, the attenuation of input ripple is usually adequate with current-mode control
    - With voltage-mode control, far more gain (or feed forward) is needed in the main feedback loop to achieve the same performance

PWM Controller

- For the sake of example, we'll use UC184x or MIC38HC4x family

Unitrode Products
from Texas Instruments

application INFO available

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low Ro Error Amp

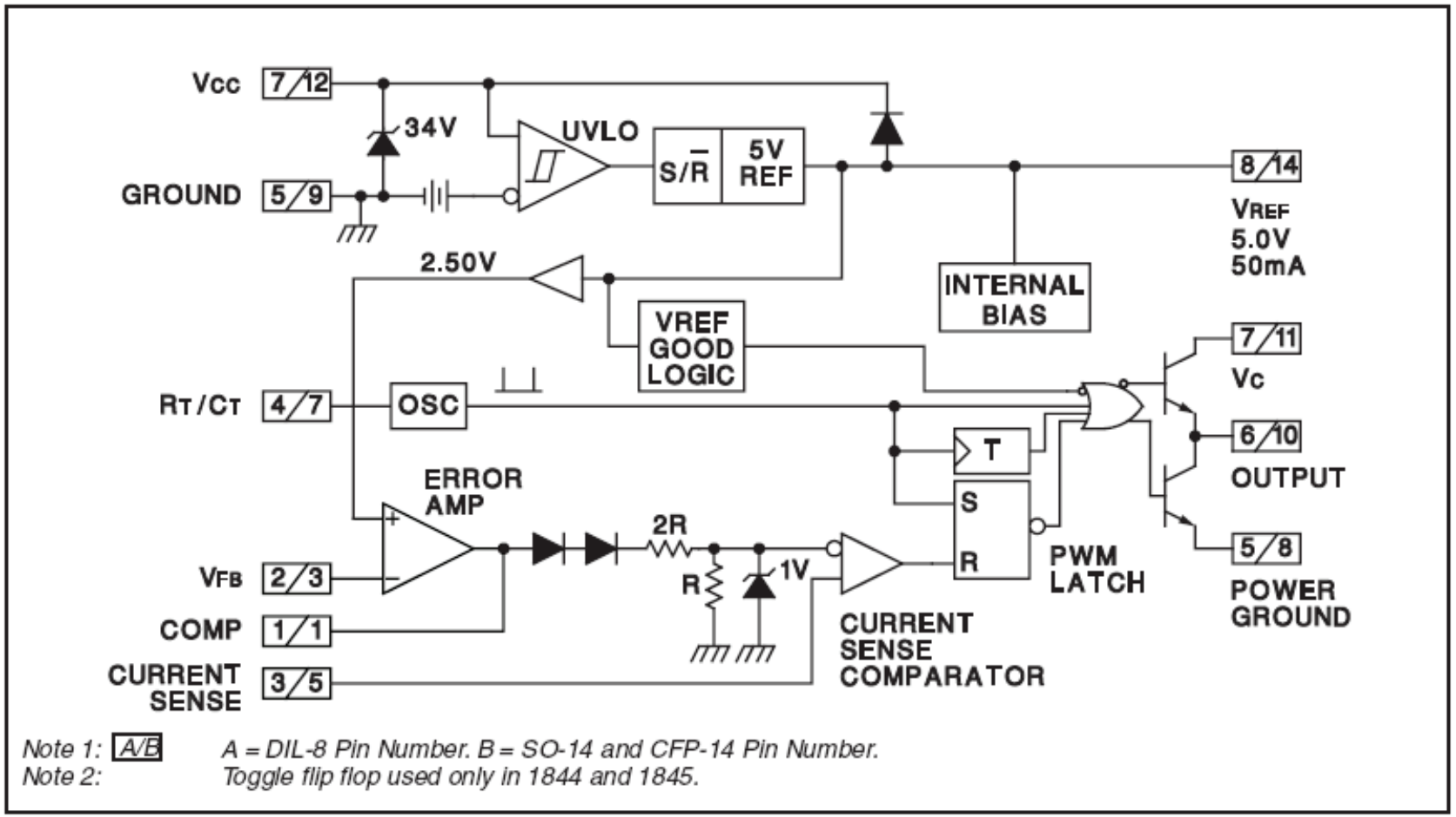
DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

PWM Controller

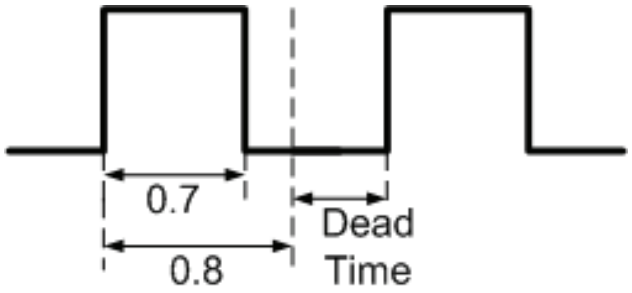
BLOCK DIAGRAM



Note 1: A/B *A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.*
Note 2: Toggle flip flop used only in 1844 and 1845.

PWM Controller

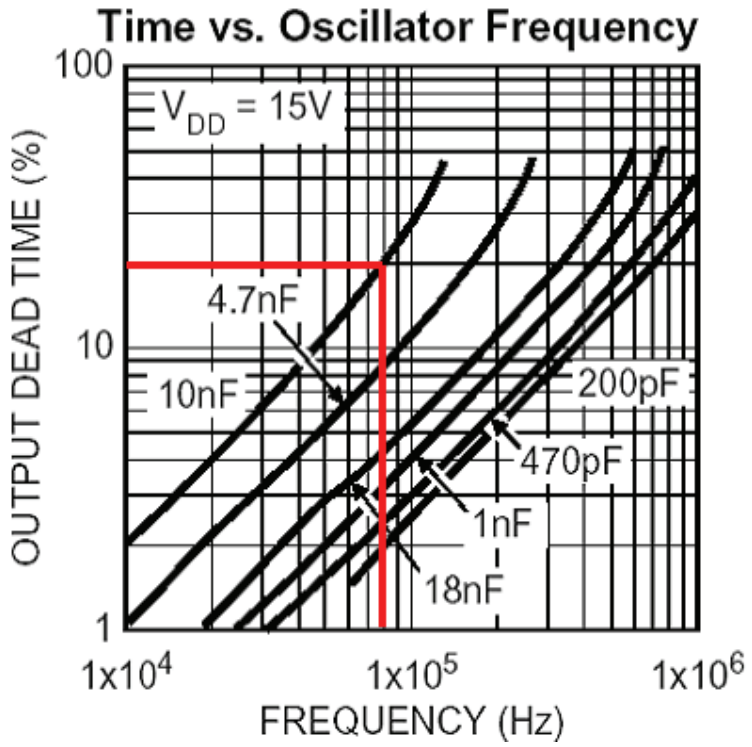
- Selecting Timing Resistor and Timing Capacitor
  - Maximum Duty Cycle and Switching Frequency have to be determined first
  - Percent Dead time would then be computed from Dmax
  - Using % Dead time along with Switching Frequency, we can then use plots provided in the data sheet to determine the required timing capacitor and timing resistor
- Example: Let's say that Dmax was calculated to be 70% or 0.7. Add safety factor to Dmax. Say 10% such that Dmax' = 0.8



- The dead time is therefore = 100% - 80% = 20%
- If switching frequency used is 80 kHz, then the value for % dead time along with switching frequency can be used to determine the required Timing Capacitor
- This is done by using the plot provided in the data sheet.

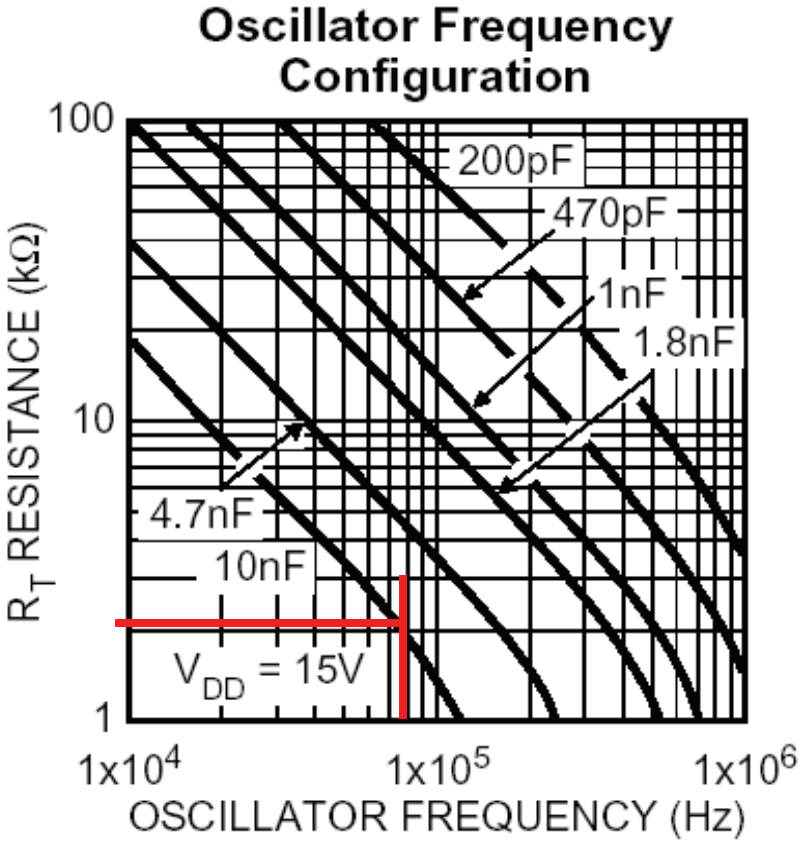
PWM Controller

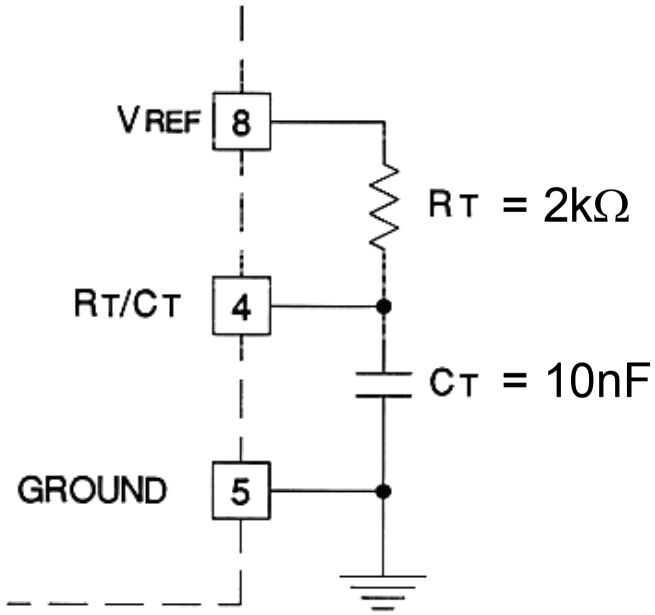
- From plot, 80 kHz intersects the 20% dead time at approximately Timing Capacitor value of 10 nF.
- Next, the timing resistor is found from the plot which is also provided in the data sheet



PWM Controller

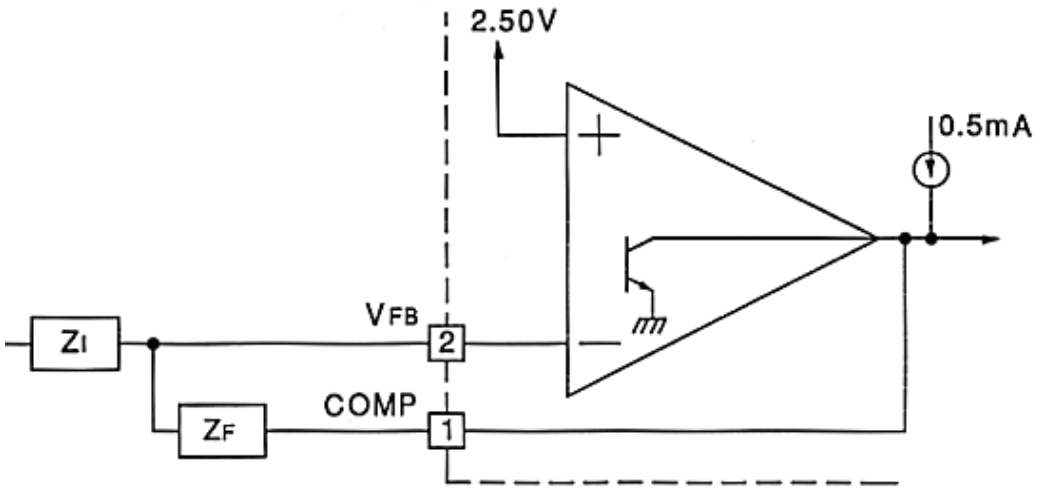
- Plot shows that 80kHz intersects the timing capacitor plot for 10 nF at timing resistance approximately equals to 2kΩ
- So, in order to provide the 20% dead time at 80 kHz switching frequency, the timing components are: C_T = 10 nF and R_T = 2 kΩ



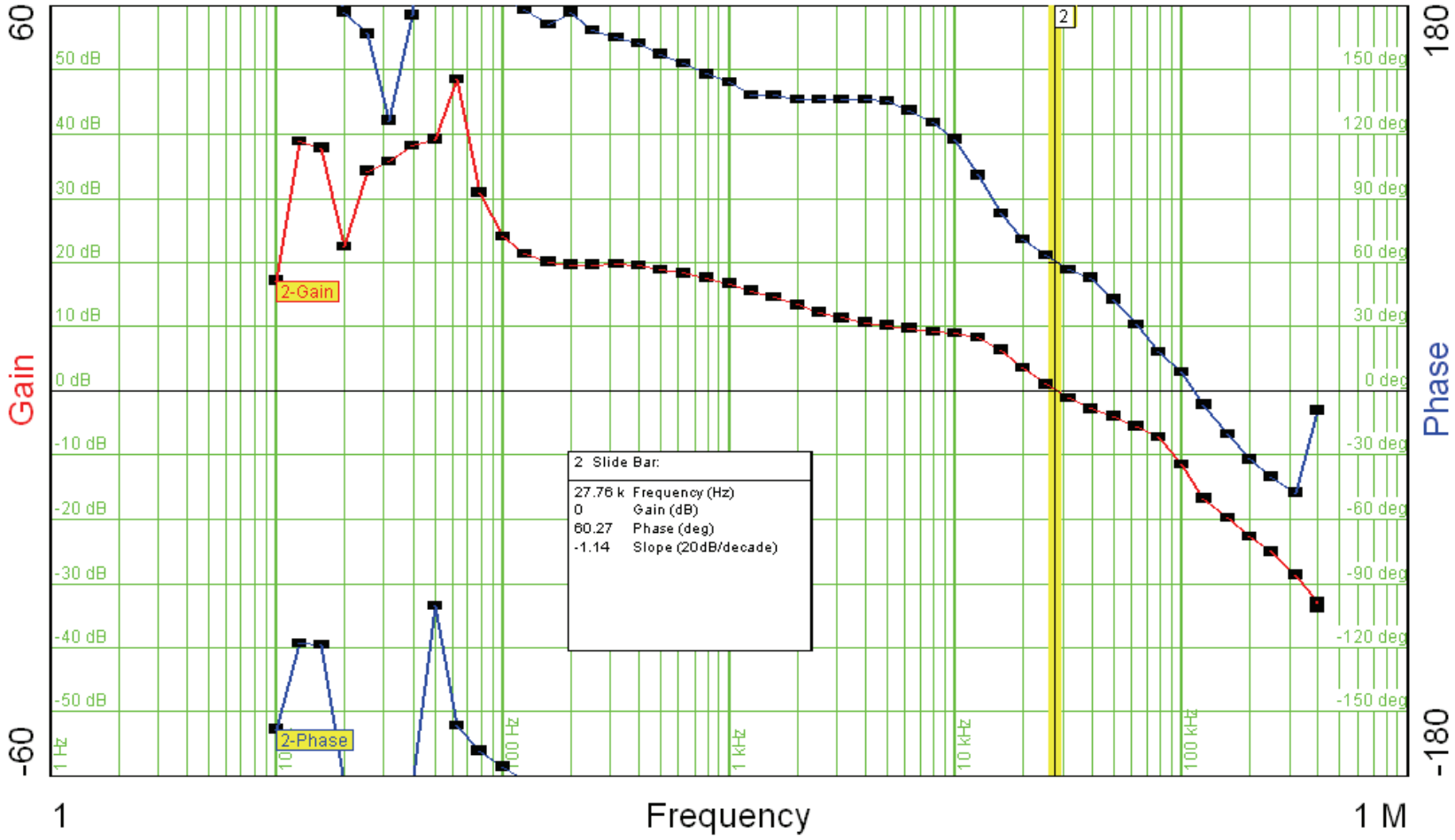


PWM Controller

- Feedback Compensation
  - As a start, typically a small capacitor is placed on ZF (such as 2200 pF) for feedback compensation
  - Once a prototype is built, the feedback compensation will be investigated to give the desired gain and phase margin and stability (over wide range of load)
  - Involves decision of whether to use type I, II, or III error amplifier



PWM Controller



PWM Controller

- Steps for selecting components in Type 2
  - Choose cross-over frequency F_{cross} to be around 1/3 of switching frequency F_{switch}
  - The required pole frequency F_{p0} that yields the desired crossover frequency of the open loop gain (where H_0 is dc gain of the plant)

$$F_{p0} = \frac{F_{cross}}{H_o}$$

  - Calculate capacitor C_1 where R_1 should have been selected when setting the voltage divider

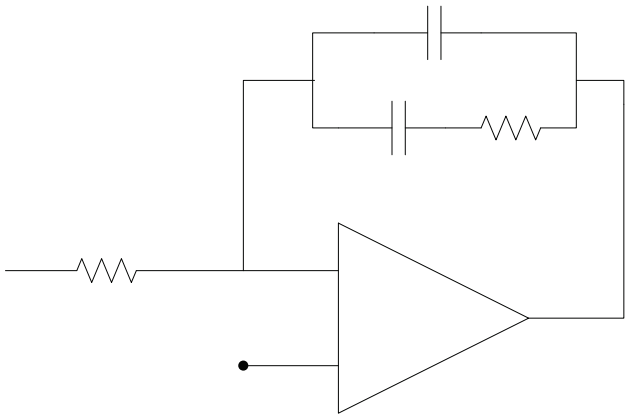
$$C_1 = \frac{1}{2\pi R_1 F_{p0}}$$

  - Calculate R_2 using the previously calculated C_1 and the output pole of the plant F_p

$$R_2 = \frac{1}{2\pi C_1 F_p}$$

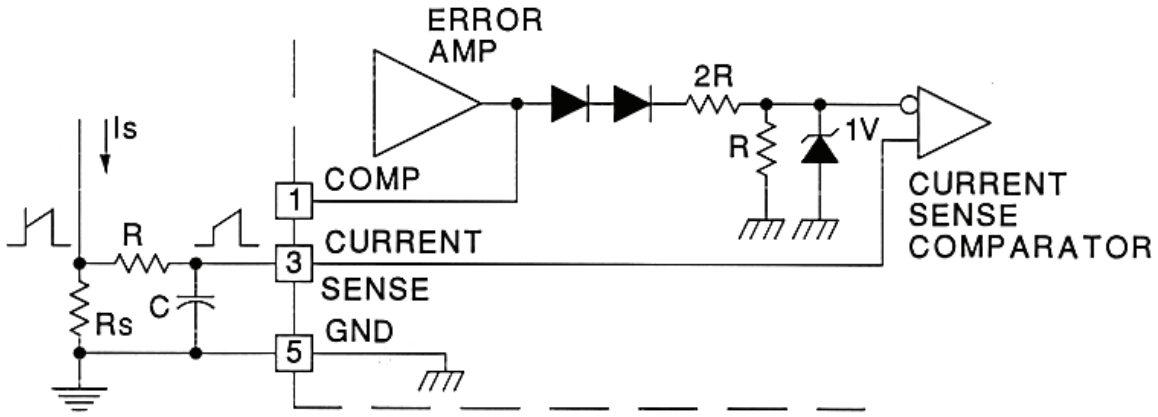
  - Calculate capacitor C_3 where F_{esr} is the location of the ESR zero

$$C_3 = \frac{1}{2\pi ESR \cdot F_{esr}}$$



PWM Controller

- Current Sensing Resistor
  - Need to calculate power rating of the sensing resistor. This involves calculating worst case I_{rms} through the sensing resistor, and then compute $P = (I_{rms})^{2*}R_{sense}$
  - A low pass RC filter circuit is also needed to eliminate leading spike on the pulse voltage resulted from current being sensed
  - Ensure that voltage out of the filter is less than 1V (for this controller). If not, then reduce the value of R_{sense}



Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{RS}$$

Layout Considerations

- Keep trace inductance low (preferably by reducing length, not increasing width) for the critical path (switch and diode paths)
  - Noise spikes may appear in input and output, and to the controller chip
  - Avoid using a current probe (a loop of wire) for diode and switch due to additional inductance it will produce
- Provision of good Input decoupling since input capacitor is in the critical path
  - Besides the usual bulk capacitor, also put a small ceramic capacitor at the supply end to ground, and another one close to the switch to ground
- Provision of good decoupling with a small ceramic capacitor between input and ground pins
- Try using shielded inductor, and position the inductor away from the controller and feedback trace
- In multi-layer boards, dedicate one layer for ground
- Keep the feedback trace as short as possible to minimize noise pickup and place it away from noise sources

Multiphase

- The technique used mainly in very low voltage and high power applications such as processors
  - Next-generation networking ASICs and processors require multiple lower voltages, higher currents, faster dynamic response, greater efficiency and power management solutions that reside close to the load
  - To meet the need of increasing power density through higher efficiencies and higher operating frequencies
- A novel power architecture, multiphasing topologies, is emerging to contend with tomorrow's power requirements
- High-density applications with lower power levels are usually managed with 2-phase solutions, whereas higher power levels can require up to 4-phase solutions

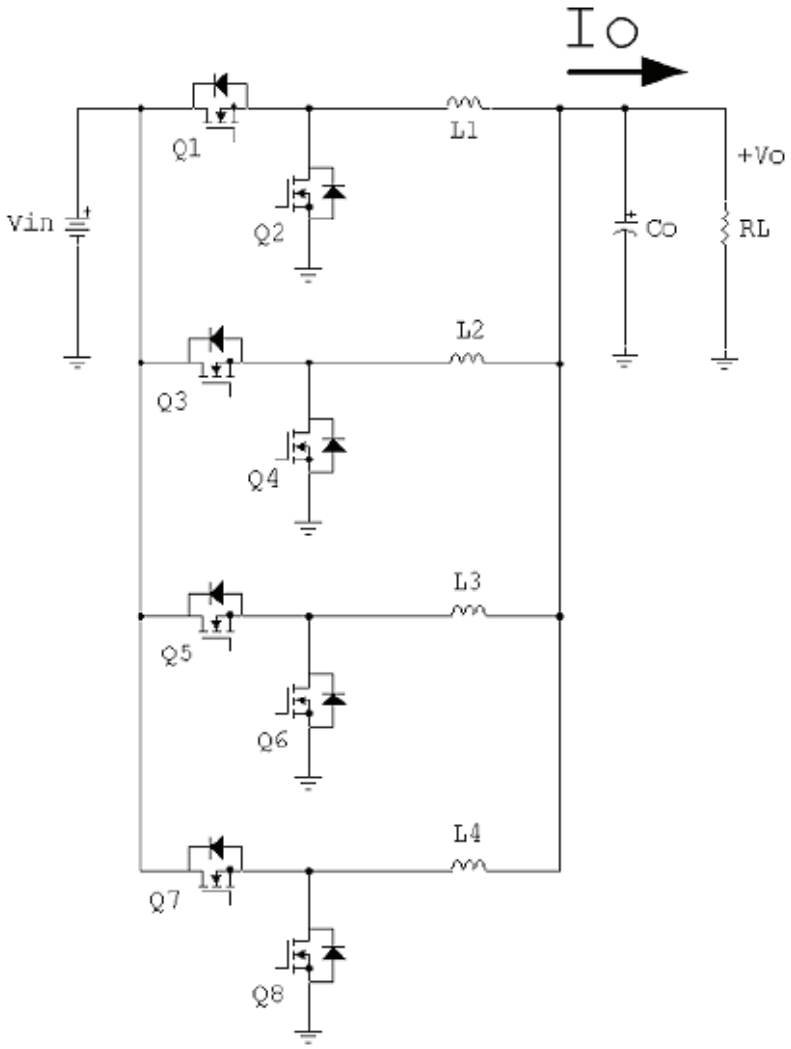
Multiphase

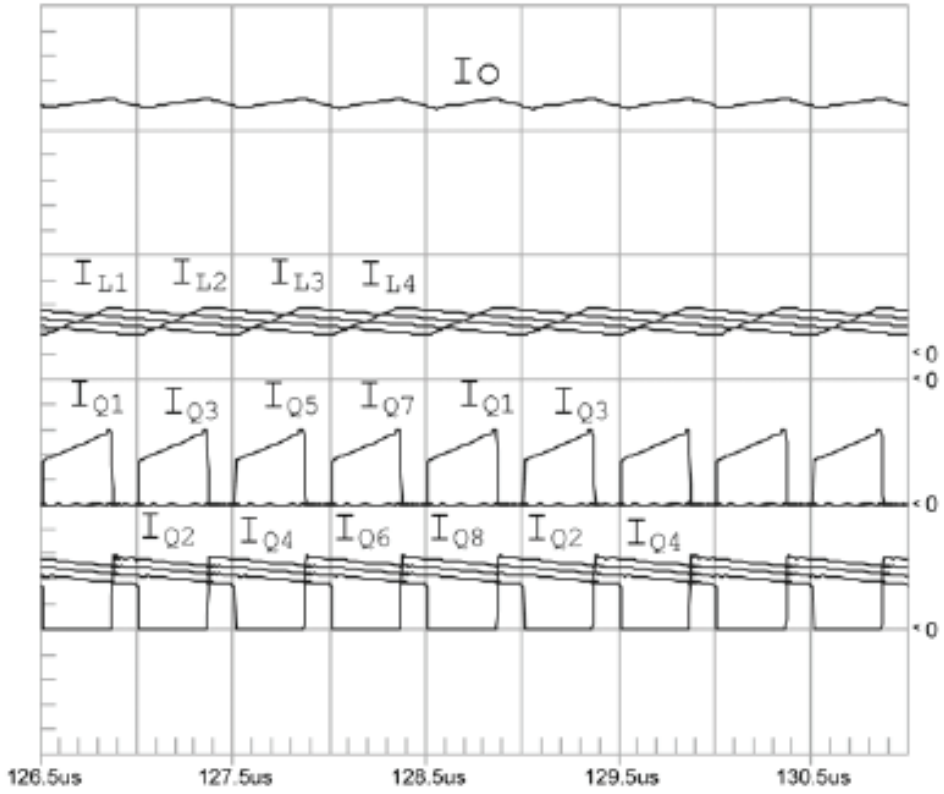
- Multiphasing address 5 key parameters in power conversion
  - Efficiency: The best power efficiency is achieved by converting a voltage in a single stage, rather than double conversion.
    - For example, assume you want to convert 48V to 1.2V at 100W using a 2-phase forward converter
    - In a 2-phase conversion, current is split equally in the two phases. The FET on-losses are $I^2 \times R$, which equates to a 50% reduction in on-losses
    - Lower peak currents provide lower turn-on and turn-off losses, resulting in lower switching losses
    - Lower turn-on and switching losses provide overall greater efficiency
  - Input/output ripple reduction: Multiphasing PWM controllers increases switching frequency. The resulting frequency is equivalent to the PWM clock frequency times the number of phases. Higher operating frequency equates to less input/output capacitance and smaller input/output inductors

Multiphase

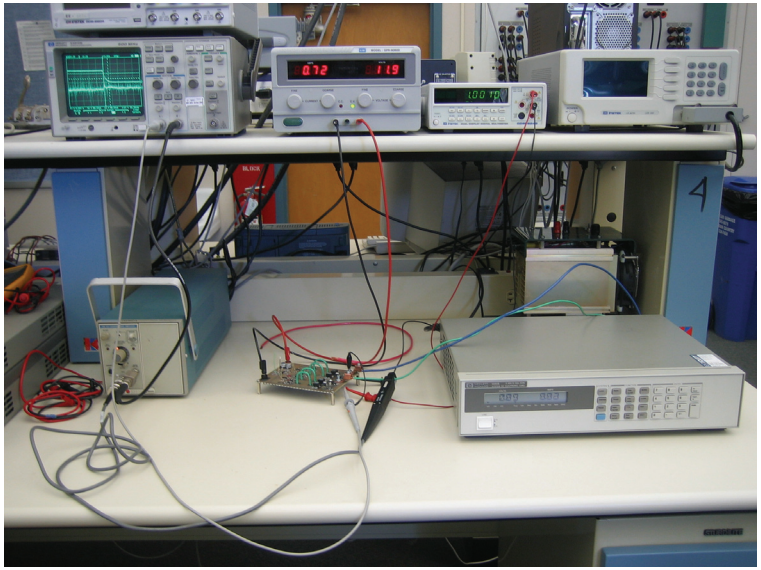
- Fast dynamic response. Improved dynamic response is the result of smaller output inductors allowing for fast response to current changes combined with higher operating frequency, equal to clock frequency times the number of phases, which allows for higher crossover.
- Ease of manufacturability: Next-generation designs demand smaller form factors and automated assembly, eschewing hand soldering of large transformers, inductors and capacitors.
- Better thermal management: Thermal management is critical at these new power densities. The challenge is even higher with the emergence of modules operating in extended temperature range. With multiphasing techniques, you spread the heat evenly over the whole converter, avoiding hot spots and improving converter reliability

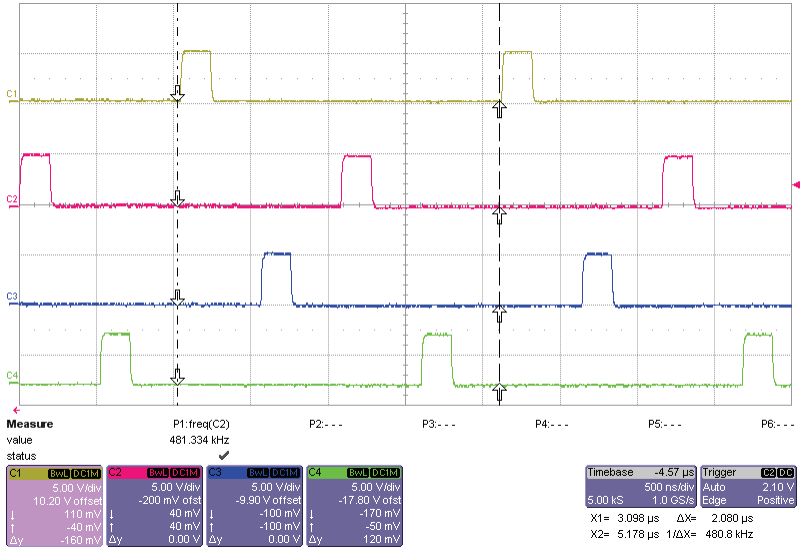
Multiphase

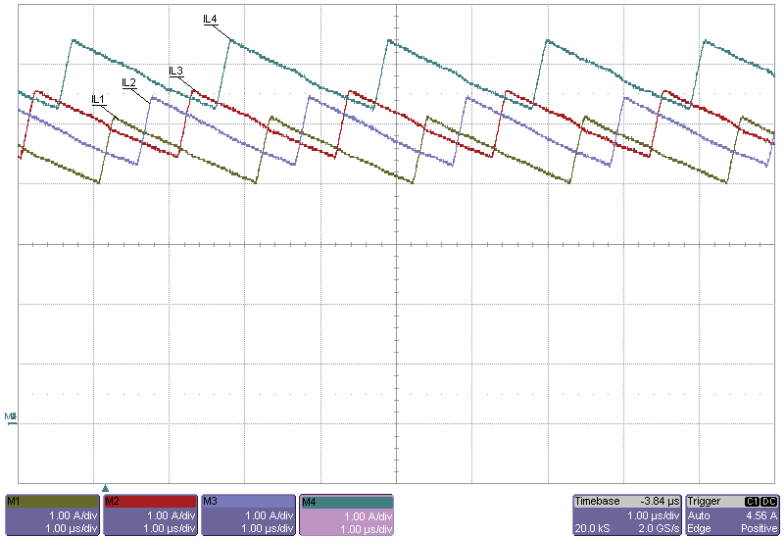

Io
Q1
L1
+Vo
Vin
Q2
Co
RL
L2
Q3
Q4
L3
Q5
Q6
L4
Q7
Q8

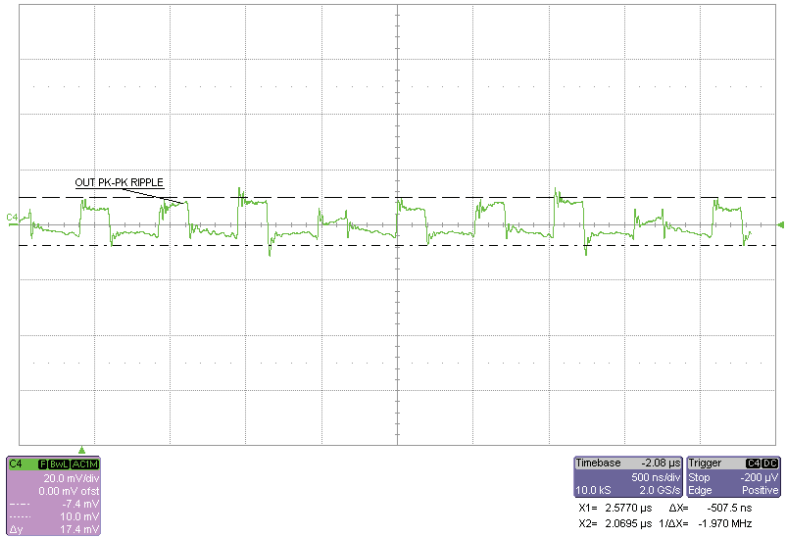

Io
IL1
IL2
IL3
IL4
IQ1
IQ3
IQ5
IQ7
IQ1
IQ3
IQ2
IQ4
IQ6
IQ8
IQ2
IQ4
126.5us
127.5us
128.5us
129.5us
130.5us

Multiphase

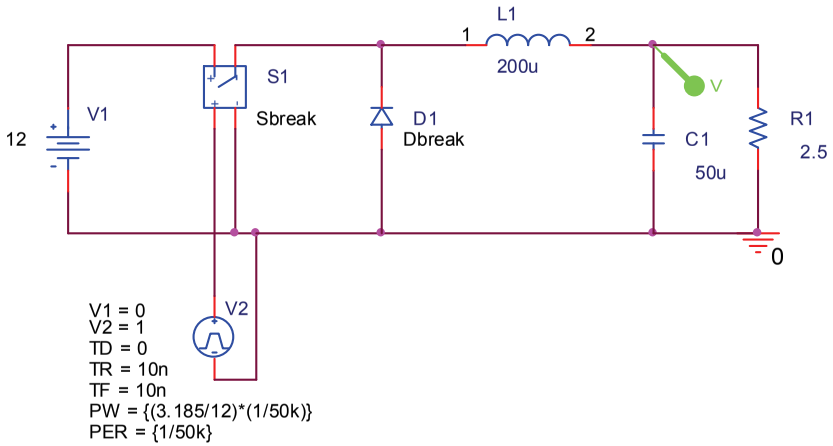


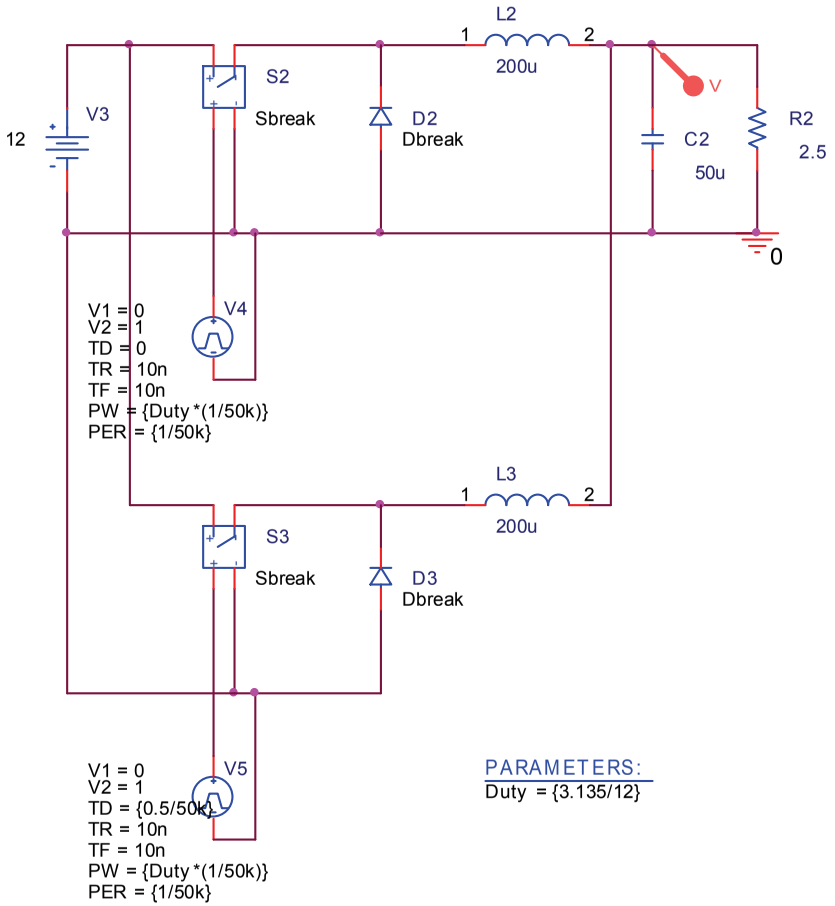

C1
C2
C3
C4
Measure
P1:freq(C2)
P2:- - -
P3:- - -
P4:- - -
P5:- - -
P6:- - -
value
481.334 kHz
status
C1 BwL DC1M
5.00 V/div
10.20 V offset
110 mV
-40 mV
-160 mV
C2 BwL DC1M
5.00 V/div
-200 mV ofst
40 mV
40 mV
0.00 V
C3 BwL DC1M
5.00 V/div
-9.90 V offset
-100 mV
-100 mV
0.00 V
C4 BwL DC1M
5.00 V/div
-17.80 V ofst
-170 mV
-50 mV
120 mV
Timebase -4.57 µs
500 ns/div
5.00 kS 1.0 GS/s
Trigger C2 DC
Auto 2.10 V
Edge Positive
X1= 3.098 µs ΔX= 2.080 µs
X2= 5.178 µs 1/ΔX= 480.8 kHz


IL4
IL2
IL3
IL1
M1 1.00 A/div 1.00 µs/div
M2 1.00 A/div 1.00 µs/div
M3 1.00 A/div 1.00 µs/div
M4 1.00 A/div 1.00 µs/div
Timebase -3.84 µs
1.00 µs/div
20.0 kS 2.0 GS/s
Trigger C1 DC
Auto 4.56 A
Edge Positive

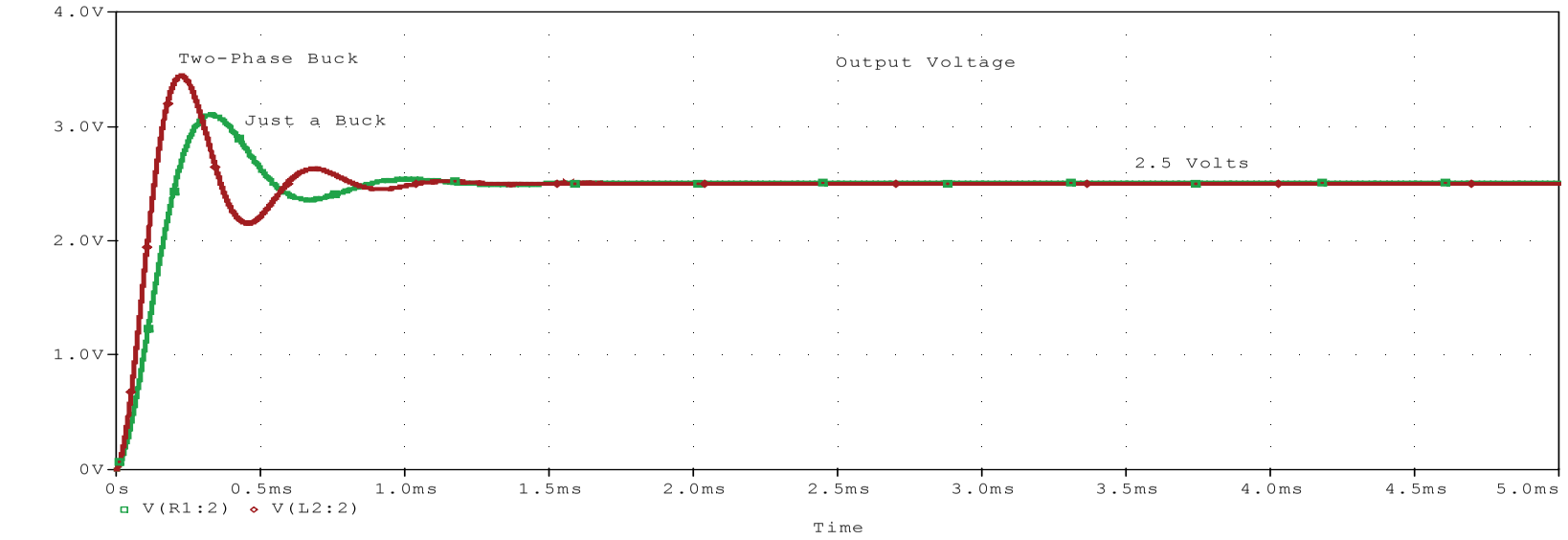

OUT PK-PK RIPPLE
C4
C4 BwL DC1M
20.0 mV/div
0.00 mV ofst
-7.4 mV
10.0 mV
17.4 mV
Timebase -2.08 µs
500 ns/div
10.0 kS 2.0 GS/s
Trigger DC DC
Stop -200 µV
Edge Positive
X1= 2.5770 µs ΔX= -507.5 ns
X2= 2.0695 µs 1/ΔX= -1.970 MHz

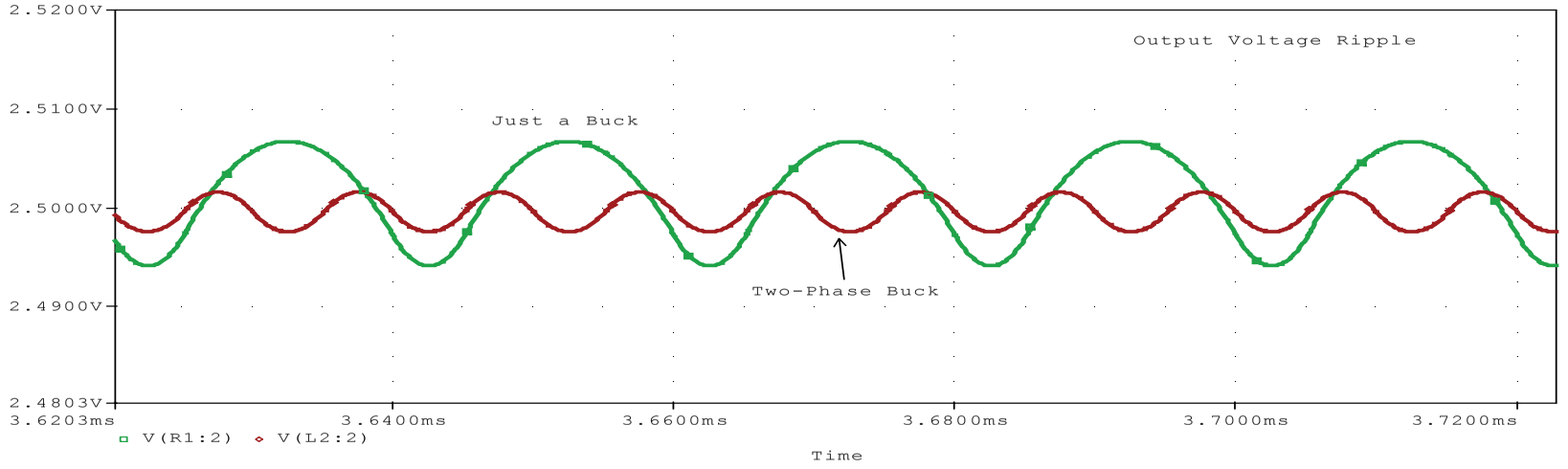
Two-Phase vs. 1 Buck



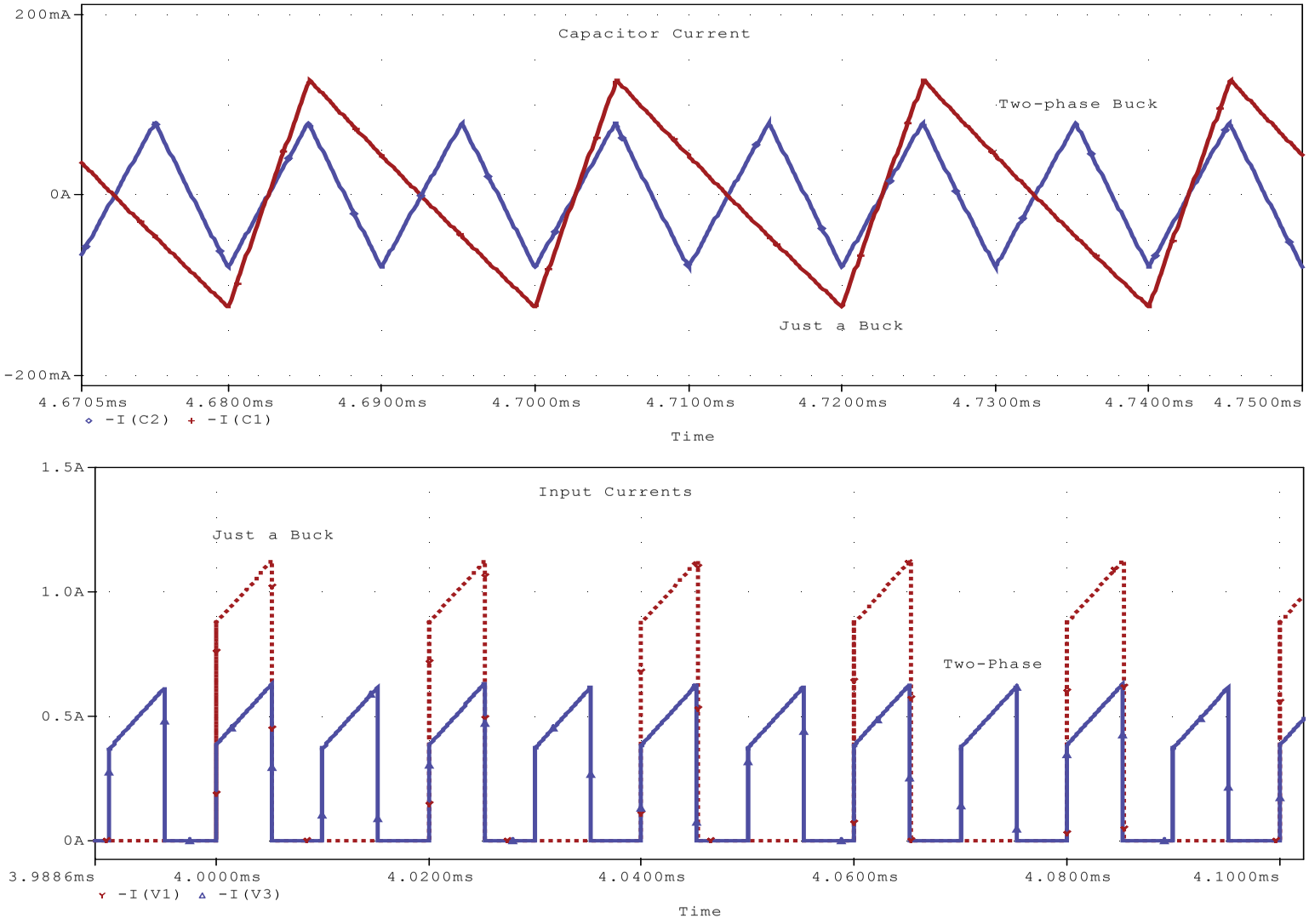


Two-Phase vs. 1 Buck





Two-Phase vs. 1 Buck



Power Electronics Lab at Cal Poly State University

- 6 Instructional Lab Benches, 2 Project/Thesis Benches
- For further information, contact Power Electronics Lab Coordinator, Dr. Taufik at taufik@calpoly.edu

Cal Poly
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