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Comparison between Analog and Digital Current To PWM Converter for Optical Readout Systems

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Abstract: **In this paper, we designed and compared analog and digital types of current to pulse-width modulation (PWM) converters for optical sensor readout. Two types of converters are designed and simulated in standard CMOS 65 nm technology. By comparing main performance parameters of sensor readout integrated circuits, such as chip area, power consumption, detectable current (sensitivity), and tolerance against process variations, we presented the design methodology, the pros and cons, and what applications are appropriate for each converter.**

Keywords: **Pulse-width modulation, current to PWM converter, optical sensor, photodiode, transimpedance amplifier.**

I. INTRODUCTION

In a fourth industry revolution, sensors for Internet of Things (IoT) systems are expected to be compact, low-cost, low-power. Among various sensing methods, an optical method using a photodiode is one of the rapidly growing methods due to high speed, small area and its wide range of applications from home applications to healthcare, environment and industrial monitoring [1-4].

Conventional readout circuit for optical sensors typically utilizes an analog to digital converter (ADC) to quantize the output voltage of a transimpedance amplifier (TIA), resulting in several disadvantages. For example, a capacitive successive approximation ADC can be low power, but has large area overhead. On the other hand, a sigma-delta ADC can achieve better resolution, but consumes significant power [5-6].

Pulse-width modulation (PWM) is another method for analog quantization, which converts the input current of photodiode to a pulse width signal [2-4]. Digital circuits and analog circuits of the TIA and comparators are used to convert the photocurrent into a PWM signal instead of the ADC. In this way, the complexity, power consumption and effect of environmental noise due to its digital two-level nature of the system are reduced. Generic PWM output type readout circuit block diagram is shown in Fig. 1. The PWM readout circuit consists of a current to PWM converter and a PWM to digital converter. The current to PWM converter (CPC) changes a photodiode current into the PWM signal. The PWM to digital converter converts the pulse width of PWM signal to digital signal generally using n-bit counter [3, 8]. The CPC can be implemented as a digital CPC and an analog CPC. The digital CPC [2] consists of all digital logics, and the TIA and comparator instead of the ADC are used to convert into PWM signal in the analog CPC [3].

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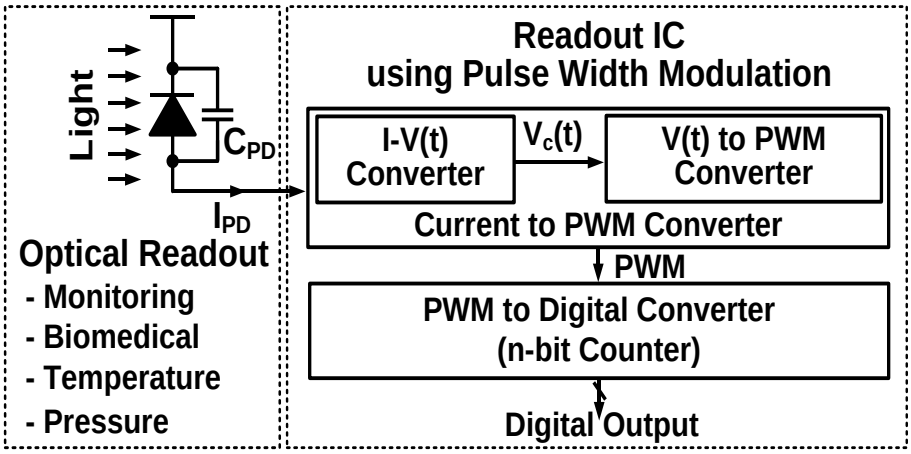

Figure 1: Block diagram of PWM-based readout circuit for optical readout systems

In this paper, a comparison of the digital and analog current to digital converter for optical sensors is presented. The comparison is performed through the post-layout simulation using 65 nm CMOS process. This paper is organized as follows. In Section II, the design of the digital and analog current to PWM converter is presented. Section III show the post-layout simulation results and comparison. Finally, the conclusion is given in Section IV.

II. CIRCUIT DESIGN

In the optical sensors using the photodiode, a detected sensing data is converted into a light intensity transmitted to the photodiode, and the photodiode outputs a current of different level according to the light intensity. The current to PWM converter changes the photodiode current into the pulse width of the PWM signal which is inversely proportional to the current level. The pulse width of the PWM signal is mainly determined by the photodiode current (I_{PD}), $C_{CPC,eff}$ which has a direct effect on the PWM conversion, a sensing voltage (V_{sen}). The pulse width is determined according to I_{PD} as shown in equation (1) because $C_{CPC,eff}$ and V_{sen} is the constant parameters determined in design process.

$$PW = \frac{C_{CPC,eff} \cdot V_{sen}}{I_{PD}} \qquad (1)$$

The I_{PD} is converted into the PWM signal by two steps. The first step is to convert I_{PD} into a voltage that changes linearly (increasing or decreasing) with time. In second step, the CPC detects whether $V_C(t)$ reaches V_{sen}, and converts the time of change from a reset voltage to V_{sen} into the pulse width of the PWM signal. This CPC can be implemented in the digital and analog ways.

A. Digital Current to PWM Converter:

The digital CPC consists of two inverters and three 2-input NAND gates as shown in Fig. 2. It basically operates by a clock and performs the PWM conversion when the clock is high. The conversion of I_{PD} into $V_{C,D}(t)$ which is the voltage linearly changing with time is processed by I_{PD} and a parasitic capacitor of the photodiode (C_{PD}). The I_{PD} is charged in C_{PD} and $V_{C,D}(t)$ linearly increases with time. When $V_{C,D}(t)$ reaches a threshold-voltage of a detection inverter (V_{th}), the detection inverter detects it and turns on SW1 to reset $V_{C,D}(t)$ to ground (0 V), and the other digital logics converts the time of change from ground to V_{th} into the pulse width. As a result, the pulse width of the digital CPC can be expressed by equation (2). In the case of the digital CPC, $C_{CPC,eff}$ in Eq. (1) is the parasitic capacitor of the photodiode (C_{PD}) and the sensing voltage is V_{th} of the detection inverter. In this paper, V_{th} is designed to be 424 mV at a supply voltage of 1.2 V, a process of typical-typical and 27 °C.

$$PW_D = \frac{C_{PD} \cdot V_{th}}{I_{PD}} \qquad (2)$$

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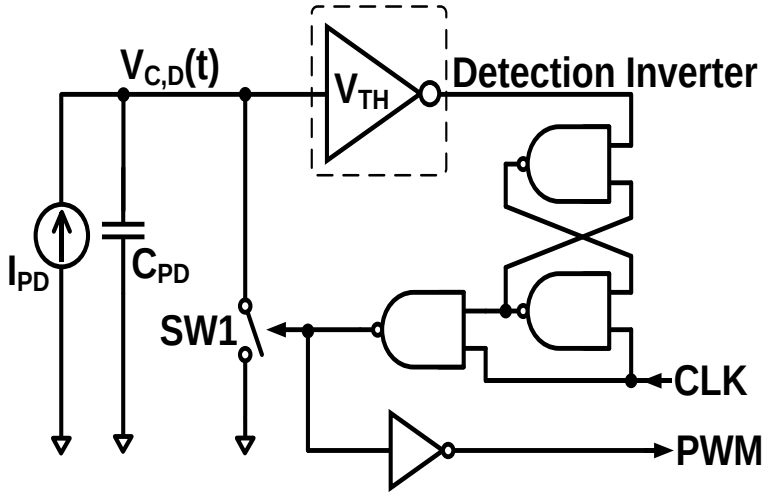

Figure 2: Schematic of the digital current to PWM converter

B. Analog Current to PWM Converter:

The analog current to PWM converter in Fig. 3 consists of a capacitive TIA, a comparator, and digital logics. It is also operated by a clock. When the clock is low, the conversion operation is performed and when the clock is high, $V_{C,A}(t)$ are reset to a V_{CM}. During the conversion operation, the TIA converts I_{PD} to $V_{C,A}(t)$ which decreases linearly from the reset voltage of V_{CM}. When $V_{C,A}(t)$ decreases to V_{ref}, the comparator detects $V_{C,A}(t)$, and the time of change from V_{CM} to V_{ref} is converted into the pulse width of the PWM signal by the comparator and the logic gates. The PWM equation of the analog CPC is shown in equation (3). Unlike the digital CPC, a feedback capacitor of the TIA (C_f) is $C_{CPC,eff}$ in Eq. (1), and V_{sen} is the difference of the voltage from V_{CM} to V_{ref}.

The miller two-stage operational amplifier (op-amp) is used for the TIA in Fig. 4. The first stage is a PMOS input differential pair with active current mirror loading, with a common source amplifier for the second stage. A Miller capacitor and RHP zero-compensating resistor are connected in series between first and second stage to split the first and second poles of the op-amp. The schematic of the comparator is same with the op-amp, except for RC compensation in the designed op-amp. The designed op-amp has a dc gain of 67.4dB, a 3-dB frequency of 16 kHz, and it consumes 109 µA from the supply voltage of 1.2 V.

$$PW_A = \frac{C_f \cdot (V_{CM} - V_{ref})}{I_{PD}} \qquad (3)$$

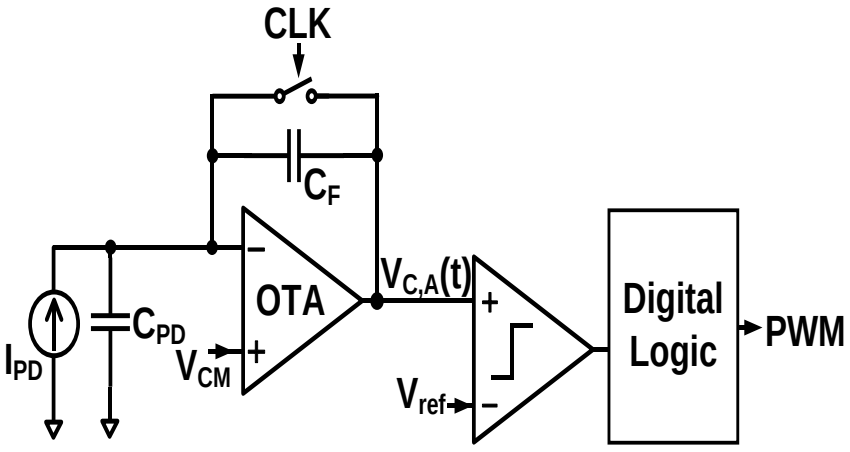

Figure 3: Schematic of the analog current to PWM converter

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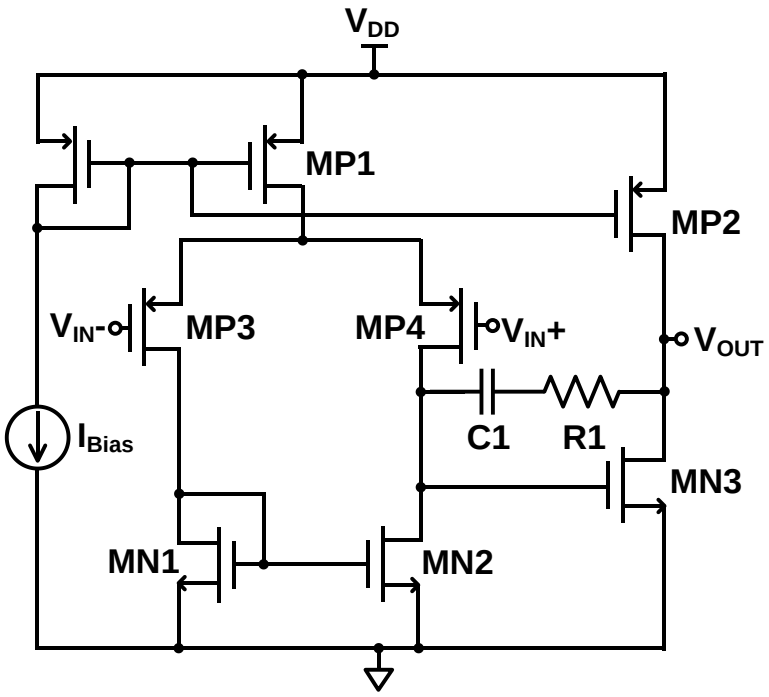
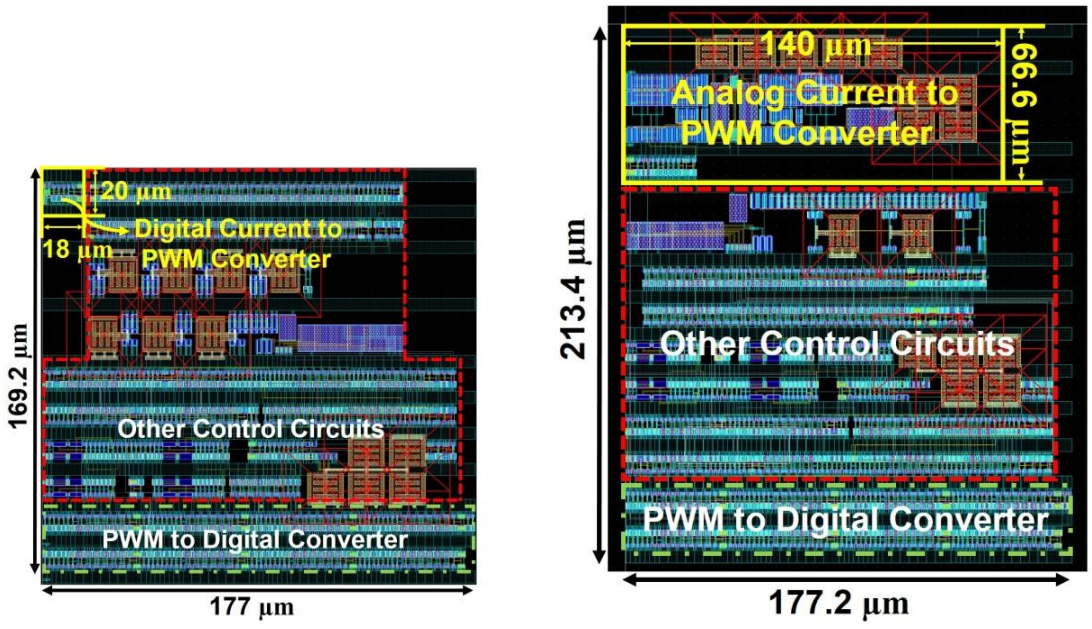


Figure 4: Schematic of the Miller two-stage operational amplifier

III. MEASUREMENT RESULTS AND ANALYSIS

The current to PWM converters were designed and post-layout simulated using a 65 nm CMOS process and the photodiode having C_{PD} of 28 pF [9]. Fig. 5 and Fig. 6 show the layouts and microphotography of the PWM readout circuits including the designed digital and analog CPC respectively. The digital and analog CPC occupy an active area of 360 μm^2 and 9324 μm^2. And whole chip sizes are 0.86mm x 0.96mm and 1.17mm x 0.96mm, respectively.



(a) **(b)**

Figure 5: Layouts of the PWM output readout circuits : (a) digital type and (b) analog type

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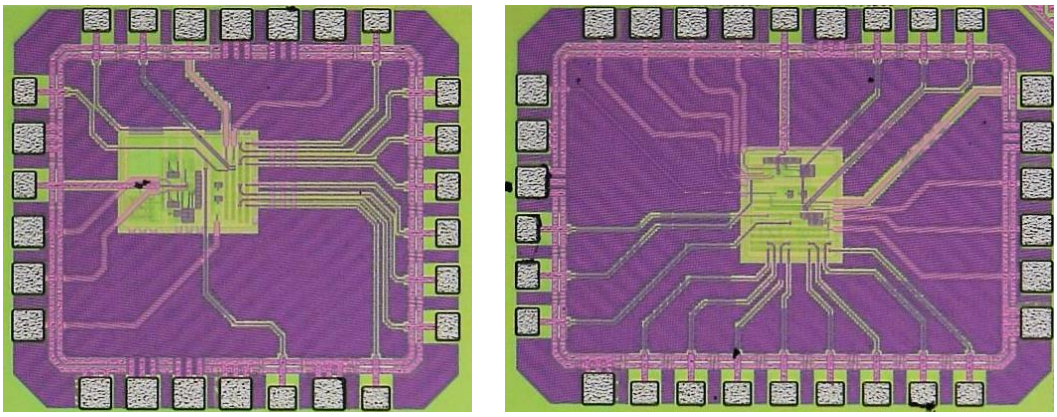
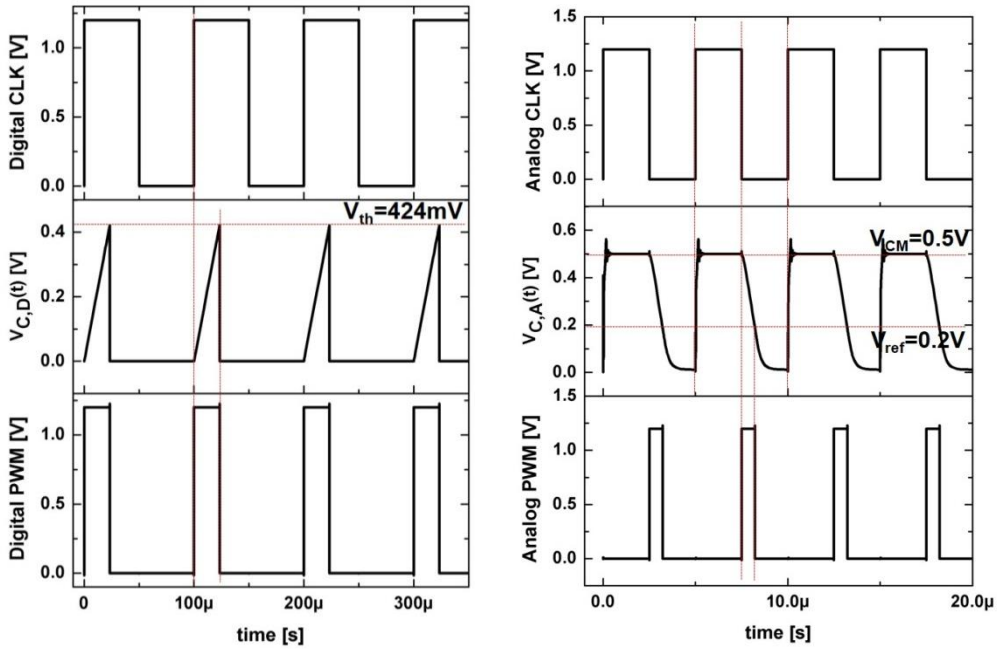


(a) (b)

Figure 6: Chip microphotography : (a) digital type and (b) analog type

Fig. 7 shows the post-layout simulation results of the digital CPC and the analog CPC when I_{PD} is 500 nA. The C_{PD} of 28 pF, C_f of 1 pF, V_{th} of 424 mV, V_{CM} of 500 mV and V_{ref} of 200 mV are designed and selected. Fig. 7 (a) shows the results of the digital CPC. When the clock is high, I_{PD} is converted into the pulse width which has the time of change from ground to V_{th}, resulting in the pulse width of 23.3 µs. Fig. 7 (b) shows the result of the analog CPC. The analog CPC performs the conversion operation when the clock is low, and performs the reset operation that $V_{C,A}(t)$ is reset to V_{CM} of 500 mV when the clock is high. The $V_{C,A}(t)$ decreases from V_{CM} with time as opposed to the digital CPC. I_{PD} is converted to the pulse width of 721 ns, which is the time of change from V_{CM} to V_{ref}.



(a) (b)

Figure 7: Post-layout simulation results : (a) digital type and (b) analog type

Fig. 8 summarizes the pulse width obtained by the post-layout simulation and the calculation obtained by Eq. (2) and (3) of the digital and analog CPC according to I_{PD} when C_{PD} is 28 pF. In case of the same I_{PD}, the analog CPC outputs the shorter pulse width than the digital. Based on these results, the operating frequency of the digital CPC is in the range of 500 Hz to 1 MHz, and the analog CPC has the operating frequency of 100 kHz to 10 MHz. In the effect capacitor of the PWM signal, C_{PD} of 28 pF directly affects the PWM signal in the digital CPC, but the analog CPC is affected by C_f of 1pF. The analog CPC has the faster operating speed than the digital because of the difference of $C_{CPC,eff}$.

In the comparison of simulations and the calculation results of equations (2) and (3), the digital CPC has almost the same values of the calculation and simulation results, but at less than 10nA, the digital CPC shows the difference between the calculated and the simulated values. The SW1 is a switch implemented by an NMOS that has a leakage current of few nA level. When I_{PD} of several nA is applied, the effect of the leakage current increases, and the RC circuit by an off resistance of the SW1 and C_{PD} is dominant. For this reason, the difference of the simulation and calculation results increases at I_{PD} of nA level in the digital CPC. On the other hand, the analog CPC shows the distinct difference of the calculated value by Eq. (3) and the simulated pulse width. This is due to a clock feed through, a switch charge injection and an offset in the TIA. To solve this problems, techniques such as 'correlated double sampling' are additionally required [4].

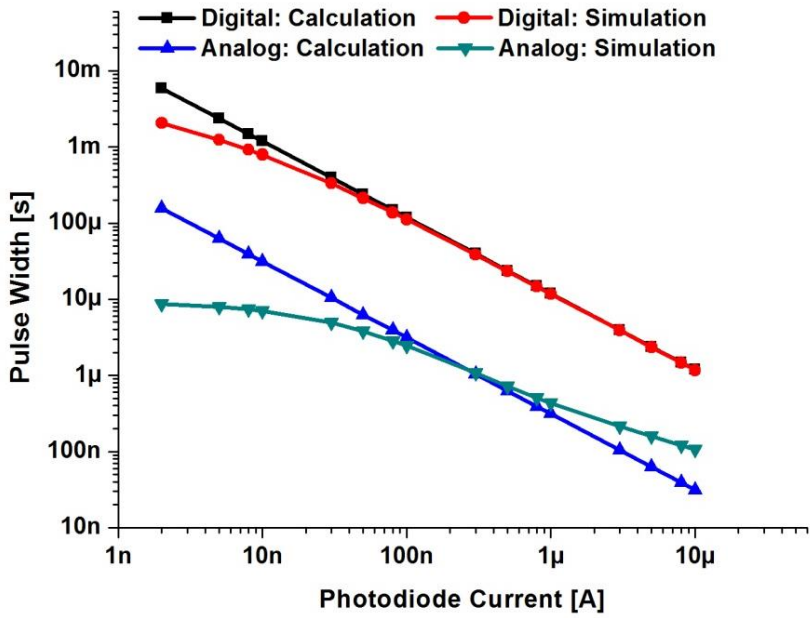


Figure 8: Measured pulse width with respect to photodiode current with 28pF of C_{PD}

Fig. 9 compares the pulse width according to C_{PD} when I_{PD} is 100nA. The digital CPC and the analog CPC increases with the increasing C_{PD}, but the analog CPC has the narrow variation than the digital because of the difference of $C_{CPC,eff}$. In other words, it means that the effect of the additional parasitic capacitors generated by wire bonding and PCB is more sensitive to the digital CPC.

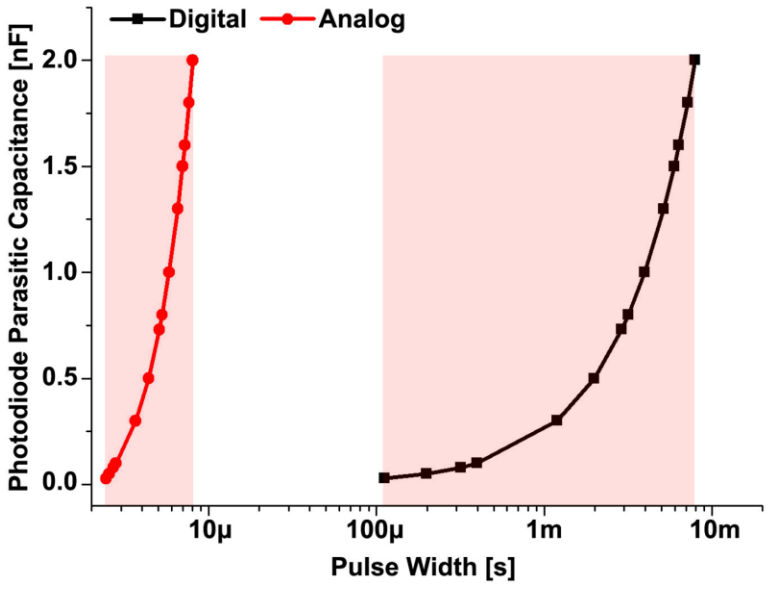


Figure 9: Measured pulse width with respect to photodiode current with 28pF of C_{PD}

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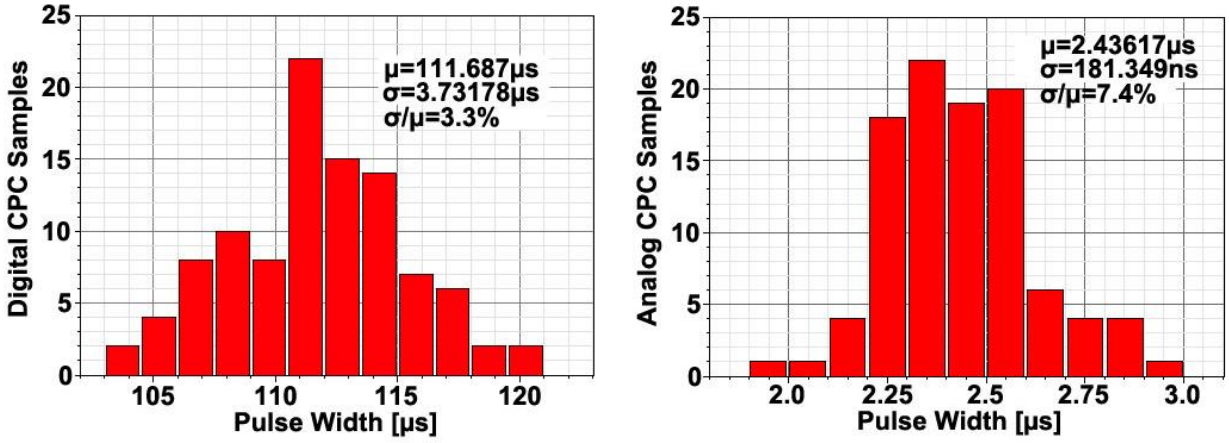
The histograms of the pulse width with 100-point Monte Carlo simulation at I_{PD} of 100 nA and C_{PD} of 28 pF is shown in Fig. 10. The average pulse width of the digital CPC was about 111.687 µs in this simulations, and the coefficient of process variation (σ/µ) was 3.3 %. The average pulse width of the analog CPC was about 2.44 µs, and the coefficient of process variation was 7.4 %. In the case of the digital CPC, V_{th} of the detection inverter which is one of the parameters determining the pulse width affected by the process variation. On the other hand, the analog CPC is more sensitive to the process variation because it has more factors affected by the process variation than the digital, the performance of the OTA of the TIA, the integrated C_f, and the performance of the comparator that are the performance and parameters affecting the conversion from I_{PD} to the PWM signal.



(a) **(b)**

Figure 10: Distribution of the pulse width with 100-point Monte Carlo analysis at 100nA of I_{PD} and 28pF of C_{PD}: (a) digital type and (b) analog type

Table 1 compares the performance of the digital and analog CPC. The digital CPC can be implemented in smaller area and has smaller power consumption than the analog. On the other hand, because of the difference of the capacitor affecting the PWM conversion, the analog CPC of the operating speed is faster than the digital, and the analog CPC can detect the smaller current at the same parasitic capacitance and the operating clock frequency. However, the PWM signal of the analog CPC is much different from the calculated value due to the effects by the capacitive TIA, and is also sensitive to the process variation than the digital.

TABLE I: Comparison between analog and digital current to PWM converter

	Digital Current to PWM Converter	**Analog Current to PWM Converter**
Area (Core)	Small (360 µm^2)	Large (9,324 µm^2)
Power Consumption (only CPC)	Low (10 µW)	High (214.2 µW)
Minimum detectable current (@C_{PD}=28pF, Clock=200kHz)	5 µA	100 nA
Operating frequency	500 Hz ~ 1 MHz	100 kHz ~ 10 MHz
Variation by the parasitic capacitor	High	Low
Coefficient of process variation	3.3%	7.4%

IV. CONCLUSIONS

In this paper, a comparison between the analog and digital current to PWM converter is presented. The comparison was carried out through post-layout simulations using 65 nm CMOS process. An analog and a digital implementation for the same current to PWM converter have its own advantages and disadvantages. Important performances depend on sensor applied to applications. The digital current to PWM converter that occupies small area and consumes small power is advantageous to IoT and biomedical applications, but in automobile and industry applications, the analog current to PWM converter that has a faster operating speed and a minimum detectable current is more suitable.

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