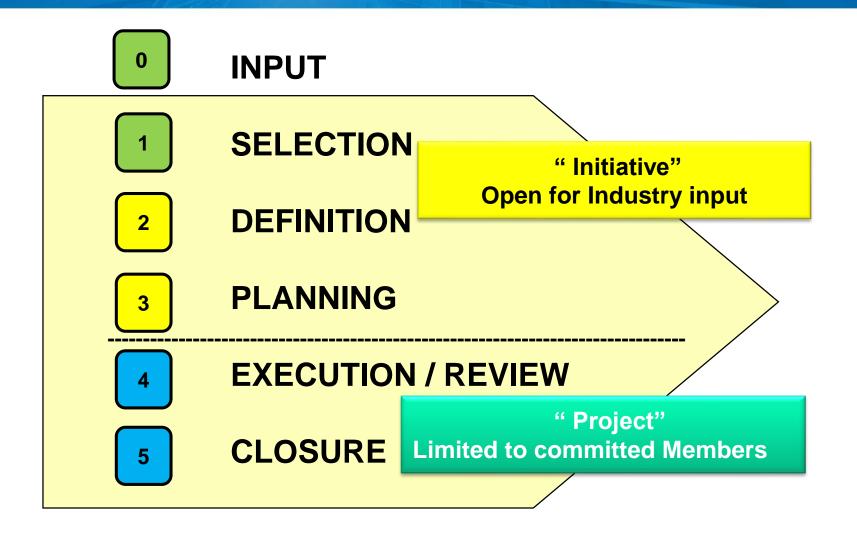
### **Approaches to minimize Printed Circuit Board (PCB) warpage in Board Assembly Process to improve SMT Yield**

Initiative Leaders: Srini Aravamudhan & Chris Combs, Intel; iNEMI Staff: Haley Fu



### **The Project Development Process - 5 Steps**





## **Project Proposal**

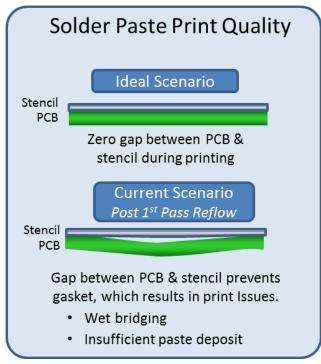
**The Starting Point** 

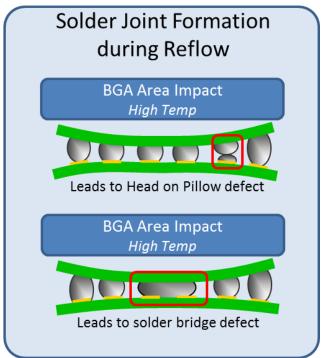


### **Background**

PCB with thickness ≤ 40mils (1.0mm) are driving higher PCB warpage in board assembly process leading to lower assembly yields and higher rework for some components

SMT yield depends on many factors including package warpage, PCB warpage, SMT materials, process, etc.





**Uncontrolled PCB Warpage leads to Print and SMT defects** 



#### **Problem Statement**

- PCB warpage at room temperature and elevated temperature impacts board assembly
  - Lack of industry specification for PCB warpage at room temperature and elevated temperature
- IPC-A-610E specification for incoming PCB warpage is not sufficient to address PCB warpage at elevated assembly reflow temperature
  - Bow and twist should not exceed 0.75% for surface mount board application as per IPC-TM-650
- Need to identify factors and guidelines to minimize PCB warpage during the SMT assembly process

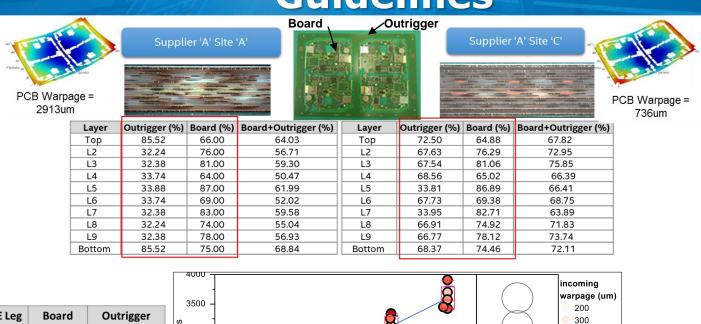


### **Proposed Mitigation to Problems**

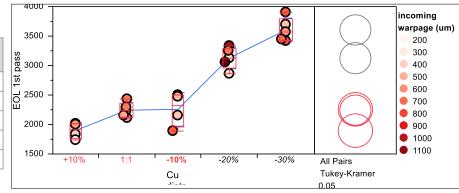
- Guidelines for PCB design on
  - Copper balancing across PCB layers
  - Outrigger Board area copper balancing
  - Outrigger tab size and placement
  - PCB location impact within panel during PCB fabrication
- Guidelines on Reflow pallet design
  - Design features
  - Pallet materials
- Other uncovered factors / solutions to minimize PCB warpage in SMT assembly process



# Potential Mitigation Paths for PCB Design Guidelines

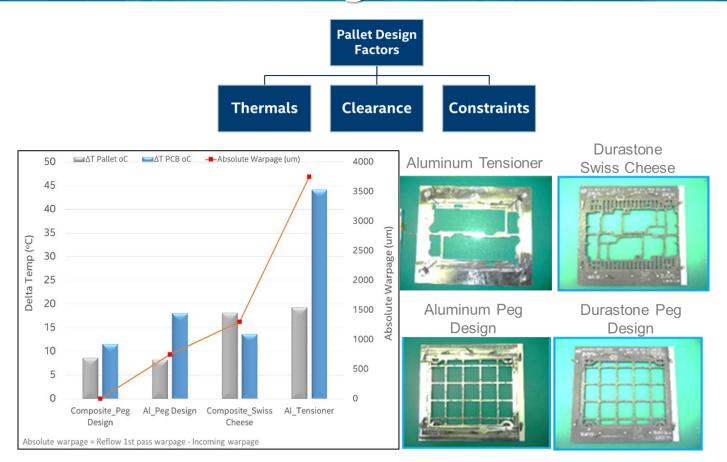


DOE Leg	Board Copper	Outrigger Copper
1:1	67 to 91%	67 to 91%
+10%	67 to 91%	77 to 87%
-10%	67 to 91%	57 to 81%
-20%	67 to 91%	47 to 71%
-30%	67 to 91%	37 to 61%



- Unbalanced copper ratio between outrigger and board area leads to varying rates of thermal expansion in reflow and drives warpage in PCB
- Recommend for each layer that the outrigger copper content to be 1:1 or greater (100-120%) of the single board image to minimize panel warpage

# Potential Mitigation Paths for Reflow Pallet Design Guidelines



- Thermal mismatch (ΔT) across the PCB due to the Pallet design (overlap heatsink effect) is the primary factor that drives panel warpage post 1<sup>st</sup> pass reflow
- Pallet material also plays a role in warpage reduction



### **Project Proposal**

#### **Objective:**

- To identify factors that influences PCB warpage and solutions to mitigate the warpage in the SMT assembly process
- Scope
  - PCB Design factors
    - Thickness ≤ 1.0mm
    - Multi-up PCB with outrigger design
    - OSP surface finish
    - Outrigger tab size and location
  - PCB fabrication process
    - Location of PCB in manufacturing panel
    - Other PCB fabrication processes and factors
  - Equipment/tooling
    - HVM reflow pallet design features
    - Reflow pallet material (Aluminum vs. Composite)
    - Reflow oven and PCB support options
  - Other factors identified through the project...



### **Proposed Steps**

Step#	Description	Expected Outputs
1	As a group brainstorm to identify and prioritize factors that influences PCB warpage	<ul> <li>Prioritized list of factors to study and characterize the impact to PCB warpage (examples shown below)</li> </ul>
2	Identification of PCB design & fabrication factors for evaluation	<ul> <li>Identify factors and DOEs for evaluation</li> <li>Align on metrology to measure warpage</li> <li>Alignment on PCB design &amp; fabrication guidelines to be evaluated</li> </ul>
3	Identification of reflow pallet and board support factors for evaluation	<ul> <li>Identify factors and DOEs for evaluation</li> <li>Align on metrology to measure warpage</li> <li>Alignment on Reflow pallet design &amp; board support to be evaluated</li> </ul>
4	PCB design & fabrication guidelines evaluation	<ul> <li>Determine the impact of PCB design &amp; fabrication guidelines to PCB warpage and validate the guidelines</li> <li>Finalize PCB design &amp; fabrication guidelines to minimize warpage at Room Temp and High Temp</li> </ul>
5	Reflow pallet design & board support guidelines evaluation	<ul> <li>Determine the impact of Reflow pallet design &amp; board support guidelines to PCB warpage and validate the guidelines</li> <li>Finalize Reflow pallet design &amp; support guidelines to minimize warpage at Room Temp and High Temp</li> </ul>
6	Publish Final Report	Completed report on all project outputs



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