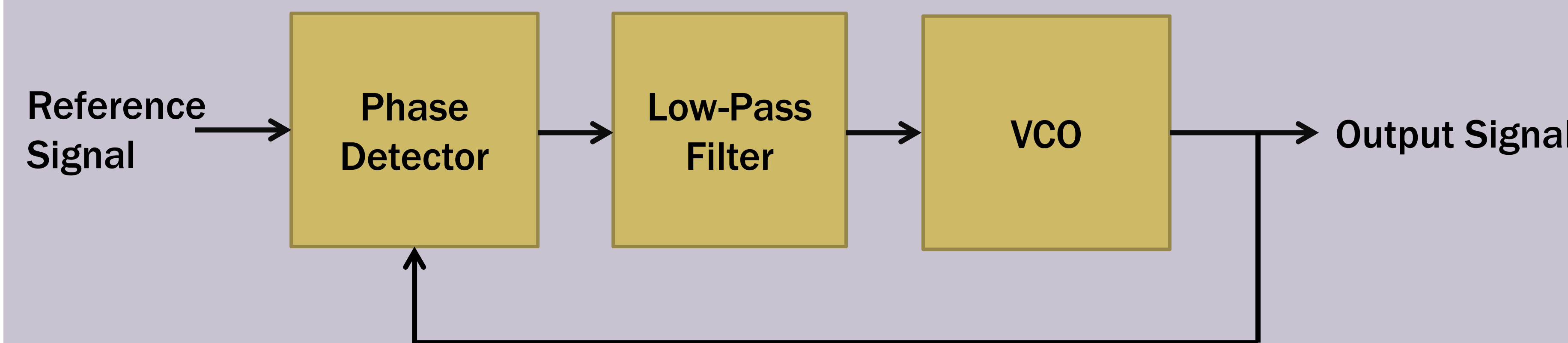
A TUTORIAL APPROACH TO ANALOG PHASE-LOCKED LOOPS

By Angsuman Roy

PRESENTATION OUTLINE

- Introduction and Terminology
- Analog PLLs
- Phase Detector (Mixer)
- Voltage-Controlled Oscillator
- Low-Pass Filter and Damping
- Applications
  - Frequency Synthesis
  - FM Demodulation

INTRODUCTION



Basic Structure of a PLL

TERMINOLOGY

Analog PLL (APLL)

- Multiplying circuit (mixer) used for phase detector
- Other components are analog

Digital PLL (DPLL)

- Mixer replaced with XOR gate or phase frequency detector (PFD)
- Other components are unchanged

All Digital PLL (ADPLL)

- XOR Gate or PFD
- Other components are digital or numerically controlled.

WHY ANALOG PLLS?

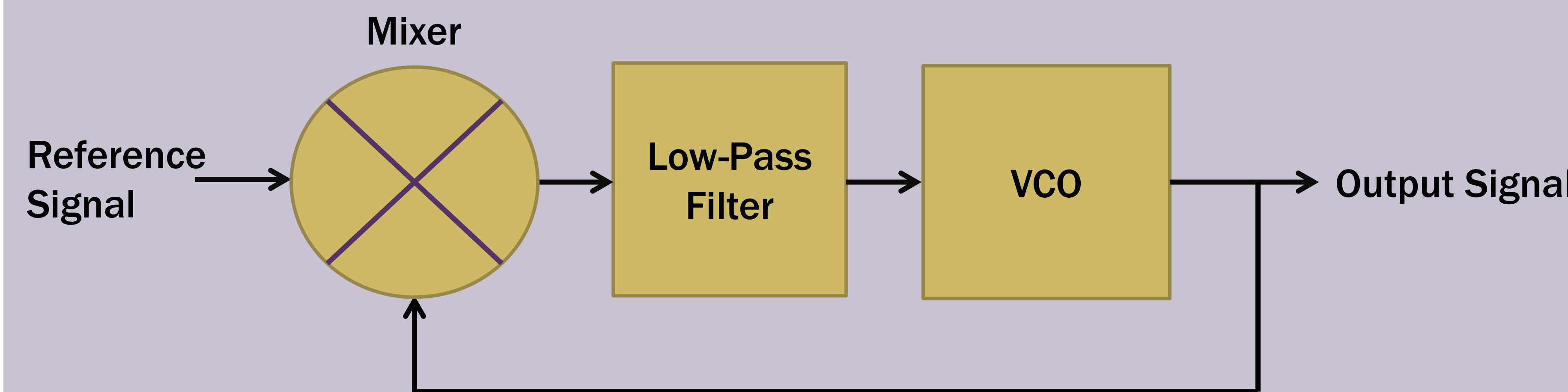
Used for RF Circuits

Wide Tuning Range

Low Noise

Many Adjustable Parameters

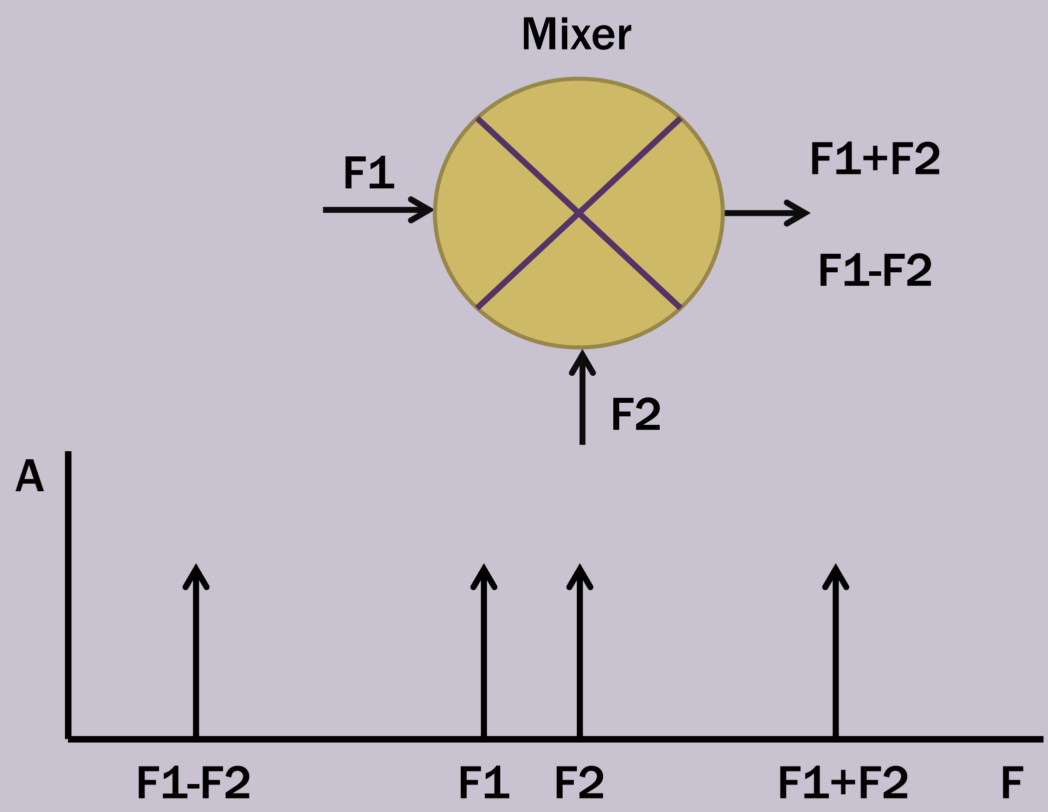
APLL BLOCK DIAGRAM



Basic Structure of a PLL

WHAT IS A MIXER?

A mixer takes two input frequencies and outputs their sum and difference from the process of multiplication.



MATH

$$V_1(t) = A_1 \cdot \sin(2\pi f_1 \cdot t)$$

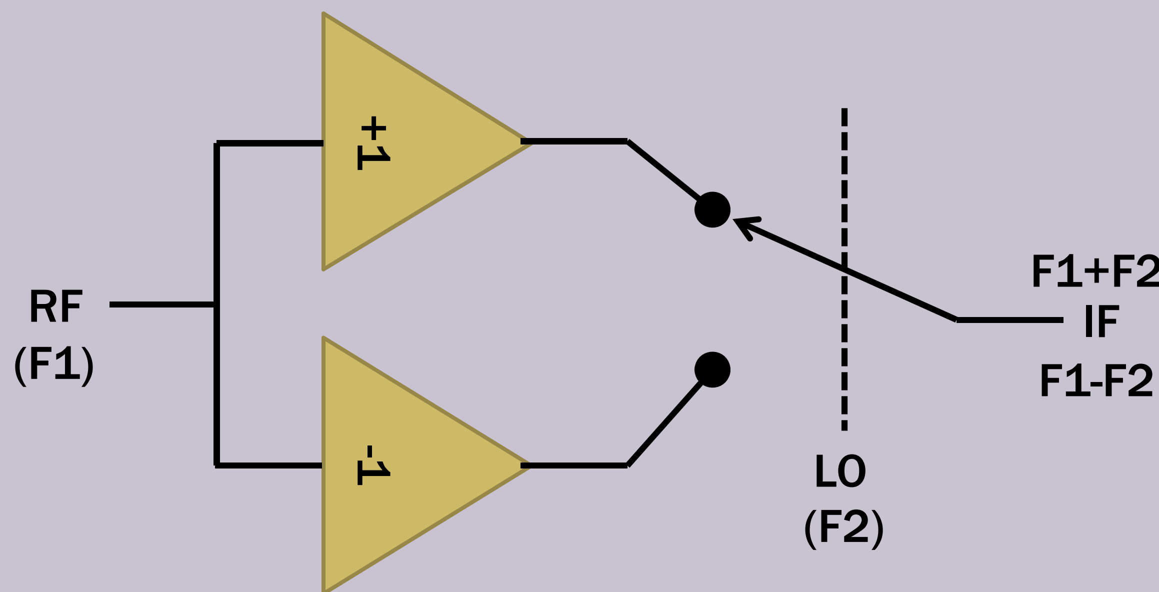
$$V_2(t) = A_2 \cdot \sin(2\pi f_2 \cdot t)$$

$$V_1(t) \cdot V_2(t) = \sin(2\pi f_1 \cdot t) \cdot \sin(2\pi f_2 \cdot t)$$

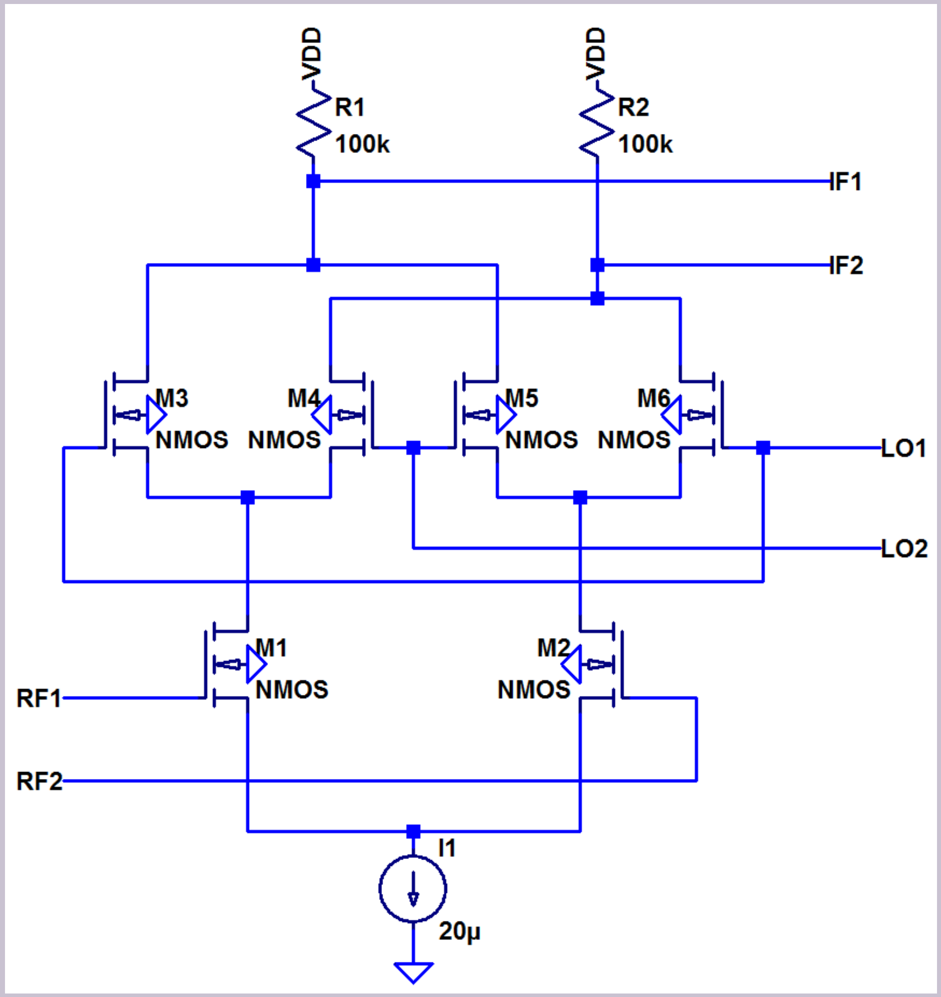
$$\boxed{\textit{Trigonometric Identity}: \sin(a) \cdot \sin(b) = \frac{1}{2}[\cos(\mathrm{a} - \mathrm{b}) - \cos(\mathrm{a} + \mathrm{b})]}$$

$$V_1(t) \cdot V_2(t) = \frac{1}{2}(A_1 \cdot A_2) \cdot \; [\cos(2\pi\underbrace{(f_1 - f_2)}_{\text{Difference}}t) - \cos(2\pi\underbrace{(f_1 + f_2)}_{\text{Sum}}t)]$$

CONCEPTUAL DIAGRAM



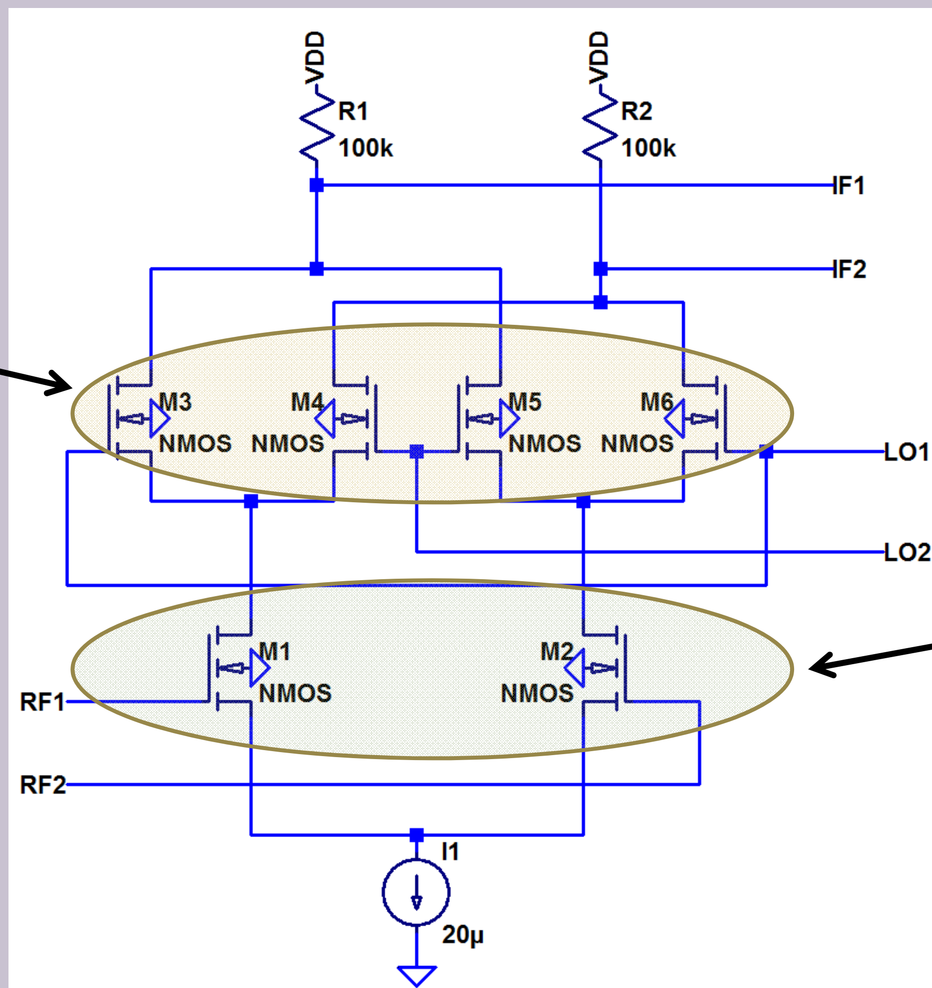
MIXER DESIGN:4 QUADRANT MULTIPLIER



4 QUADRANT MULTIPLIER DEVICE SIZES

1.8u/0.6u
min size devices

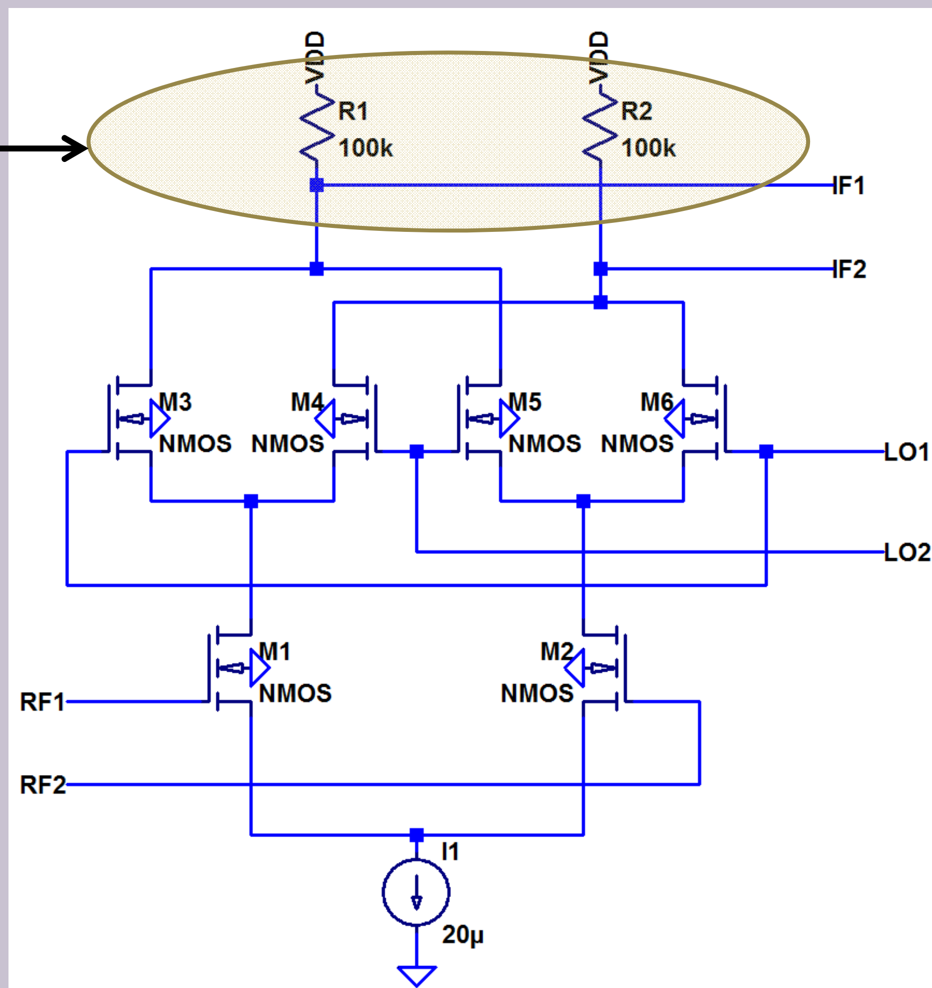
for speed



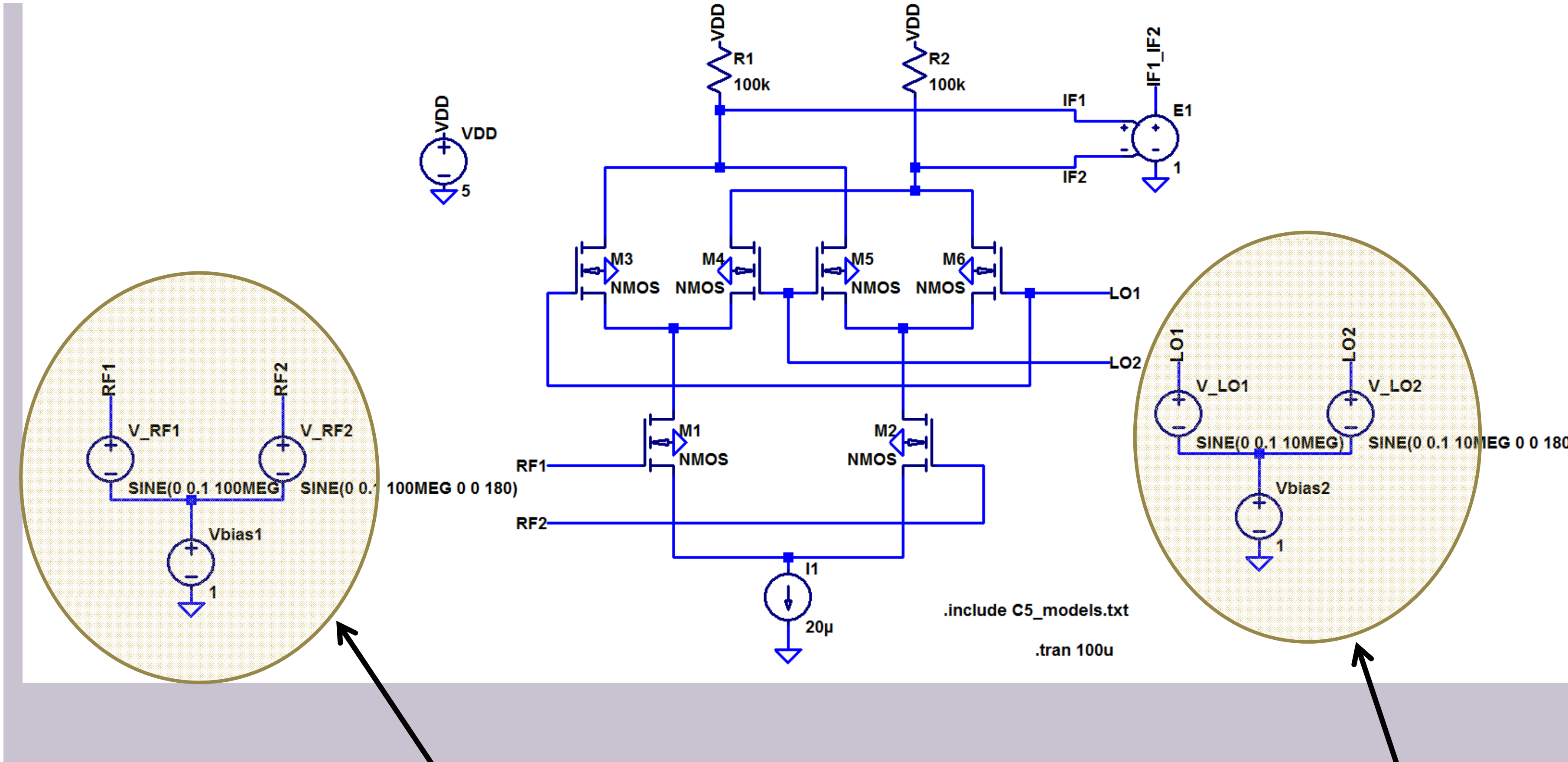
6u/0.6u for current
sinking ability

4 QUADRANT MULTIPLIER GAIN

Output voltage is developed across these resistors



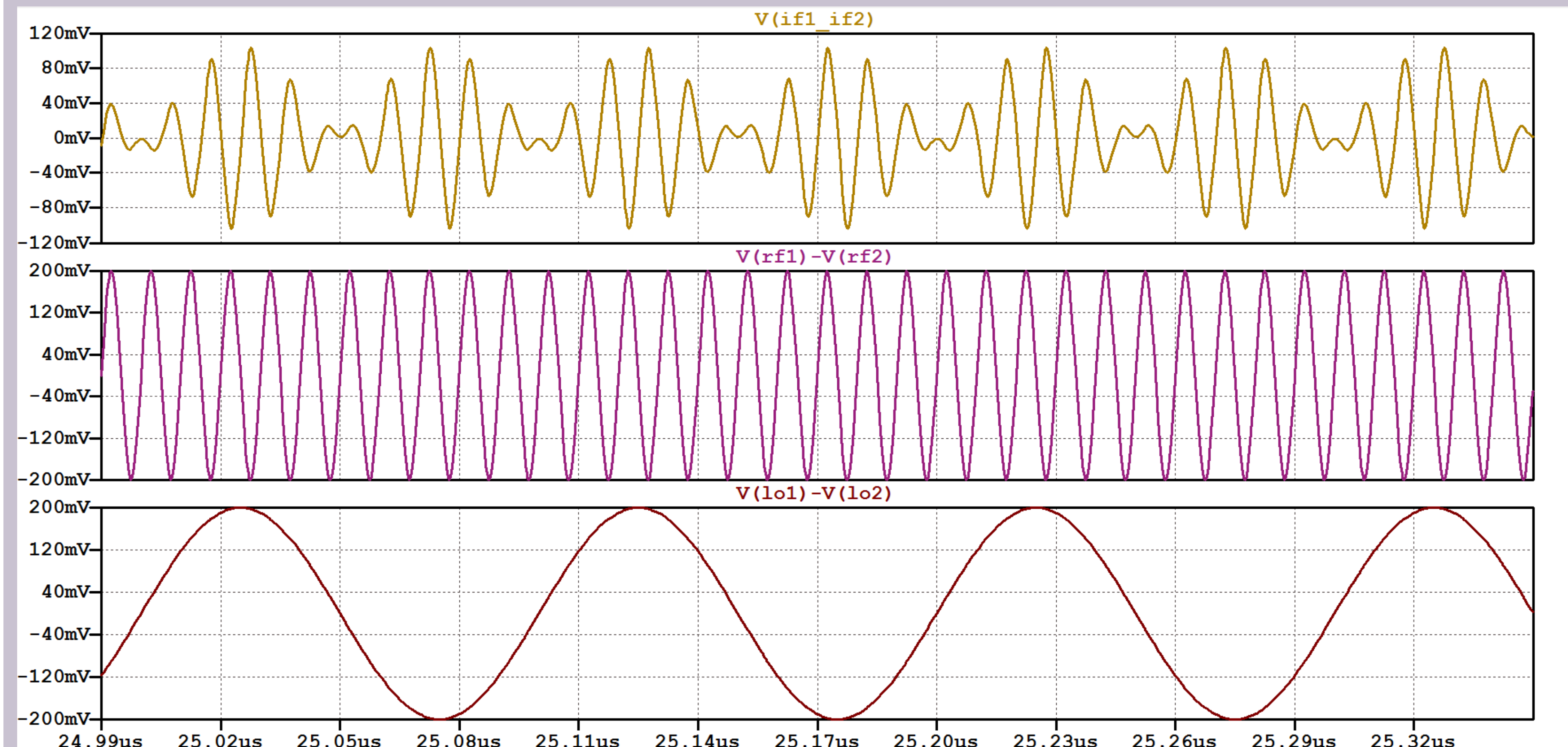
AC OPERATION OF THE MIXER



Differential sine input with bias voltage represents RF input of 100 MHz

Same, but LO input of 10 MHz

TIME DOMAIN VIEW OF INPUTS/OUTPUT

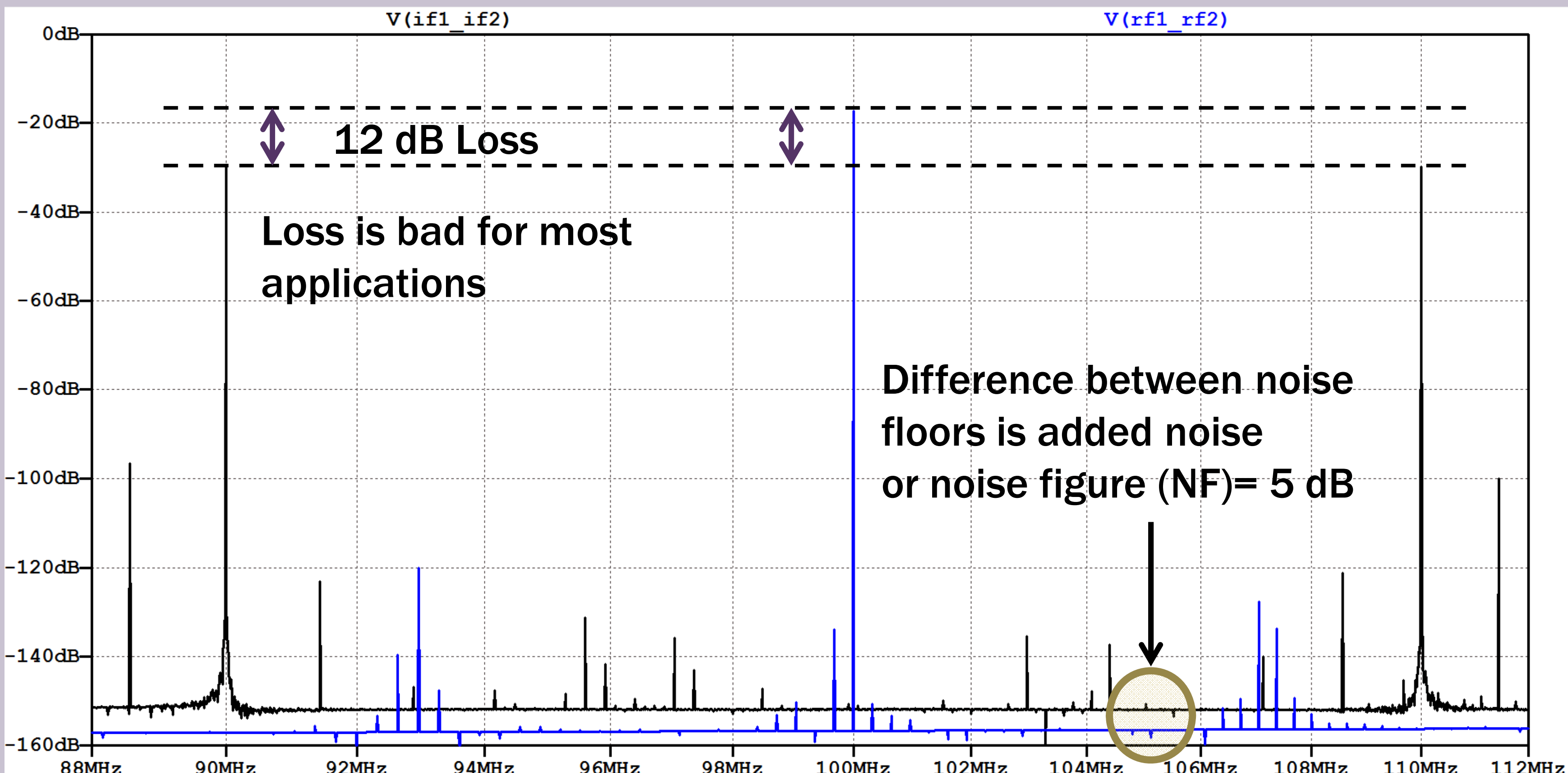


FFT OF IF OUTPUT

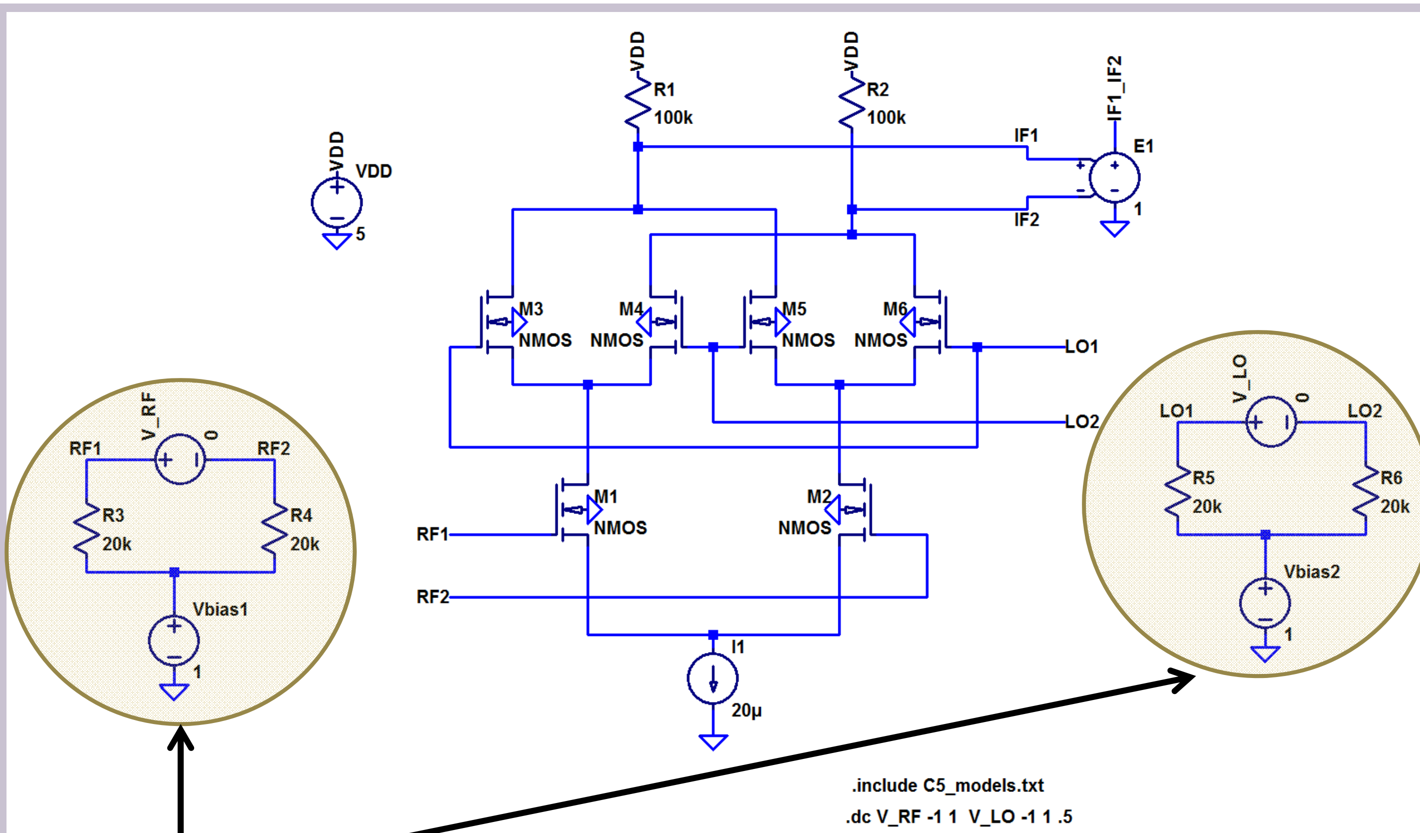
Difference frequency: 90 MHz

Sum frequency: 110 MHz

GAIN AND NOISE



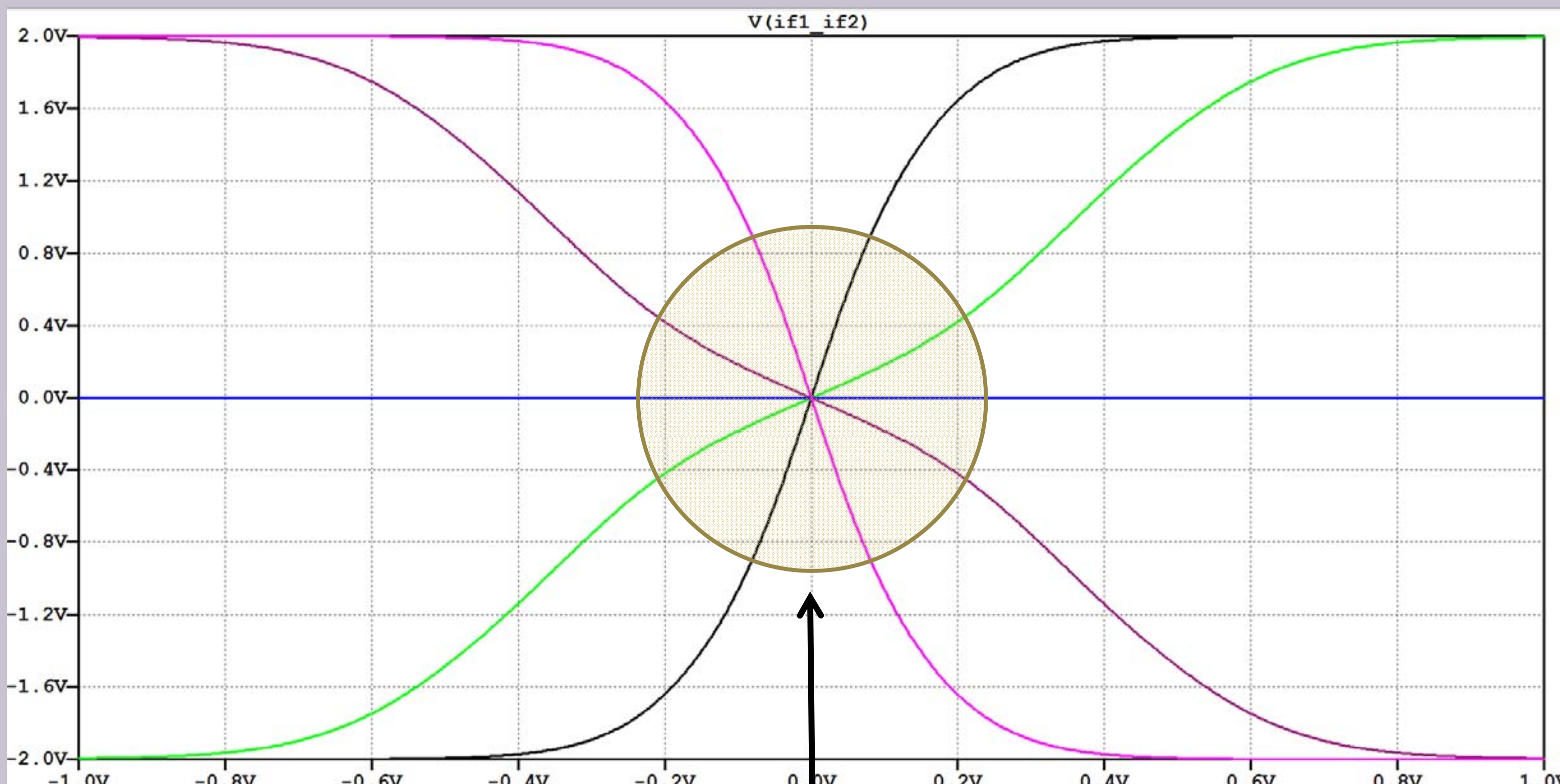
4 QUADRANT MULTIPLIER GAIN



Network to allow for sweeping differential voltages while keeping a fixed bias.

.dc V_RF -1 1 V_LO -1 1 0.5

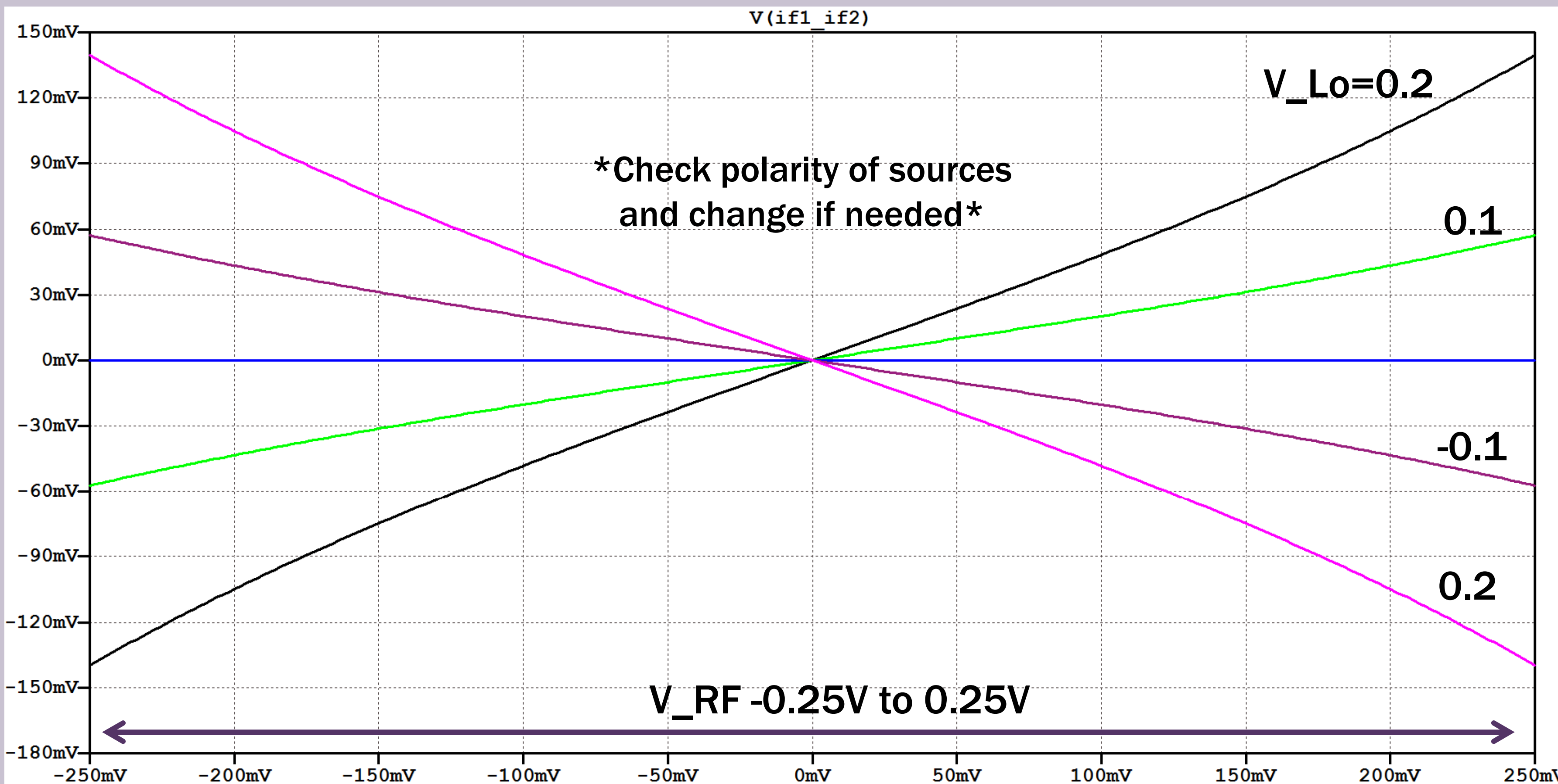
4 QUADRANT MULTIPLIER GAIN



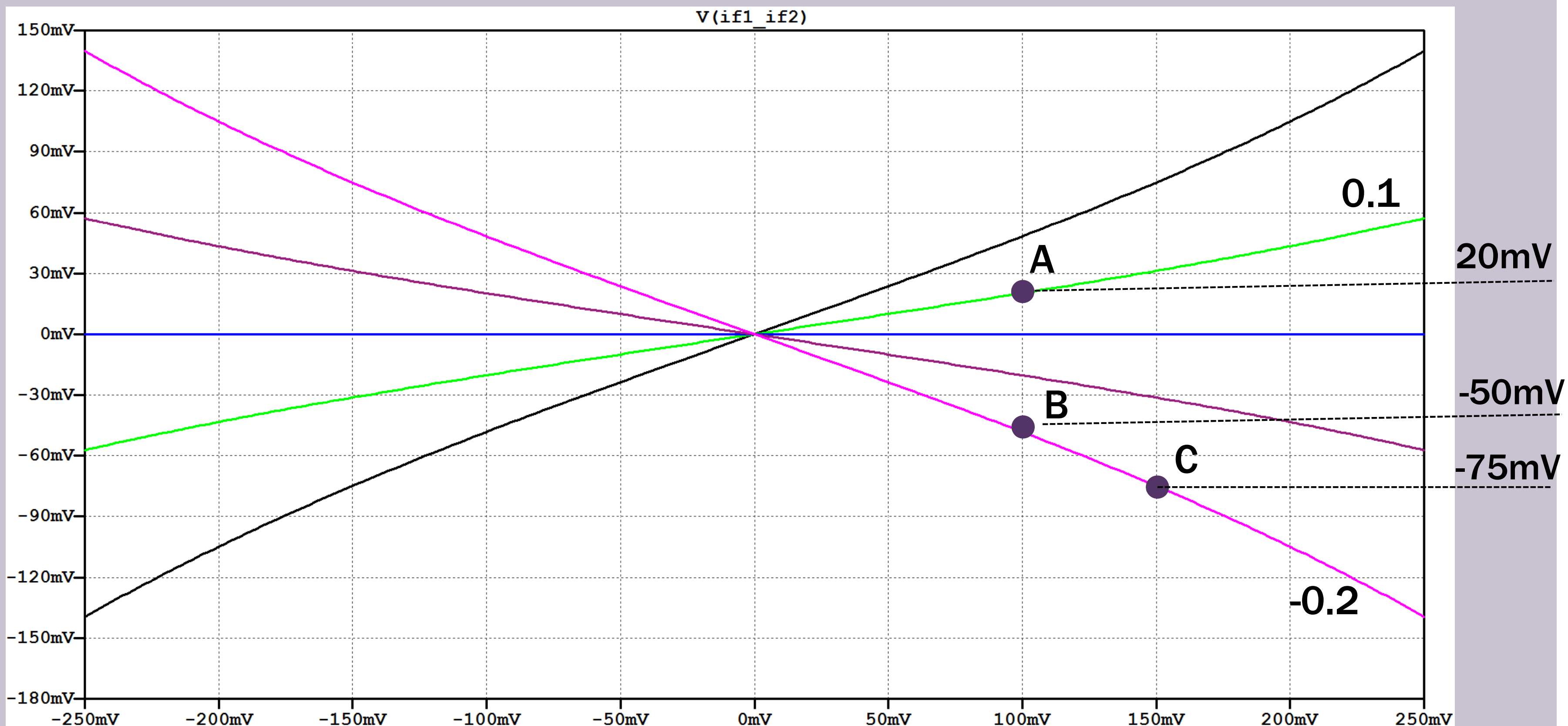
Linear only for small signals

4 QUADRANT MULTIPLIER GAIN

Changed sweep and step settings to show linear region better



LET'S MULTIPLY



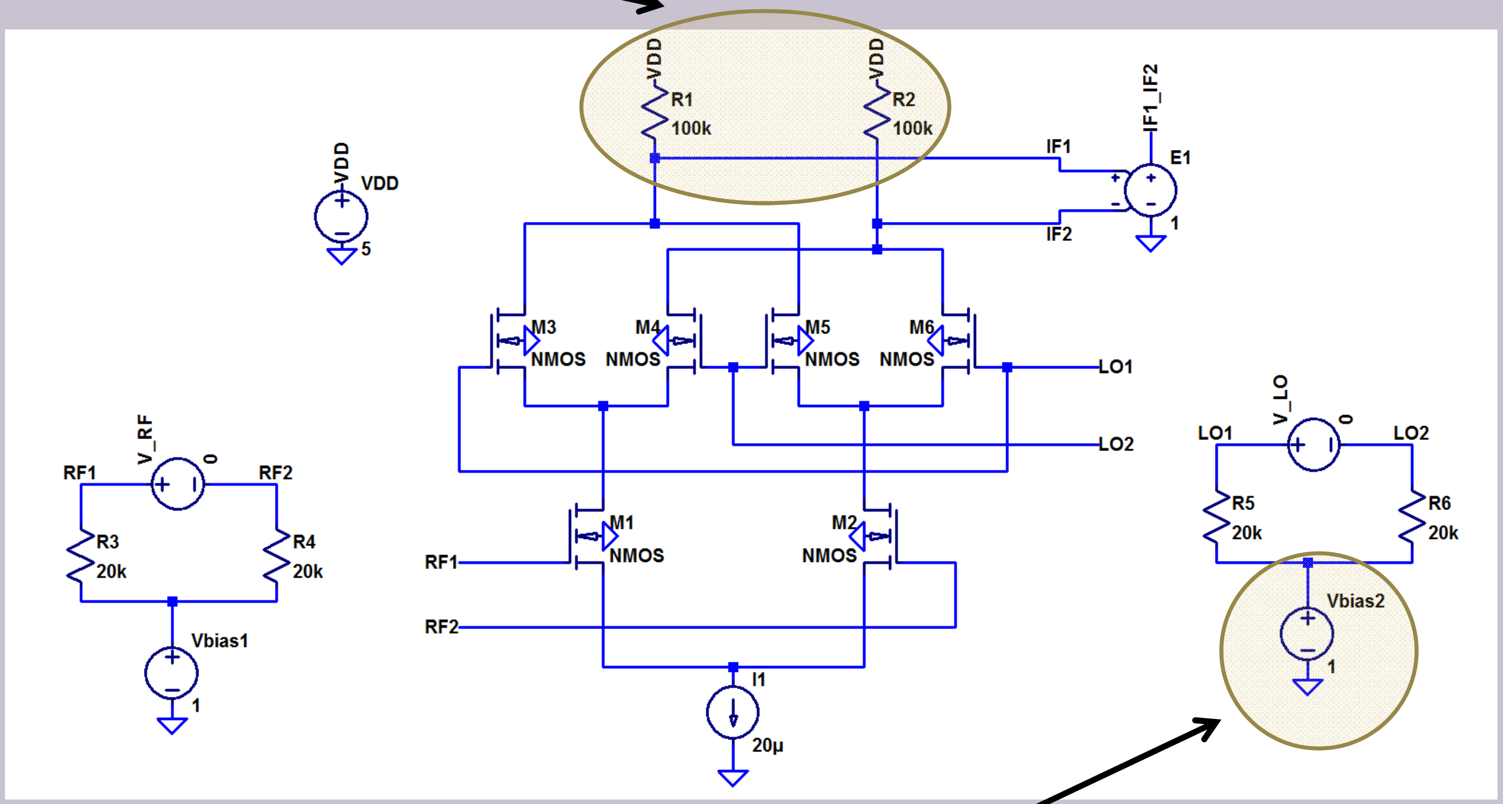
Point A: K*(0.1V * 0.1V) = 0.02V →K=2

Point A: K*(0.1V * -0.2V) = -0.05V →K=2.5

Point C: K*(0.15V * -0.2V) = -0.075V →K=2.5

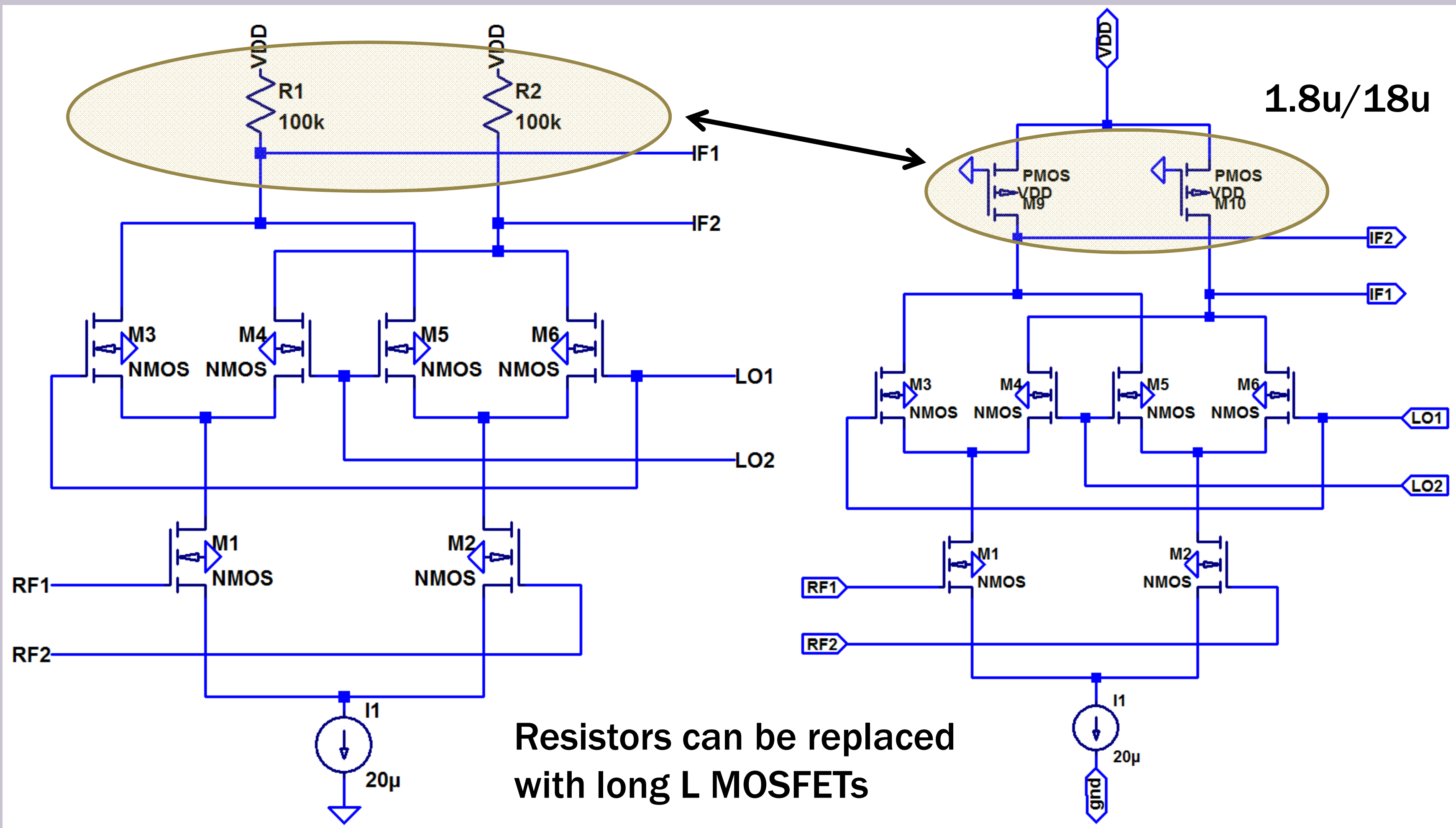
INCREASING GAIN

Increasing the value of these resistors increases gain but reduces load driving ability.



Increasing the bias voltage increases gain and allows for variable gain.

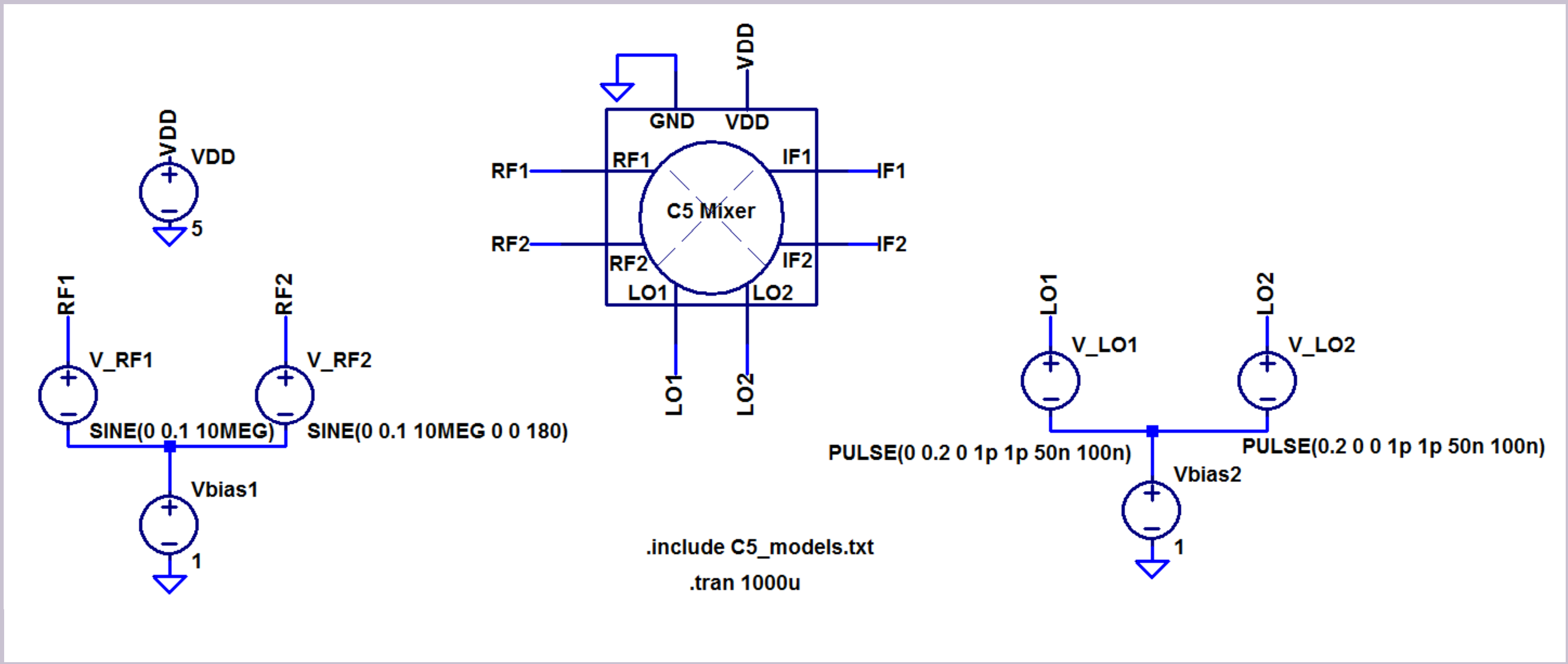
REPLACING RESISTORS



Resistors can be replaced with long L MOSFETs

MIXER AS PHASE DETECTOR

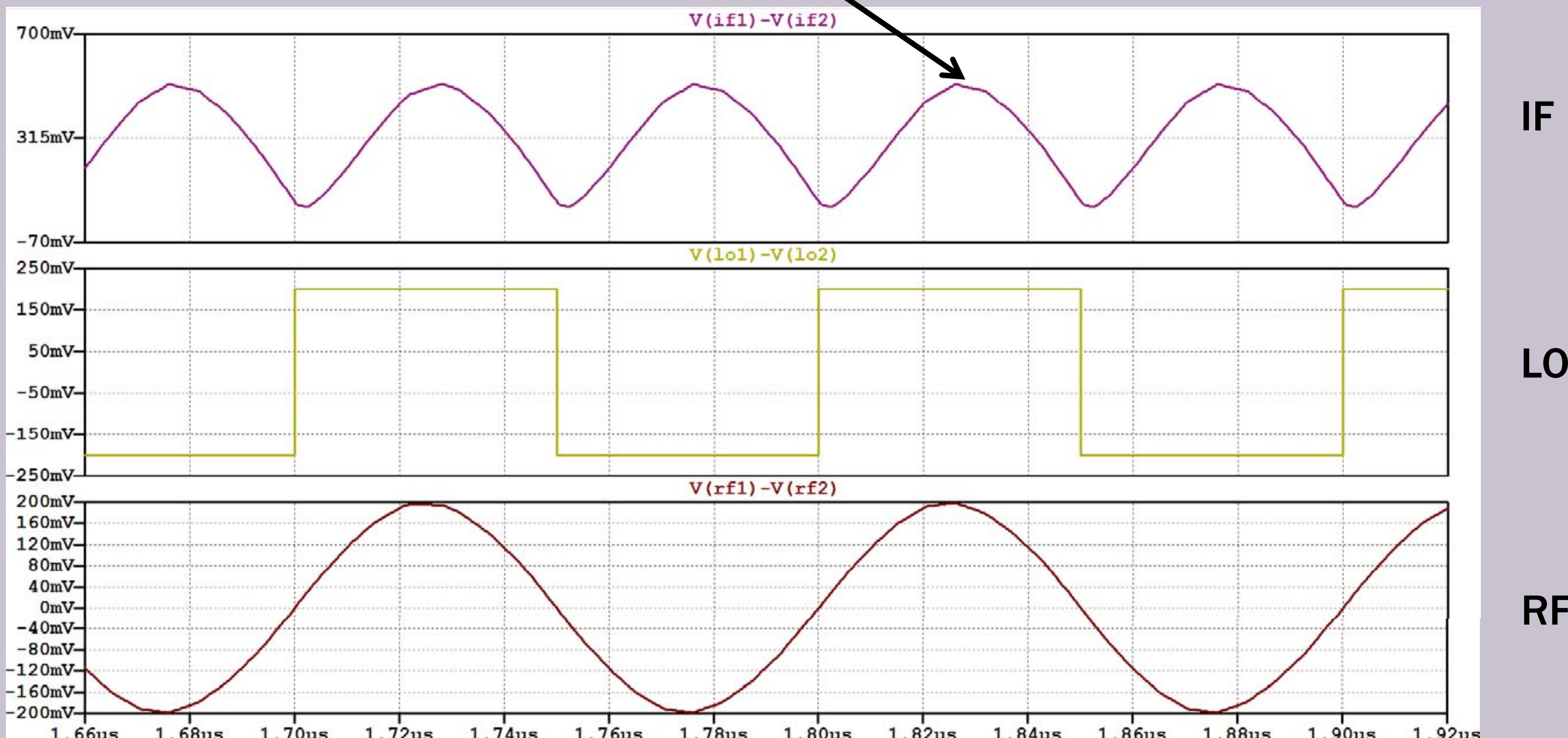
When both RF and LO frequencies are the same, the mixer operates as a phase detector.



Simulation test set-up

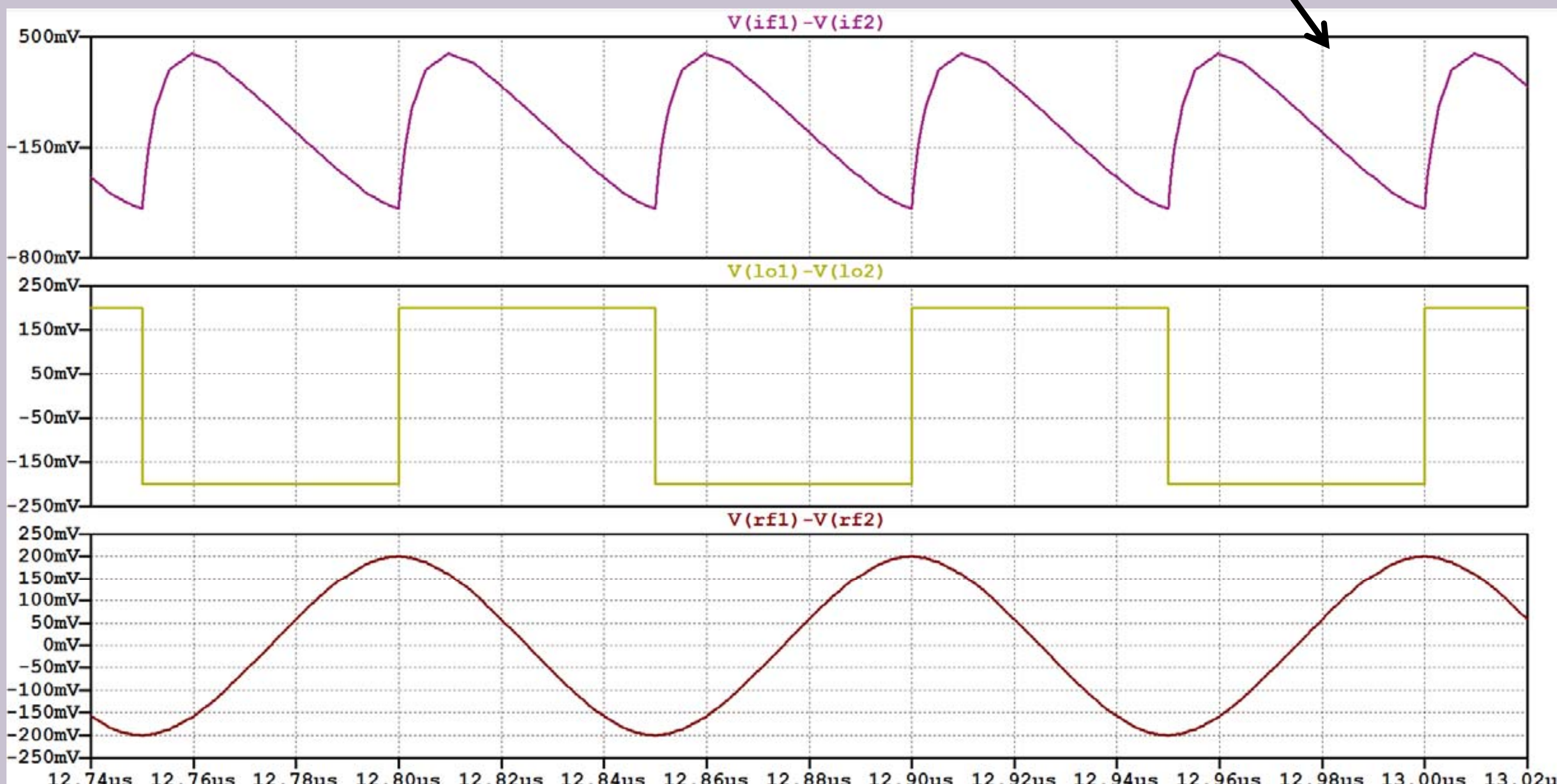
NO PHASE DIFFERENCE

IF output is rectified at twice the RF/LO frequency.
Averaging this will result in some DC value.



90 DEGREE PHASE DIFFERENCE

IF output appears to have zero average value.



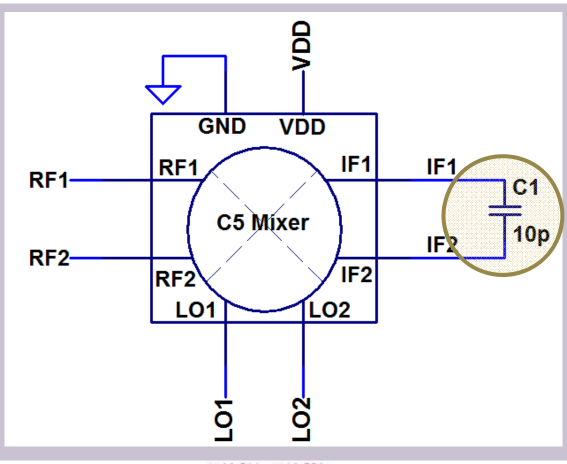
IF

LO

RF

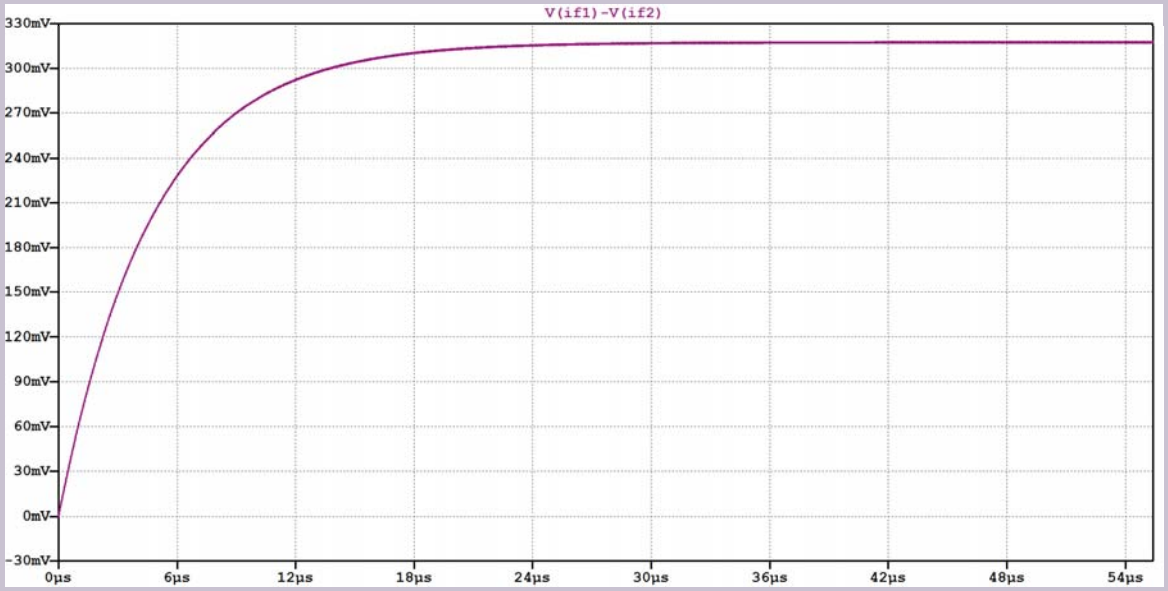
There is a relationship between average IF voltage and phase between LO and RF.

FILTERING THE IF OUTPUT



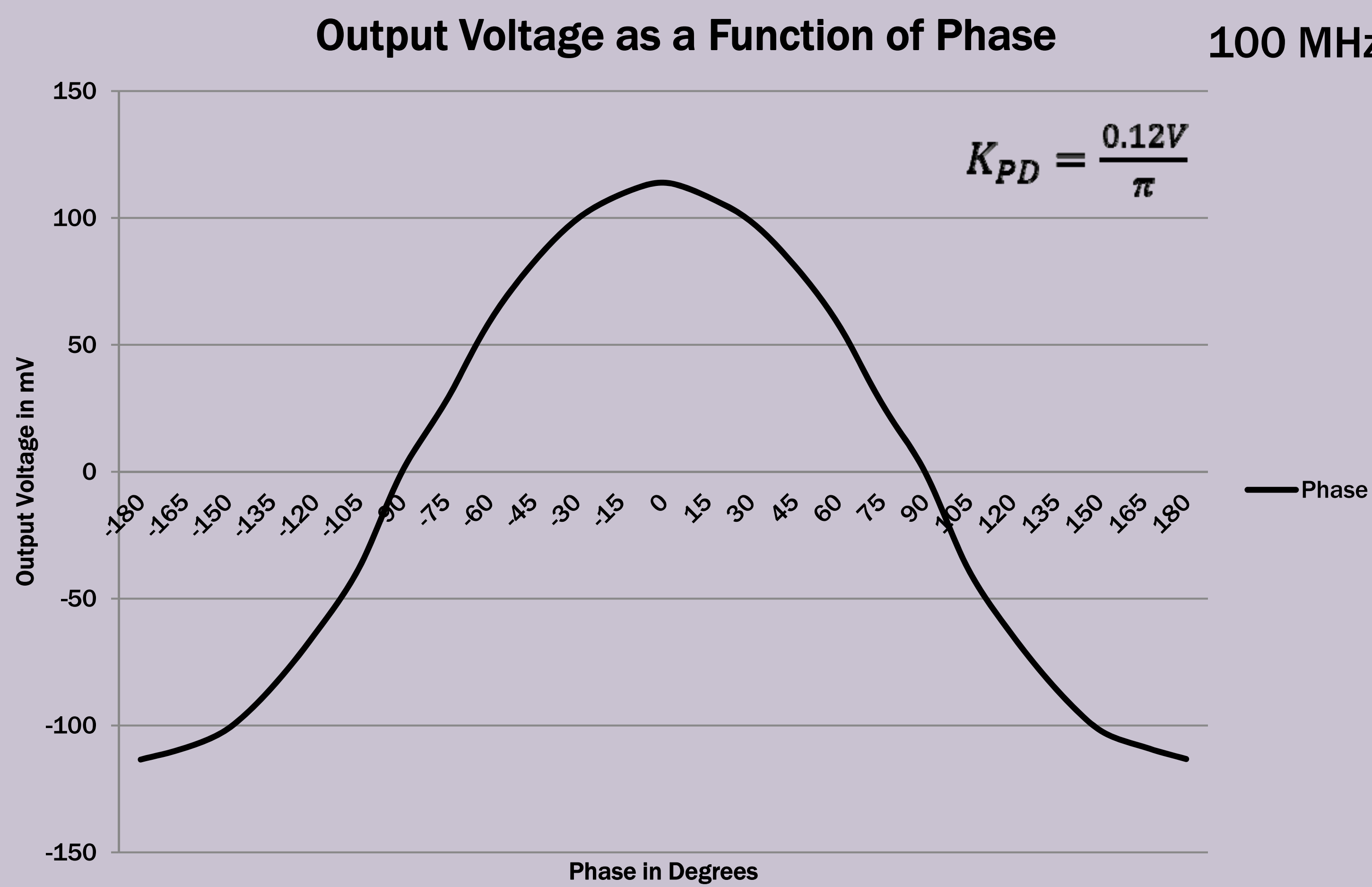
Capacitor to filter IF output

IF output is now a DC value

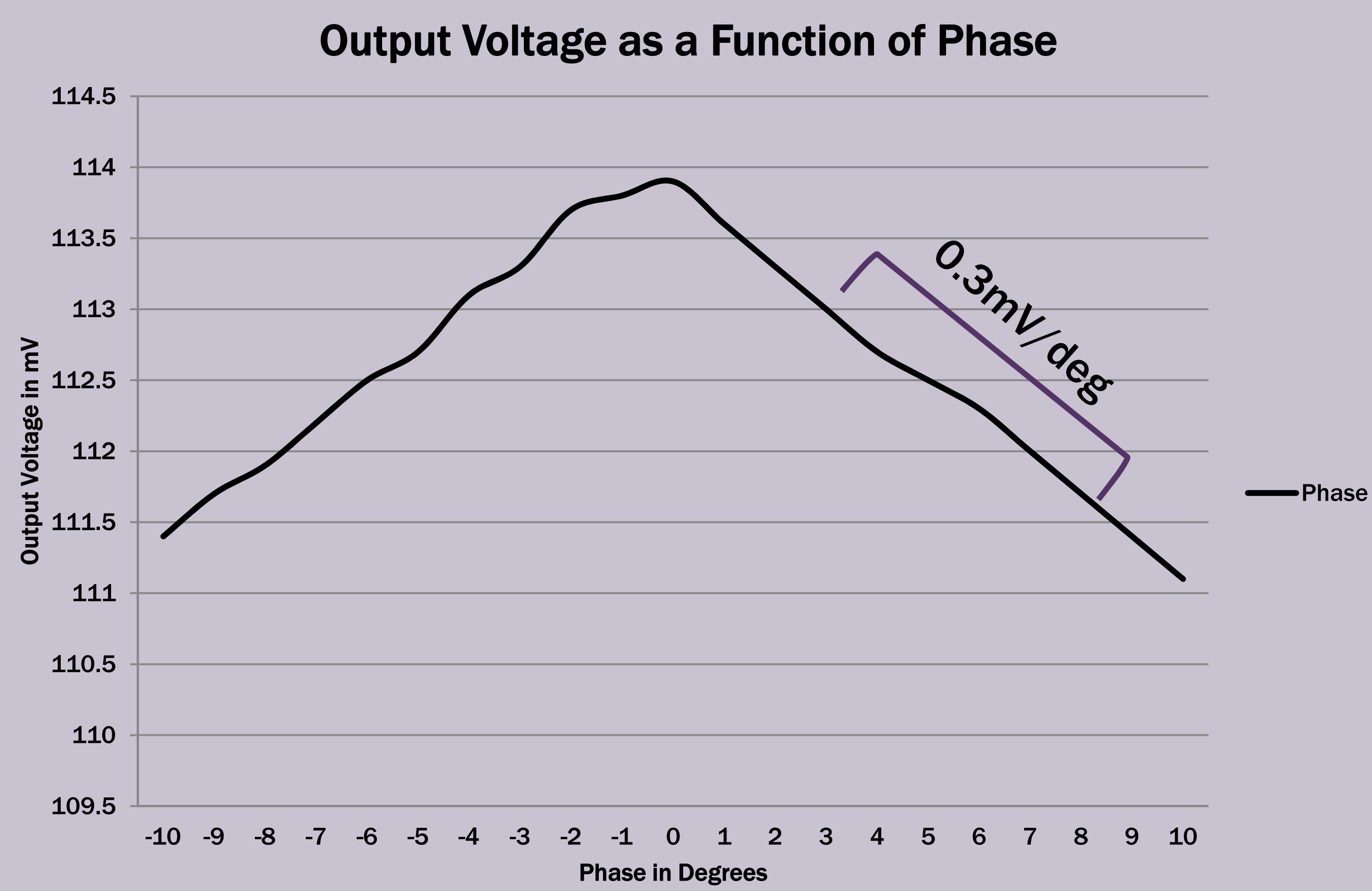


IF OUTPUT AS A FUNCTION OF PHASE

100 MHz RF/LO



ZOOMED IN



Output Voltage as a Function of Phase
114.5
114
113.5
113
112.5
112
111.5
111
110.5
110
109.5
Output Voltage in mV
-10 -9 -8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10
Phase in Degrees
Phase
0.3mV/deg

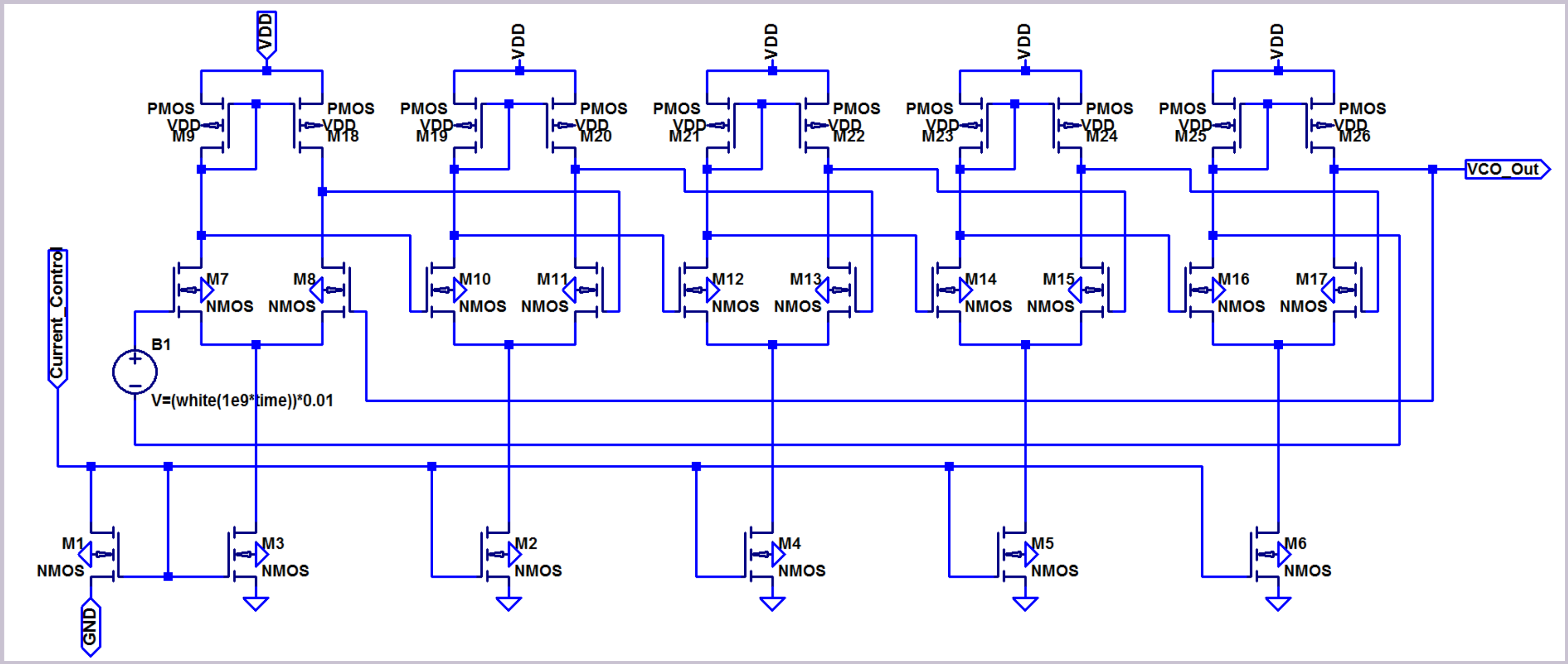
VCO DESIGN

- Many options to choose from
  - Ring oscillators
  - Relaxation oscillators
  - Varactor-tuned LC oscillators

- Requirements are
  - Relatively linear
  - Has the tuning range needed for the intended application

DIFFERENTIAL RING OSCILLATOR

Same idea as a ring oscillator made from inverters but with differential amplifiers.

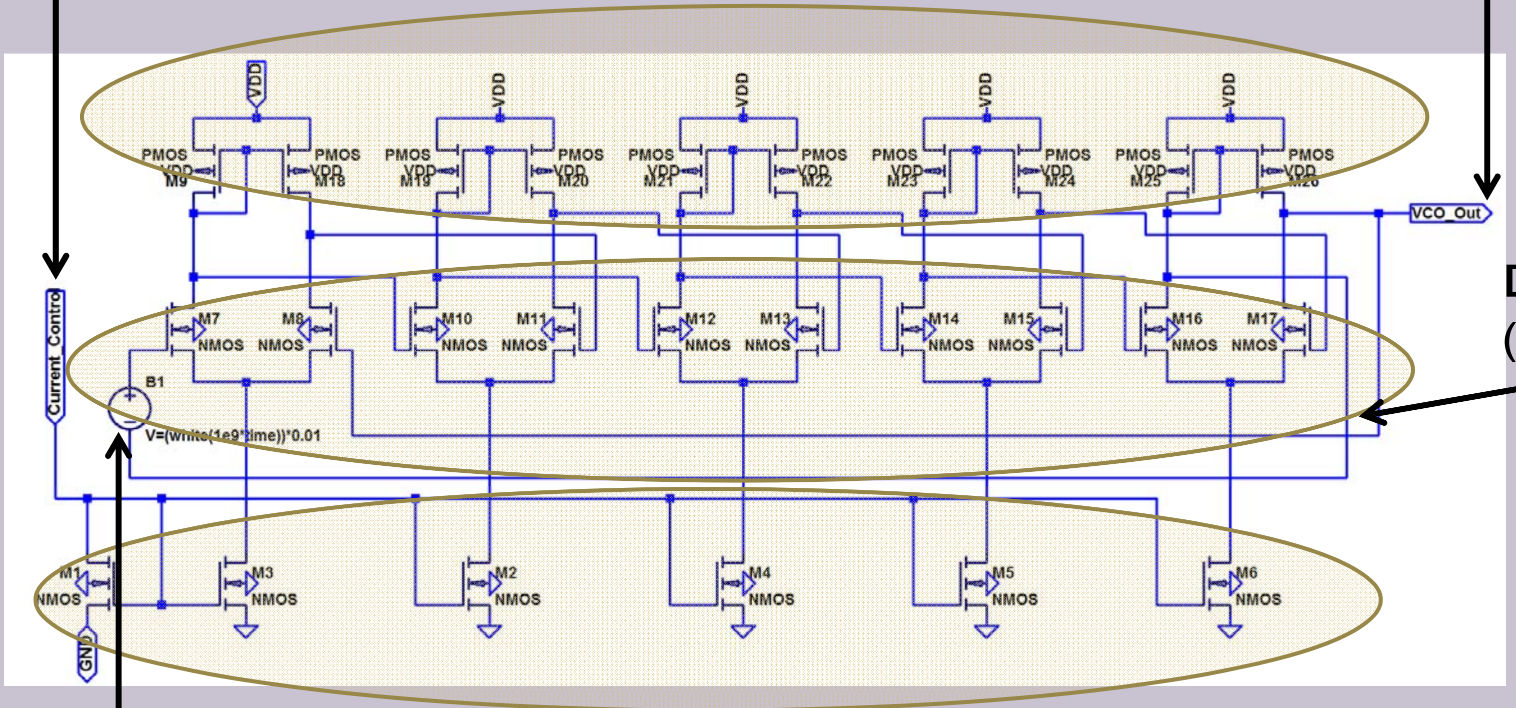


BREAKING IT DOWN

Current mirror loads (3.6u/0.6u)

Current sets delay

Output



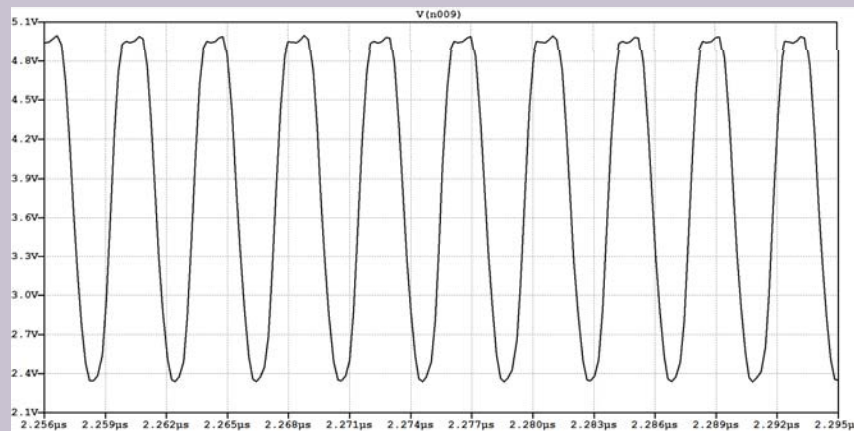
Diff pairs (1.8u/0.6u)

White noise source for simulation

Current mirrors (3.6u/0.6u)

OUTPUT

Problem: Odd output waveform shape



Problem: Output does not swing to full logic levels

Solution

Level Shifting

Need to shift the center of the output to ½ VDD so inverters switch in the middle of the waveform.

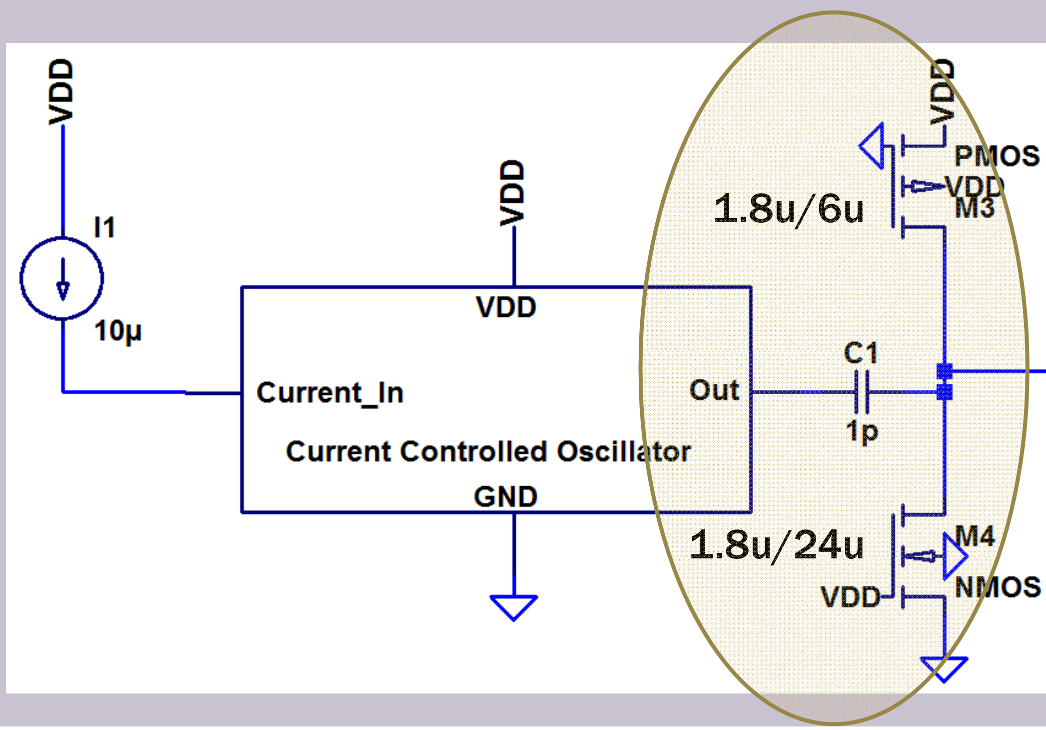
Pulse Shaping

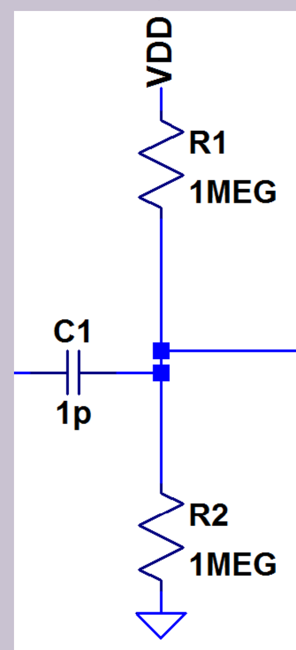
Inverter string is needed to provide full logic levels and sharpen the pulses.

LEVEL-SHIFTING

Level shifter with long L MOSFETs

Can also use resistors

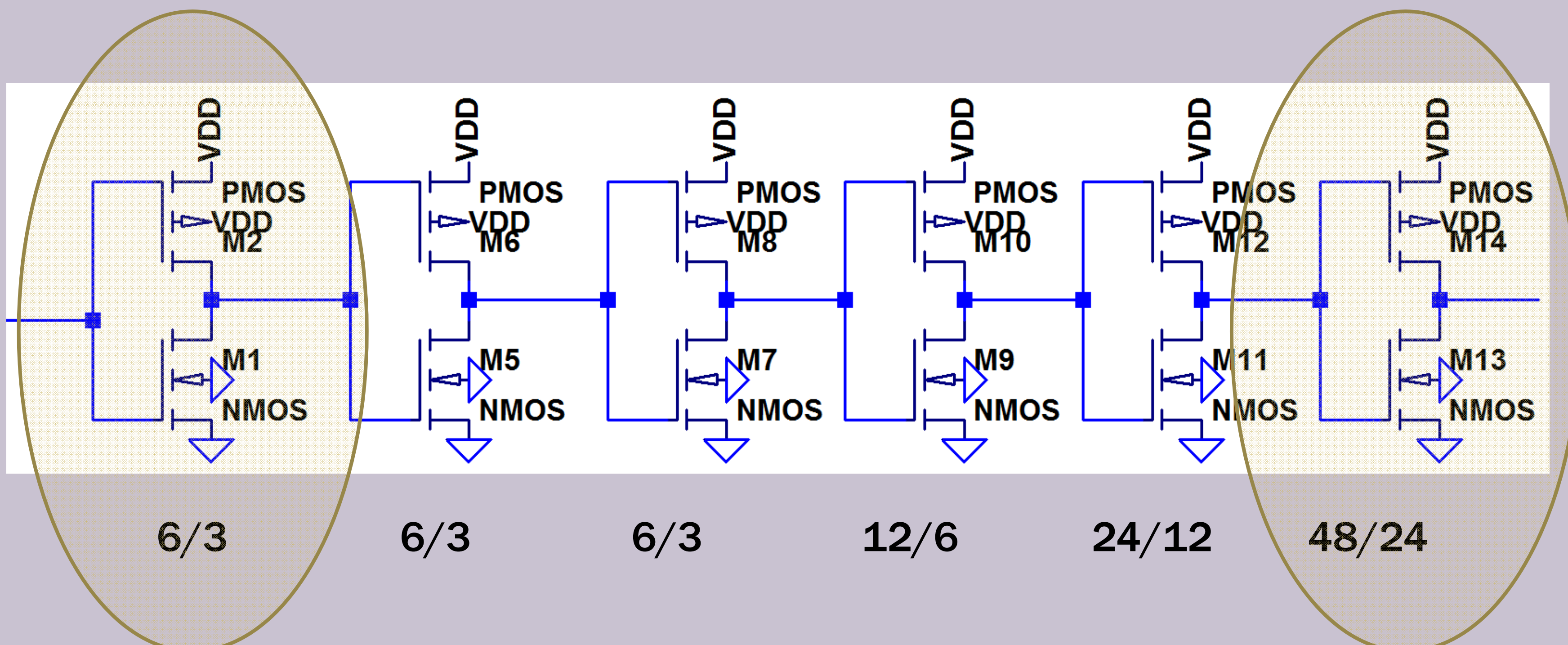




INVERTER STRING

Small inverter for
low capacitive loading

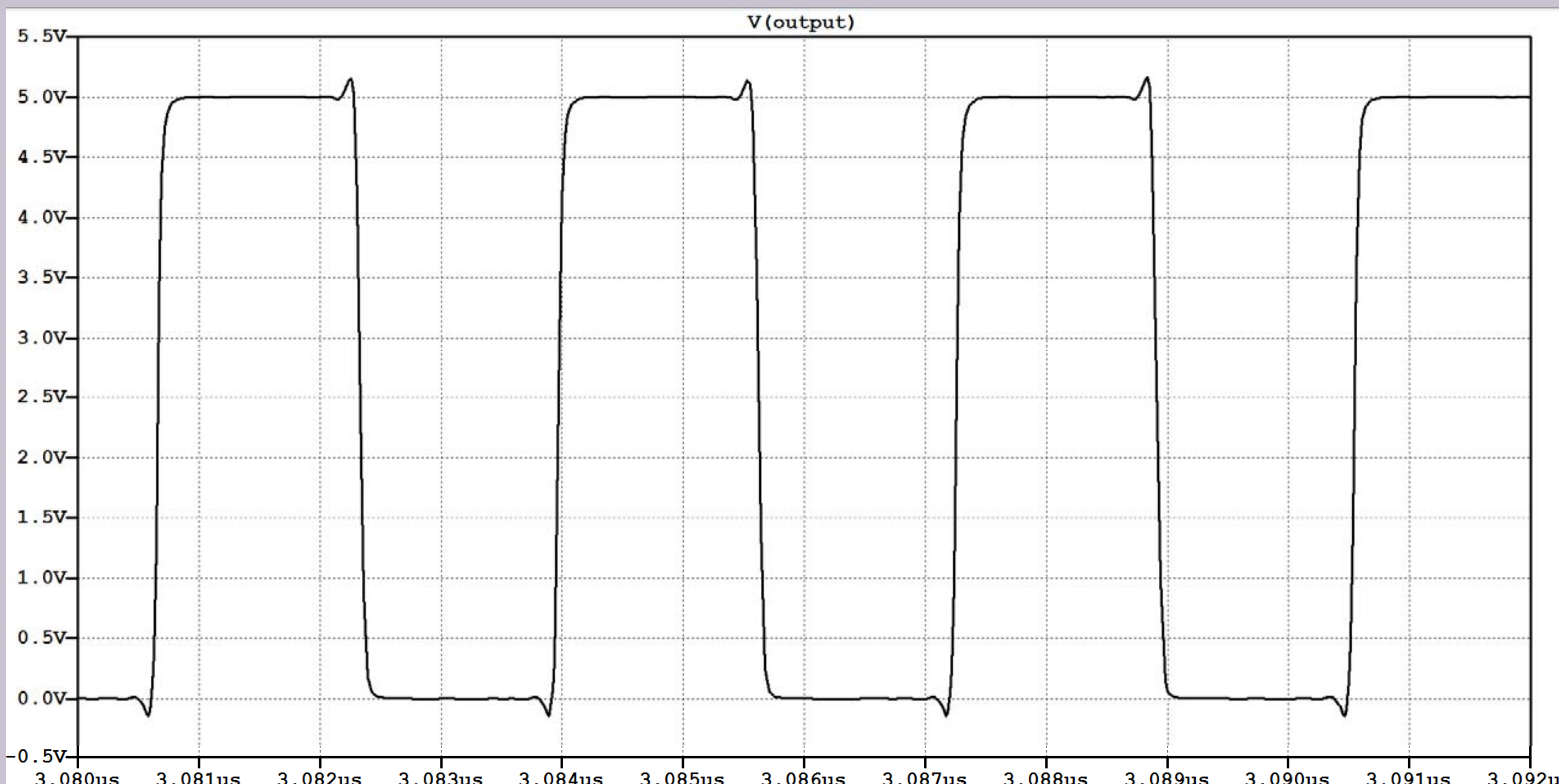
Big inverter for
load driving ability



Inverter sizes are
PMOS Width/NMOS Width

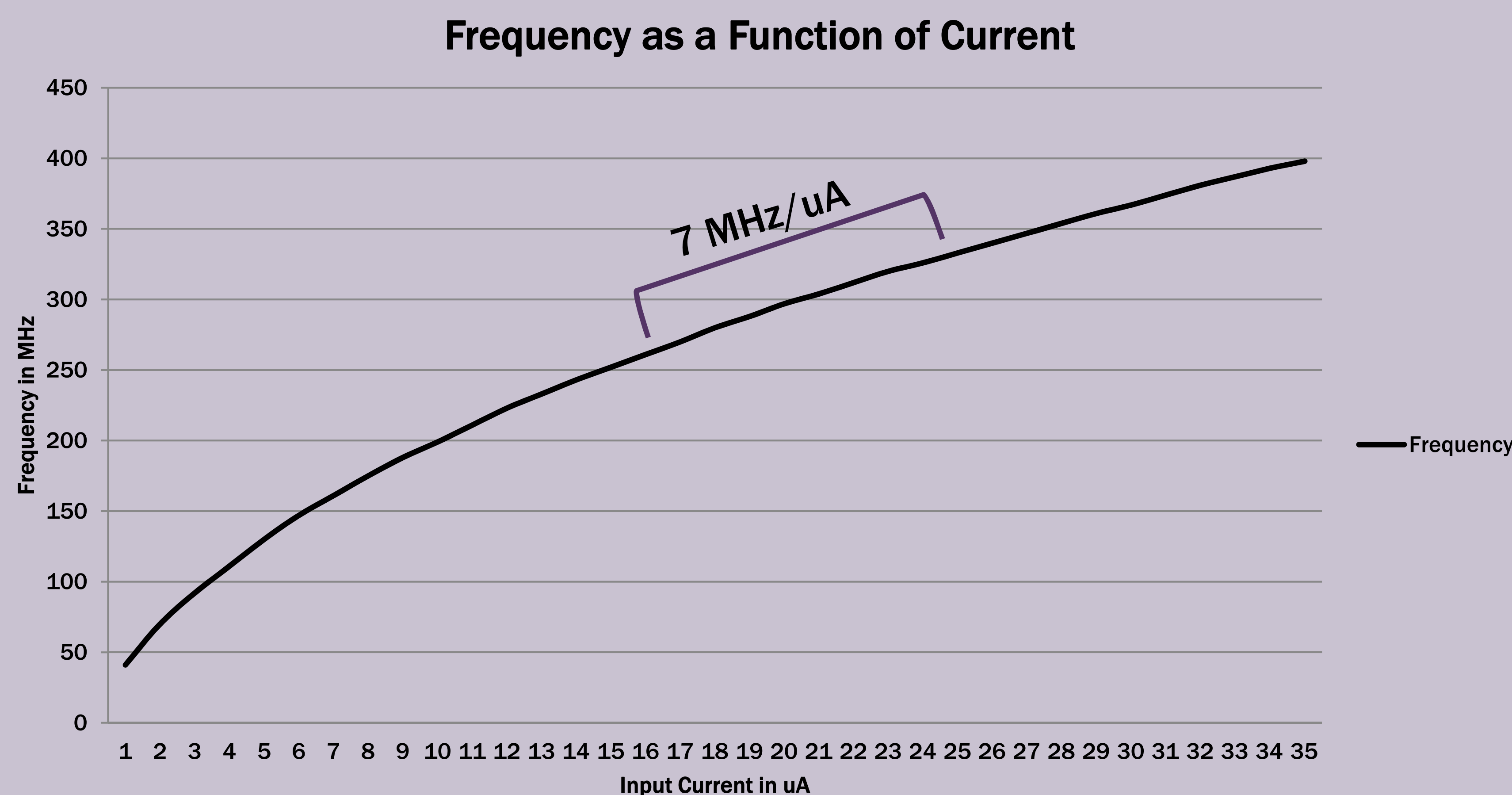
RESULT

300 MHz

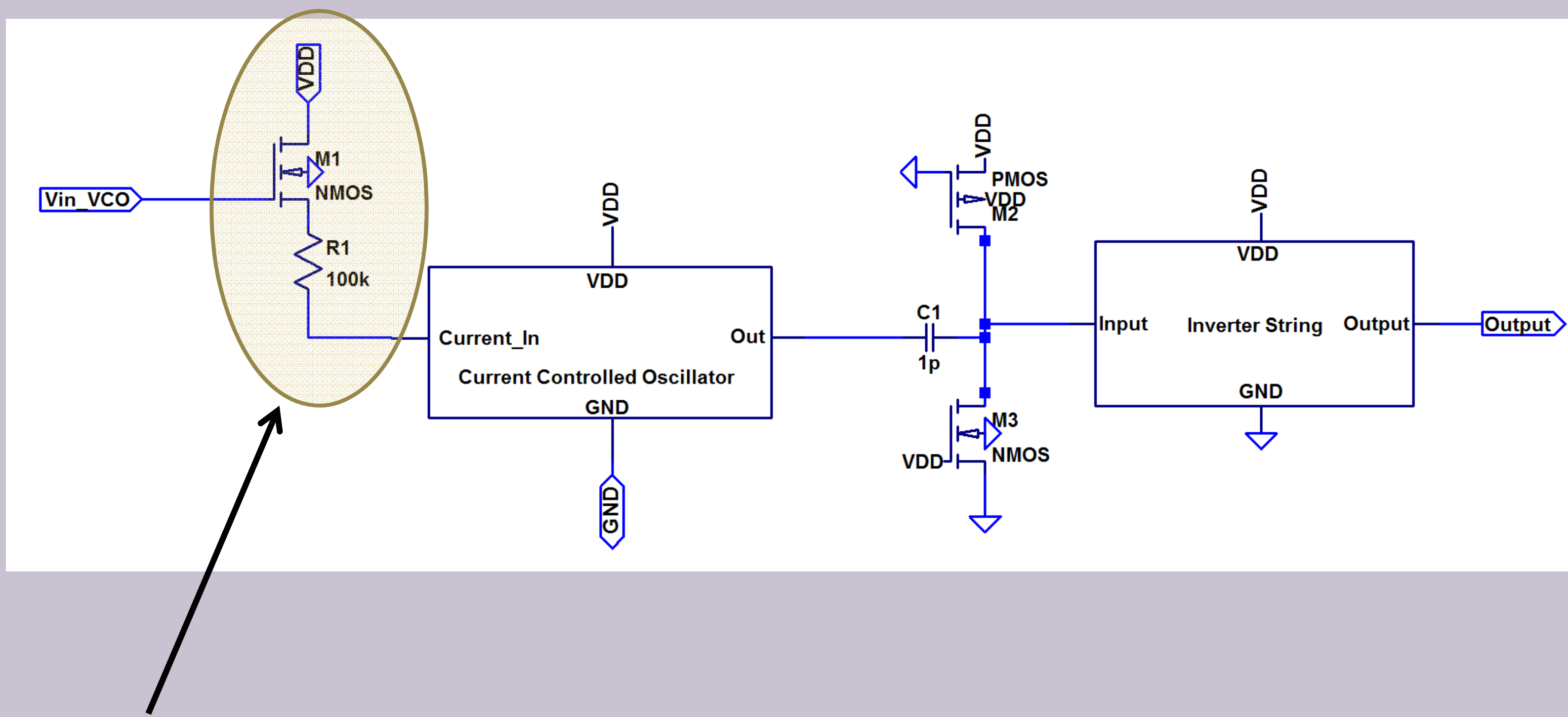


Sharp transitions with 50% duty cycle

FREQUENCY TESTING

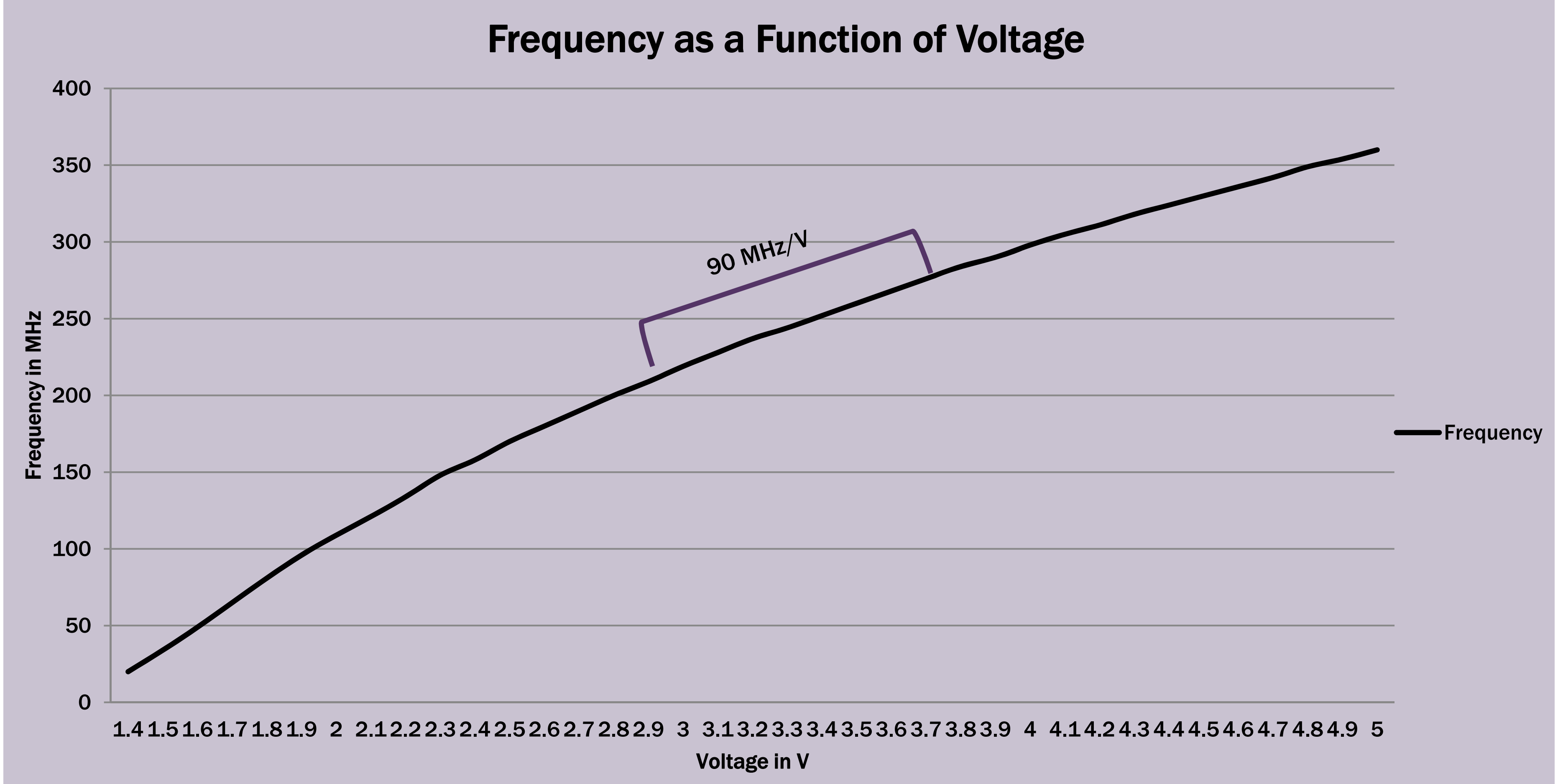


VOLTAGE TO CURRENT CONVERTER



This MOSFET and resistor serves
as a rudimentary voltage to current converter.

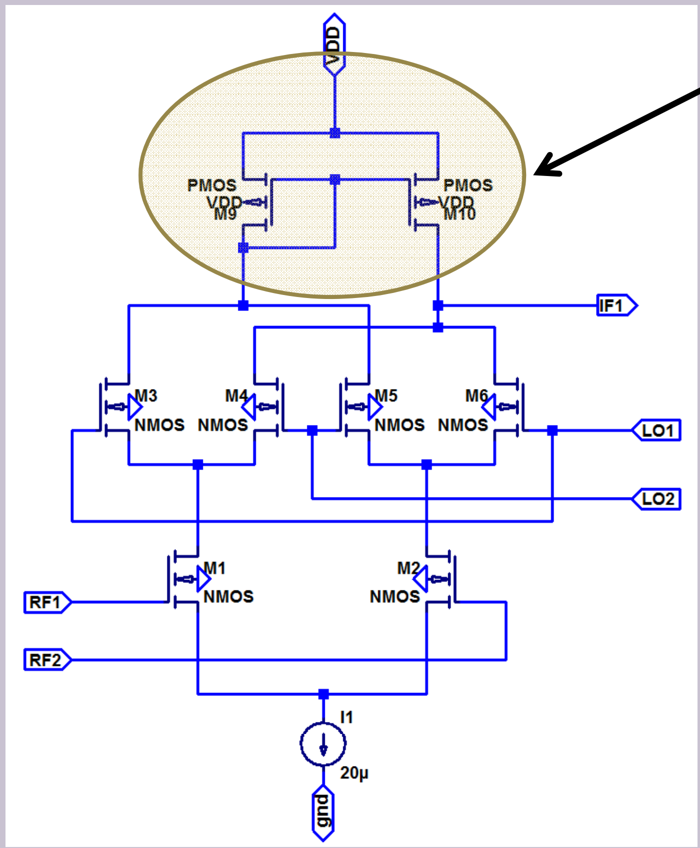
FREQUENCY TESTING



INTERFACING MIXER TO VCO

Active load for differential to single ended conversion.

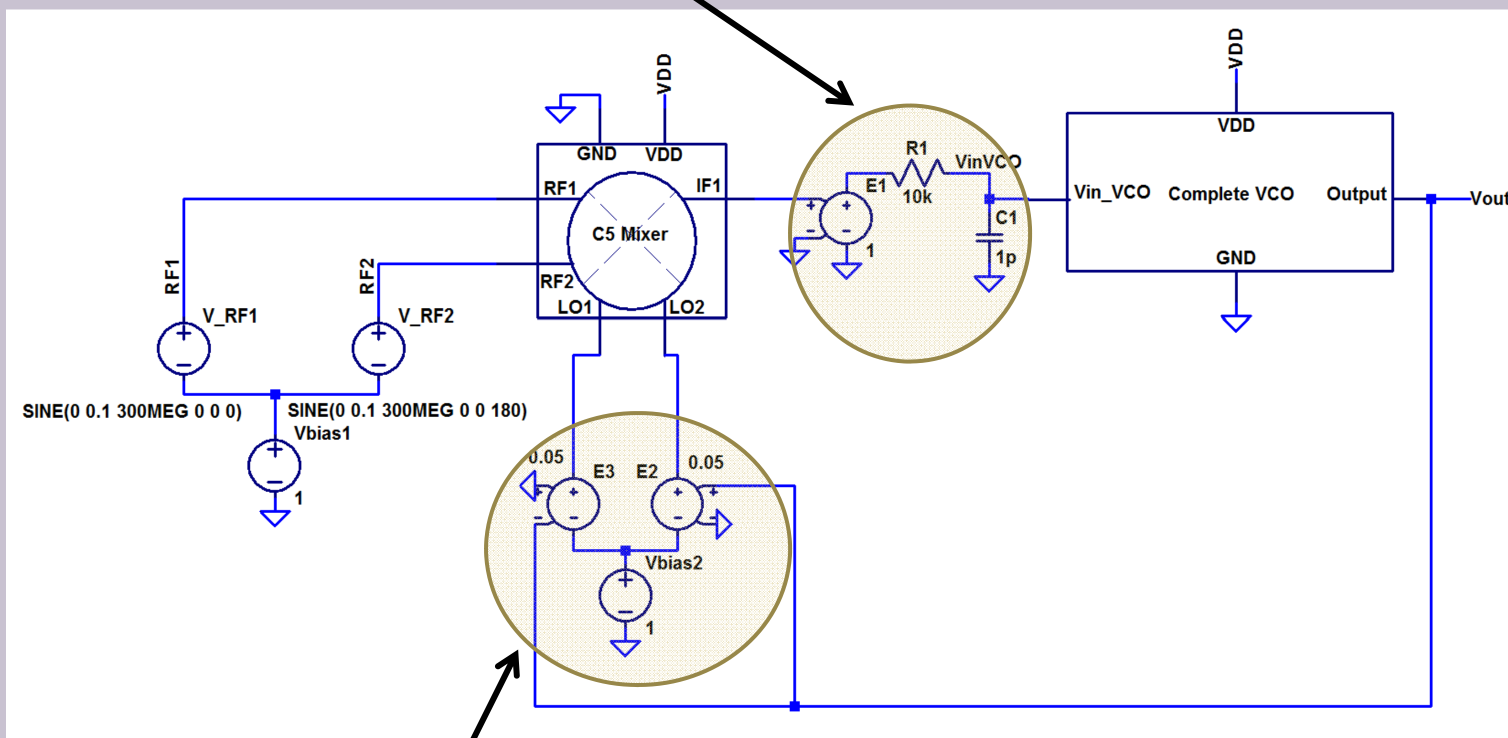
Mixer output is differential while VCO input is single-ended.



Single ended mixer

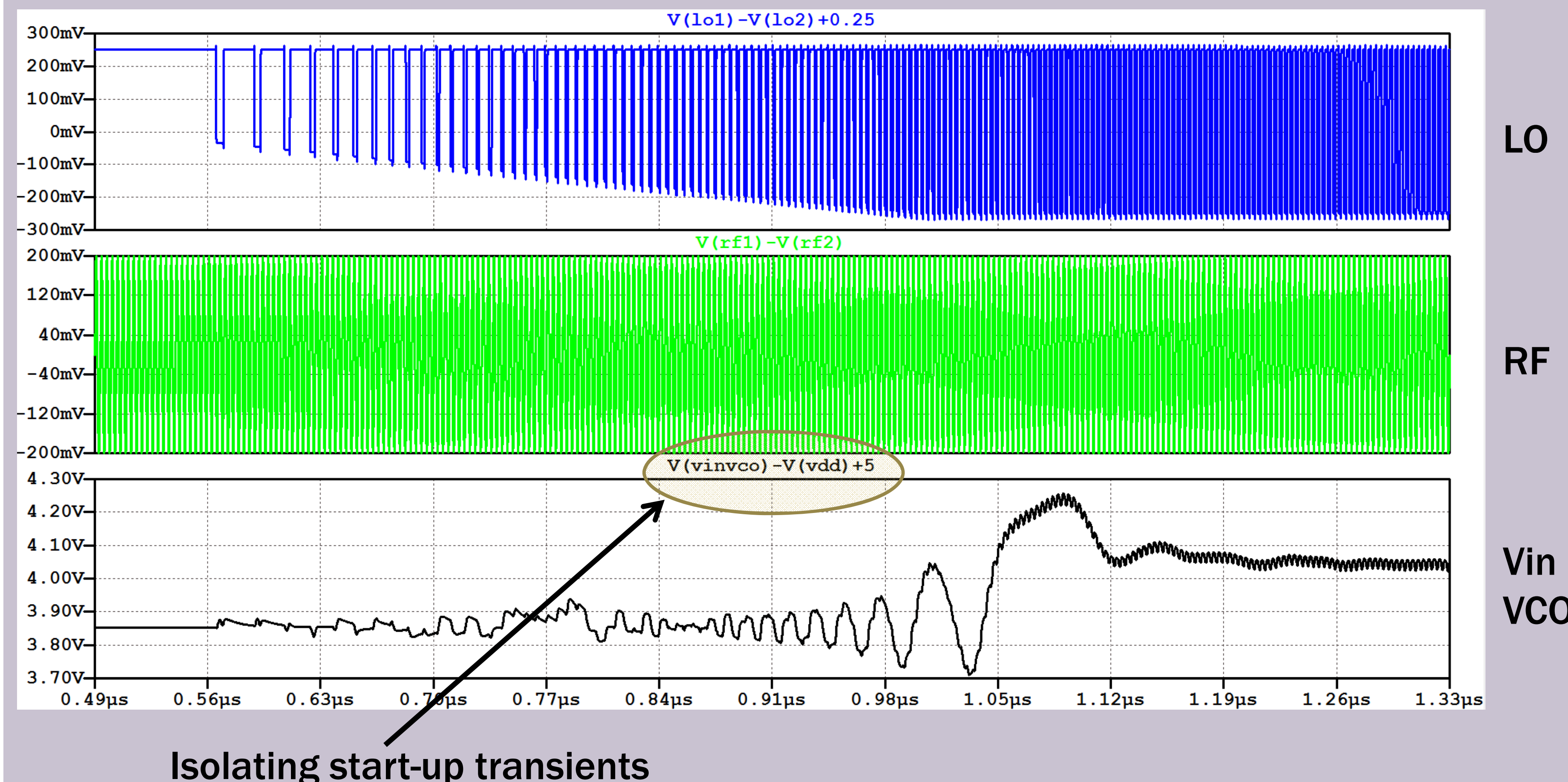
CLOSING THE LOOP

Loop filter with buffer to isolate effects from mixer output impedance.



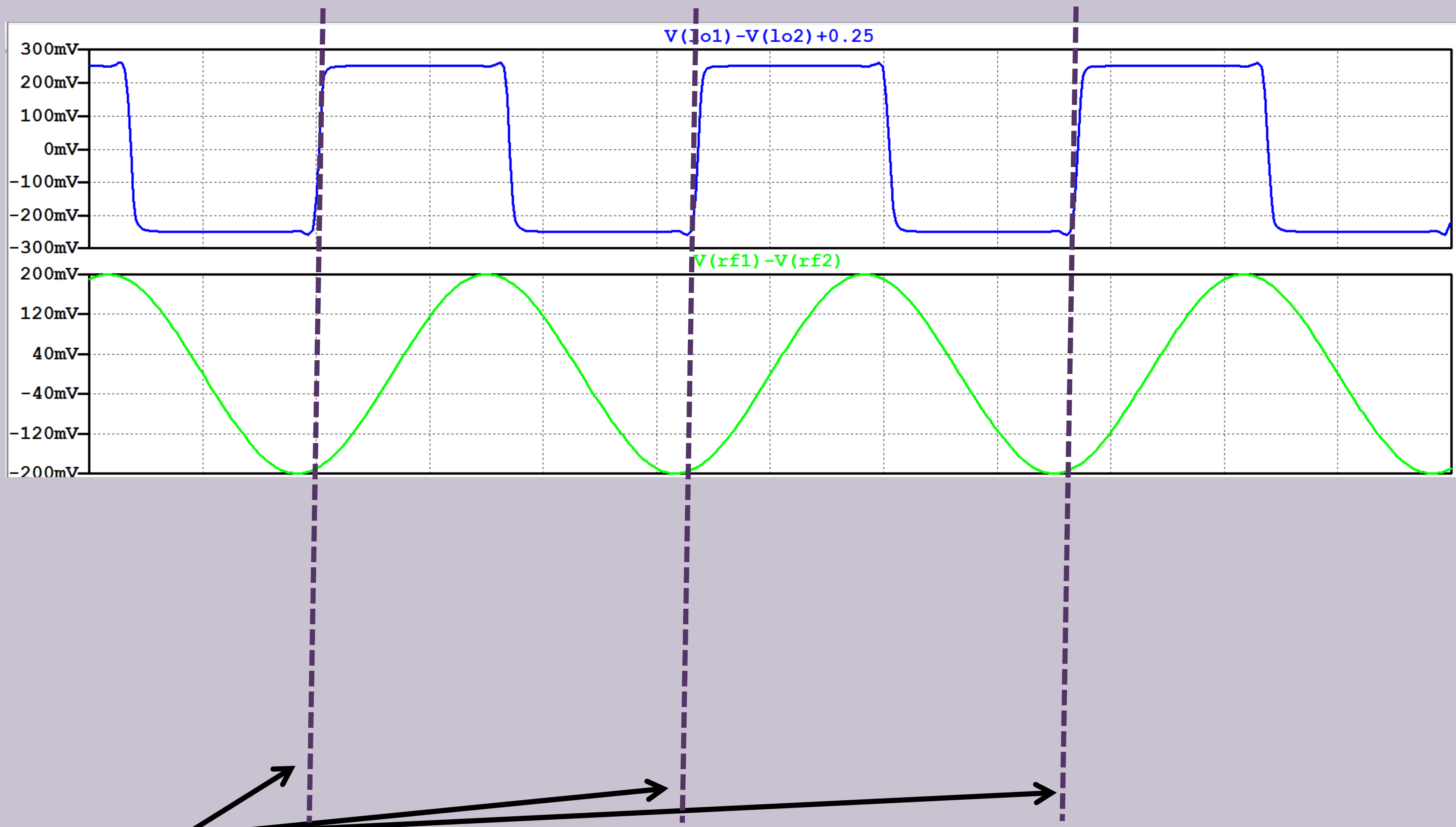
Mixer needs proper biasing and input levels.

OUTPUT



V(lo1)-V(lo2)+0.25
300mV
200mV
100mV
0mV
-100mV
-200mV
-300mV
V(rf1)-V(rf2)
200mV
120mV
40mV
-40mV
-120mV
-200mV
V(vinvco)-V(vdd)+5
4.30V
4.20V
4.10V
4.00V
3.90V
3.80V
3.70V
0.49µs
0.56µs
0.63µs
0.70µs
0.77µs
0.84µs
0.91µs
0.98µs
1.05µs
1.12µs
1.19µs
1.26µs
1.33µs
LO
RF
Vin VCO
Isolating start-up transients

LOCKED OUTPUT AT 300 MHZ



Edges line up

USEFUL EQUATIONS

$$K_F = \frac{1}{1 + sRC}$$

Loop filter transfer function (simple 1st order lowpass)

$$H(s) = \frac{\varphi LO}{\varphi RF} = \frac{K_{PD}K_{VCO} \cdot \frac{1}{1 + sRC}}{s + \frac{1}{N}K_{PD}K_{VCO} \cdot \frac{1}{1 + sRC}}$$

System transfer function (2nd order)

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N \cdot RC}}$$

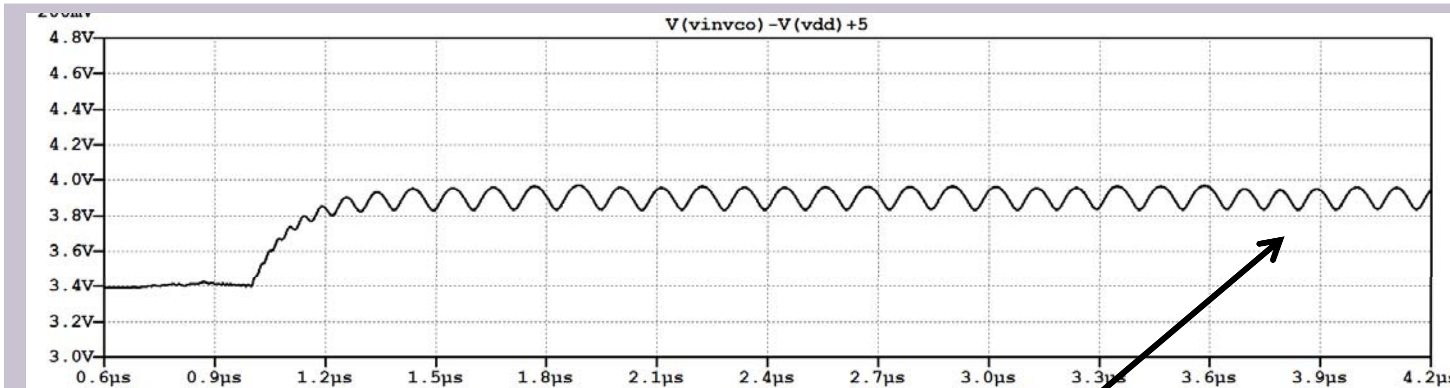
Natural frequency

$$\zeta = \frac{1}{2RC\omega_n}$$

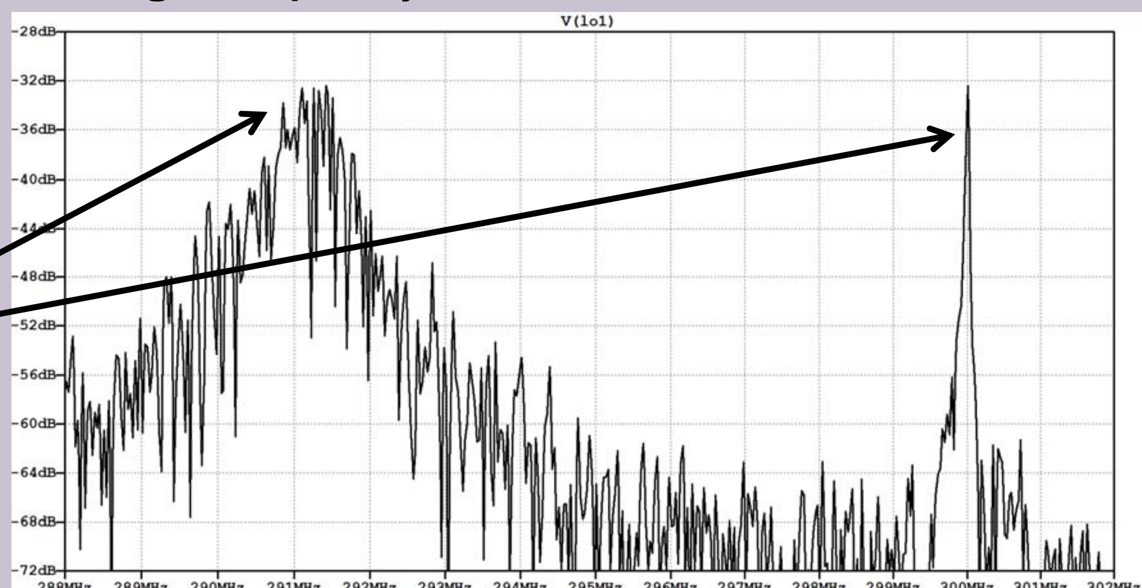
Damping ratio

N is for the divider ratio in frequency synthesis examples. If there is no divider use N=1.

OVERDAMPED CASE



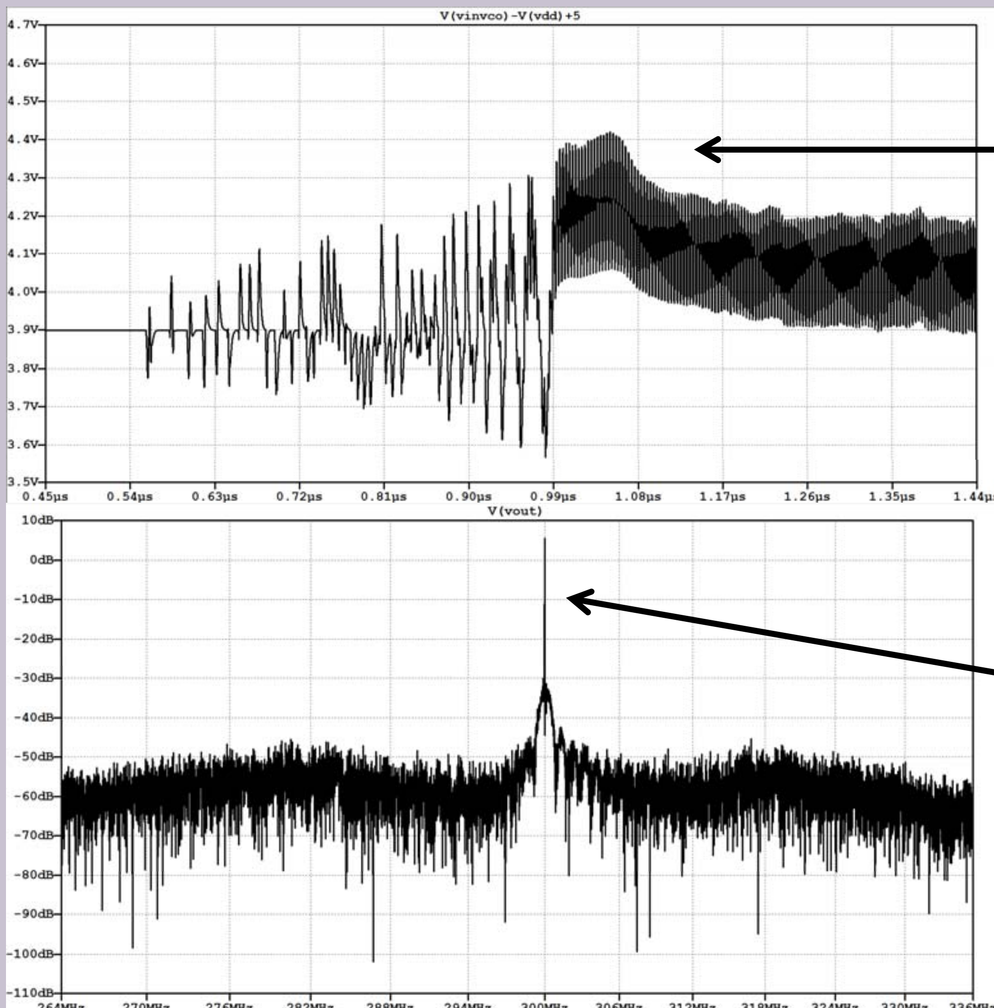
Overdamped PLL not locking on a single frequency



FFT of output shows two peaks
at 300 MHz and a noisy one at 291 MHz.

The difference is the natural frequency.

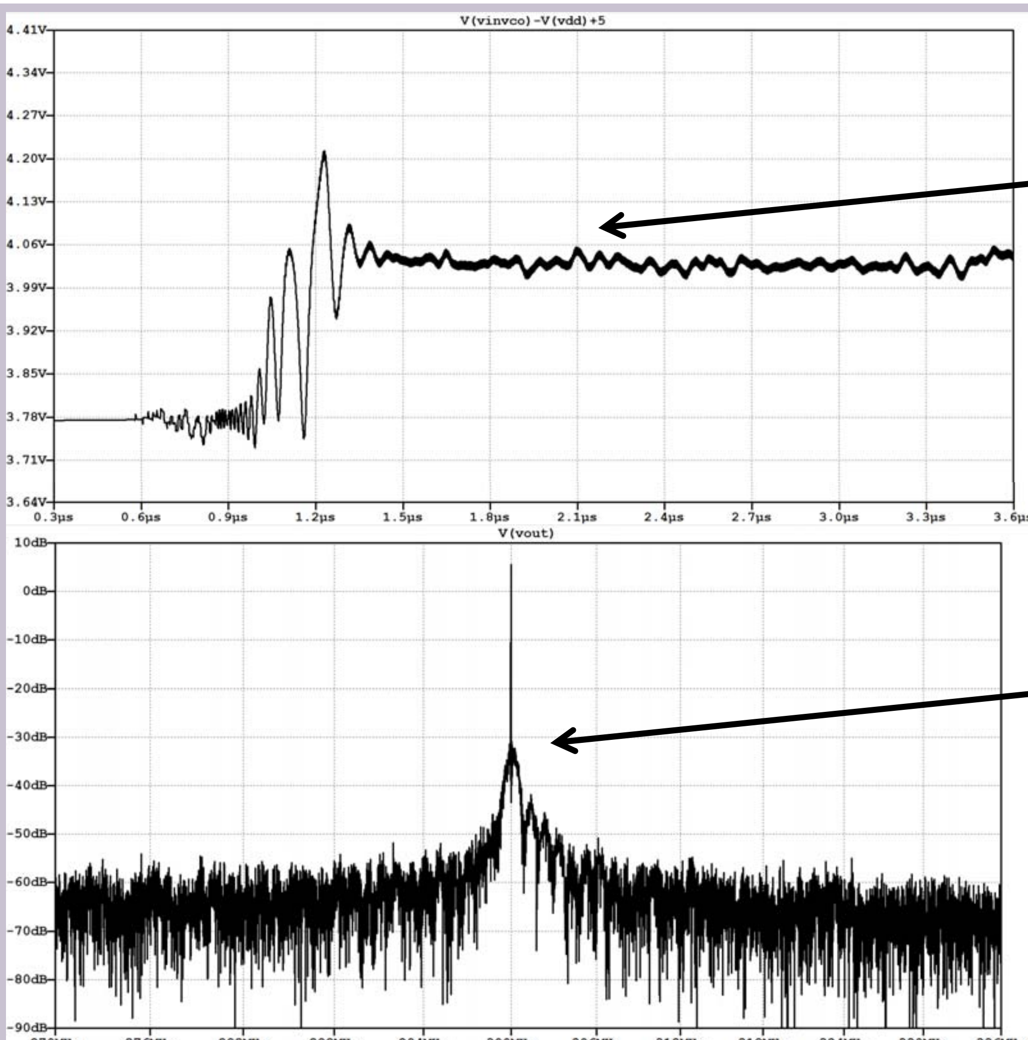
UNDERDAMPED CASE



VinVCO voltage shows some oscillation and ripple voltage.

FFT of output shows the correct peak at 300 MHz but there is significant phase noise.

CRITICALLY DAMPED CASE



VinVCO voltage settles and looks fairly random.

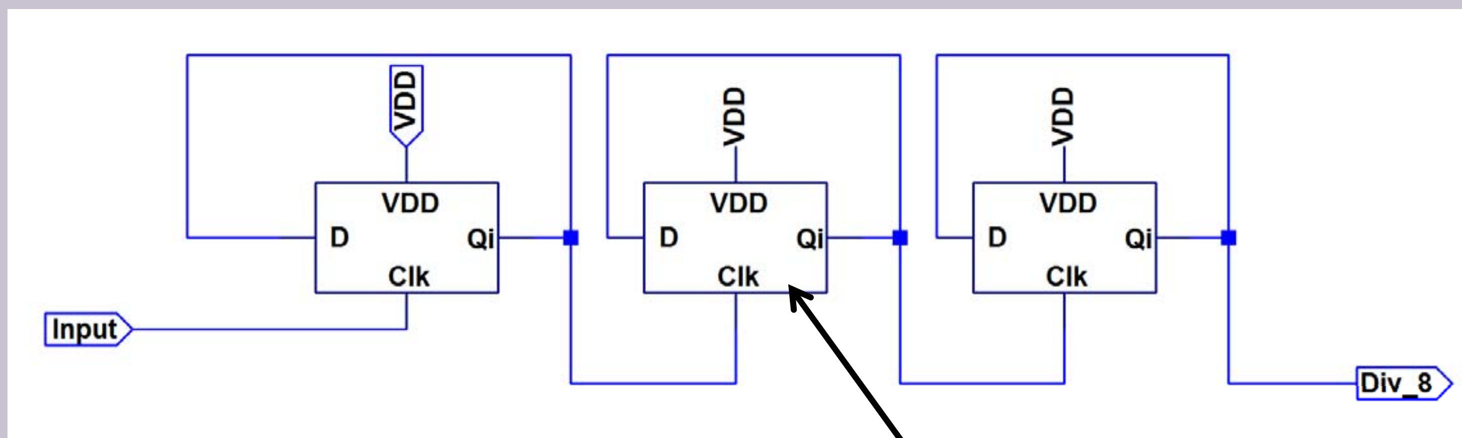
FFT of output shows the correct peak at 300 MHz with less noise.

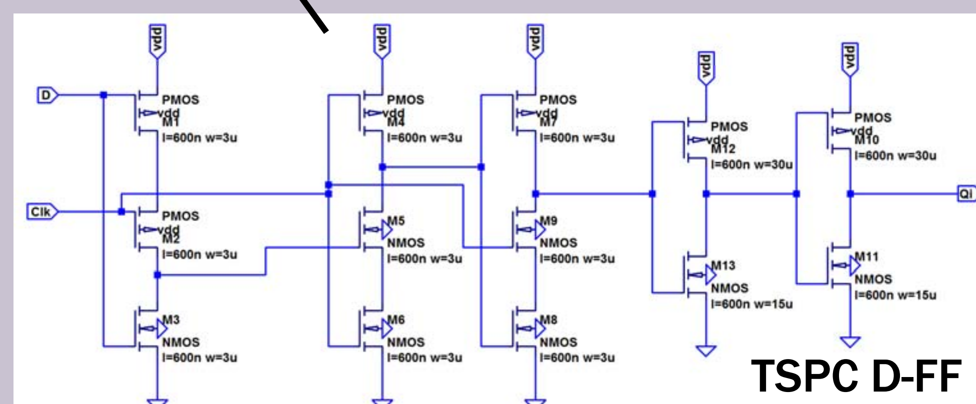
APPLICATION: FREQUENCY SYNTHESIS

- Stable oscillator topologies don’t scale well to high frequencies.
  - Quartz (32 KHz-160 MHz)
  - Rubidium (typically 10 MHz)
  - Silicon MEMS (1 MHz-140 MHz)
- A PLL locked to a stable reference can generate a stable high frequency oscillator.
  - Quartz (10 PPM)
  - Silicon MEMS (100 PPM)
  - Rubidium (0.0001 PPM or 0.1 PPB)

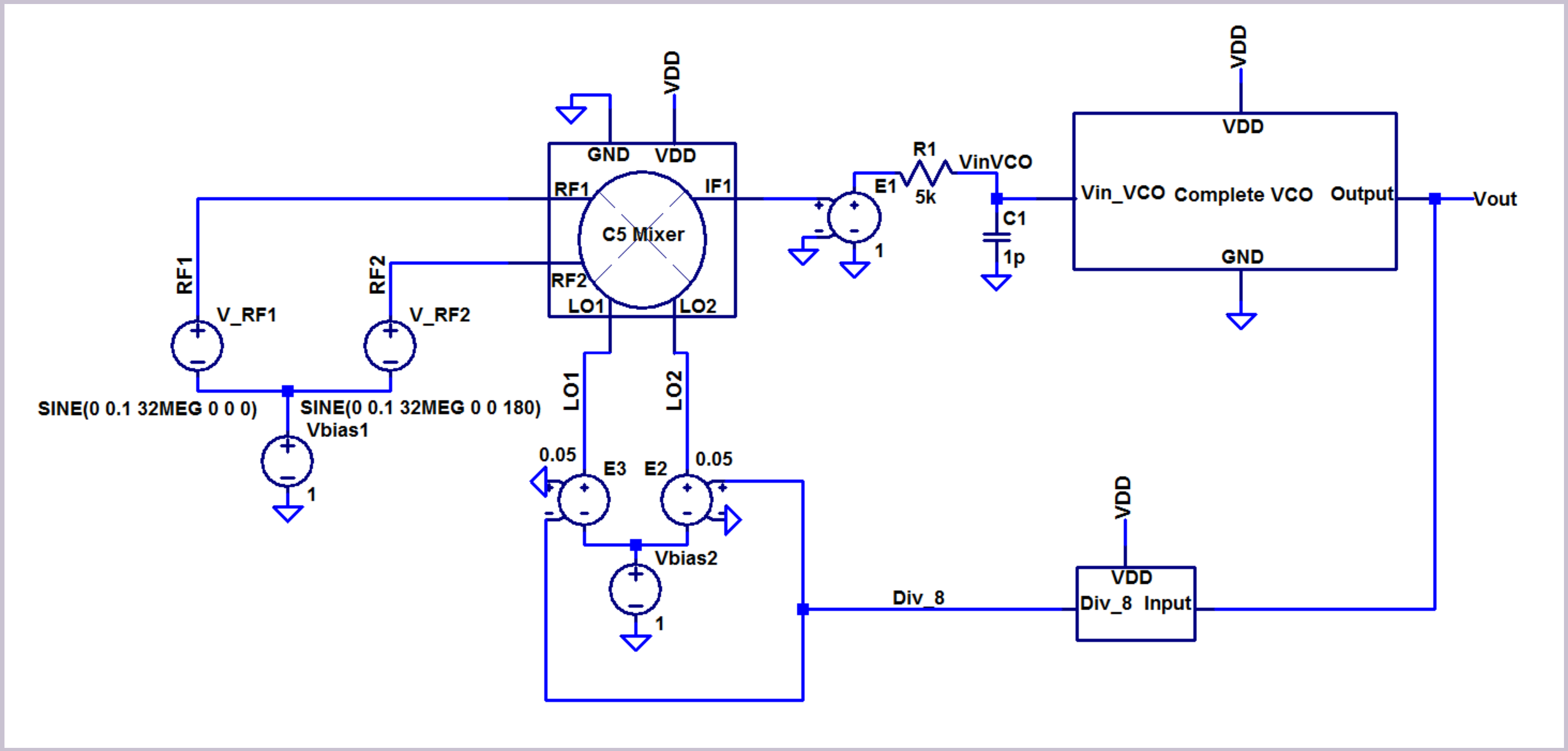
FREQUENCY DIVIDER

Each stage divides by 2



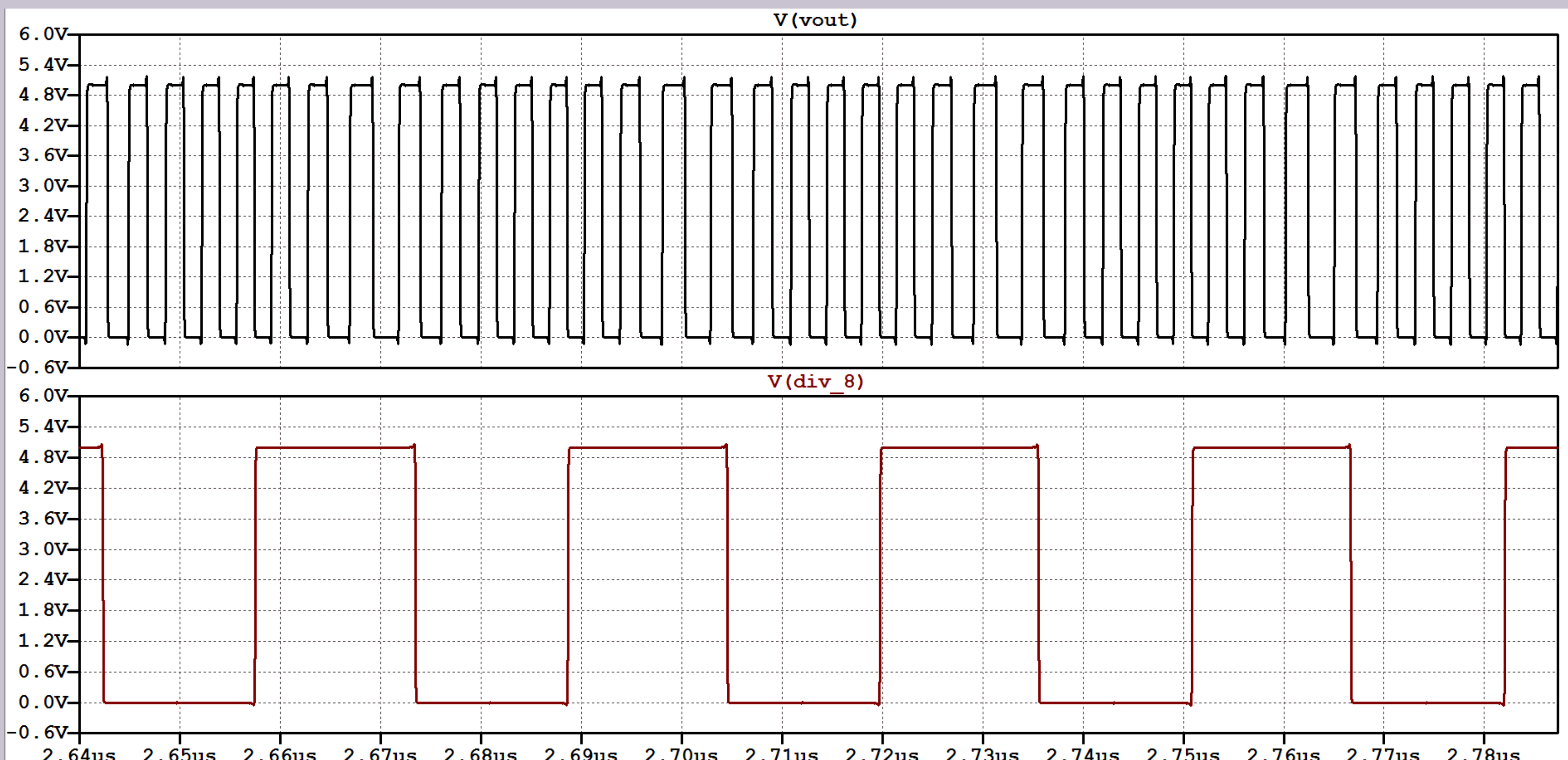


FREQUENCY MULTIPLIER SCHEMATIC



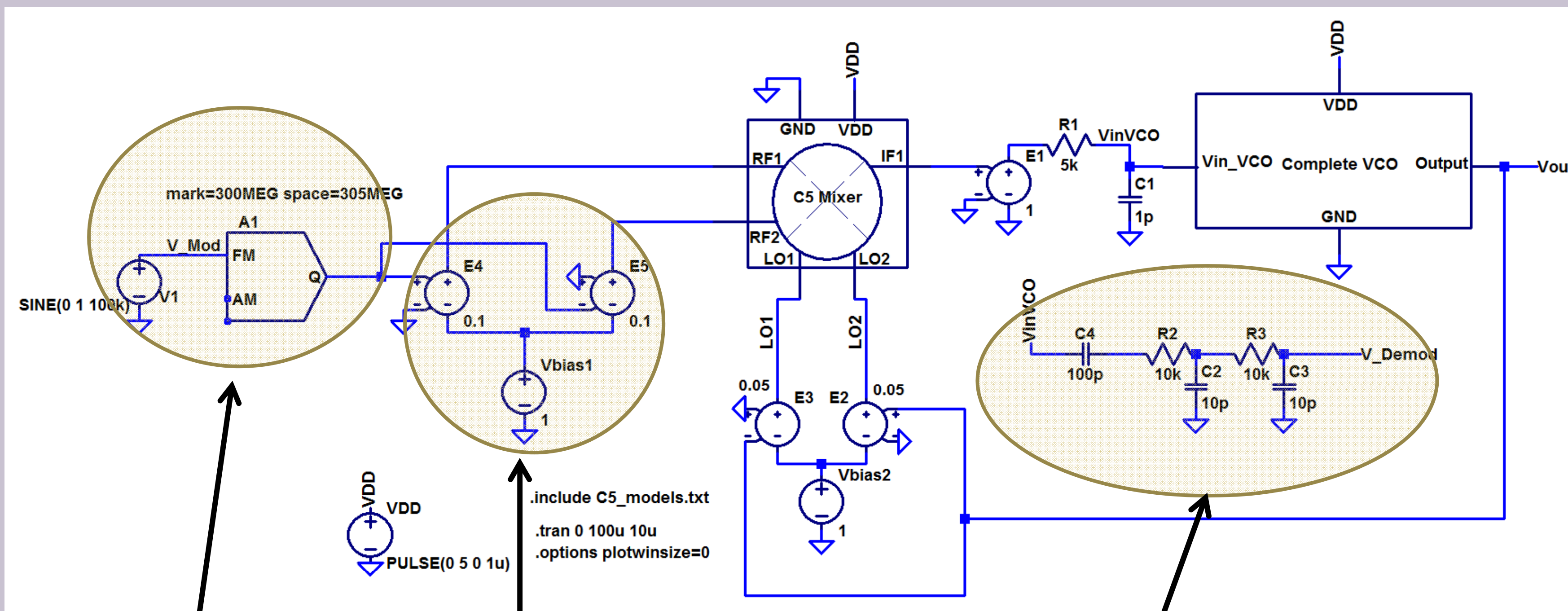
OUTPUT

256 MHz Output



32 MHz Input

APPLICATIONS: FM DEMODULATION

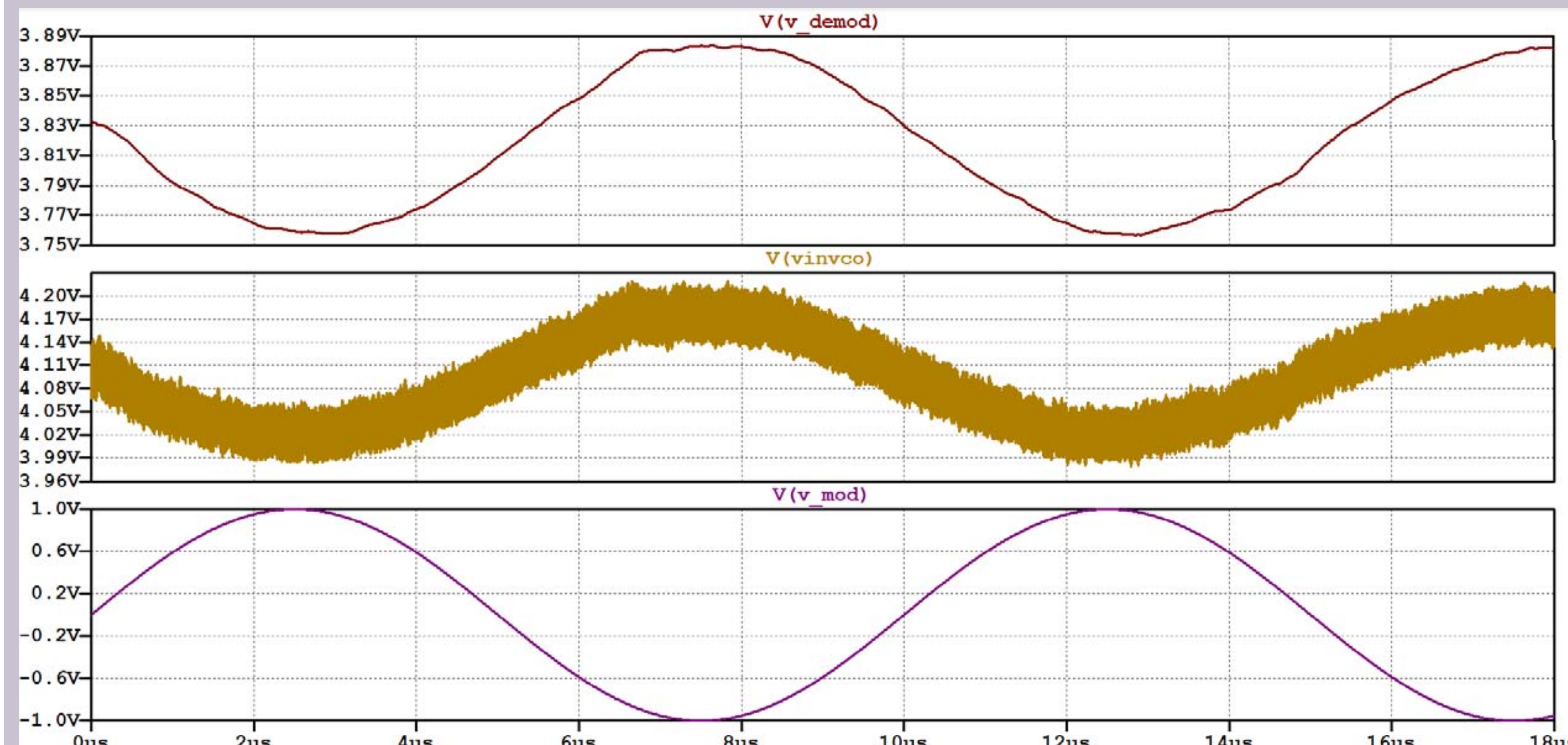


FM Modulator

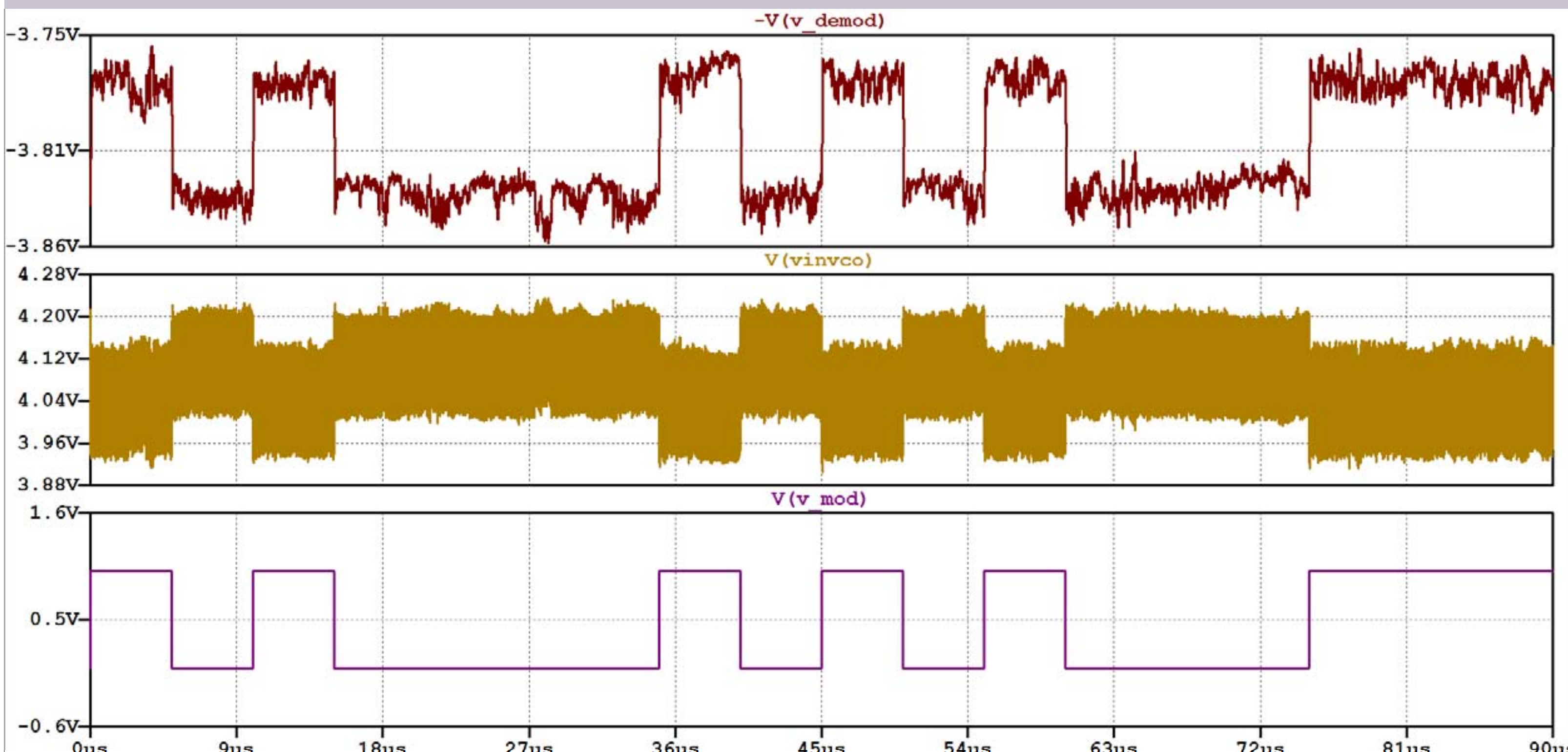
Provides differential input at correct amplitude

Additional filtering to filter out VCO ripple

INPUTS AND OUTPUTS



APPLICATIONS: FSK DEMODULATION



Filtered VCO input

VCO input

Original Input to FSK Modulator

REFERENCES

- The Art of Electronics by Horowitz and Hill
- MT-080 Mixers and Modulators by Analog Devices
- MT-086 Fundamentals of PLLs by Analog Devices
- Practical Tips for PLL Design by Dennis Fischette
- FM & PM Demodulation from The Scot's Guide to Electronics
- Mixer Basics Primer by Christopher Marki