

A PHASE SHIFTED PWM METHOD FOR INDIRECT MATRIX CONVERTER

, S.Sakthi¹, K.Bharathi², Dr.M.Sasikumar³,

EEE Department, Jeppiaar Engineering College, Anna University, Chennai Tamilnadu India

ABSTRACT

This paper proposes an indirect matrix converter (IMC) Topology with dual three-phase outputs and its effective carrier-based phase shifted pulse width modulation (PWM) method. The proposed IMC topology can independently supply ac power for two three-phase loads from a single three-phase ac power source. This converter consists of a rectifier stage used in traditional three-phase IMC and a five-leg inverter. Besides a proposed IMC topology, the carrier based PWM method suitable for this converter is introduced. The proposed PWM method is easily implemented by using only one symmetrical triangular carrier signal to generate the PWM signals for a rectifier and five-leg inverter. Proposed IMC topology features the advantages of conventional three-phase IMC, such as sinusoidal input/output current waveforms, controllable input power factor, and simple commutation at the rectifier stage. Analysis, simulation, and experimental results are provided to demonstrate the advantages of the proposed IMC topology with dual three-phase outputs and to validate the effectiveness of the applied modulation strategy.

Keywords: Carrier-based pulse width modulation (PWM), direct matrix converter (DMC), dual inverters, fiveleg inverter, indirect matrix converter (IMC), space vector PWM (SVPWM), FPGA

I.INTRODUCTION

Indirect matrix converter with dual three-phase outputs and its effective Carrier-based pulse width modulation (PWM) method. The proposed IMC topology can independently supply ac power for two three-phase loads from a single three-phase ac power source. [6]This converter consists of a rectifier stage used in traditional three-phase IMC and a five-leg inverter. Besides a proposed IMC topology, the carrier-based phase shift PWM method suitable for this converter is also introduced. [2]The proposed PWM method is easily implemented by using only one symmetrical triangular carrier signal to generate the PWM signals for a rectifier and five-leg inverter. Proposed IMC topology features the advantages of conventional three-phase IMC, such as sinusoidal input/output current waveforms, controllable input power factor, and simple commutation at the rectifier stage. Analysis, simulation, and [3] experimental results are provided to demonstrate the advantages of the proposed IMC topology with dual three-phase outputs and to validate the effectiveness of the applied modulation strategy. THE three-phase-to-three-phase ac/ac matrix converters (MCs) are originally presented. MCs allow direct ac/ac power conversion without the dc energy storage component. They have a rectifier/dc-link capacitor/inverter structures. MCs have many advantages such as

sinusoidal input and output current waveforms, unity power factor at the input side, increased power density, and inherent four-quadrant operation. In addition, MCs are highly reliable and durable due to the output three-phase indirect matrix converter. By using a matrix converter, dual loads can be used instead of single load, and by increasing the matrix converter, output loads can be increased. [4] A FPGA processor is used instead of DSP processor. Carrier phase shift PWM topology is used.in the project we are trying to prove the existing system in a simpler cost efficient way.

II. DUAL THREE PHASE INDIRECT MATRIX CONVERTER

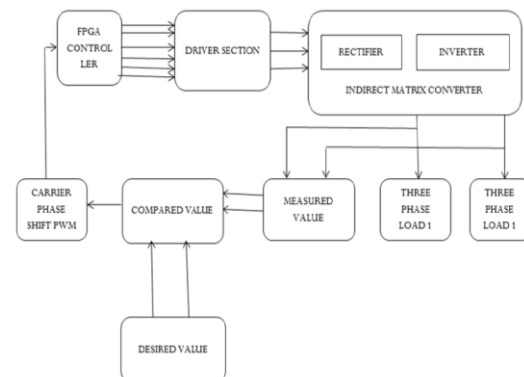


Fig 1 block diagram of the proposed system

The PWM signals are generated and they are turned on based on the software. The six PWM signals are generated in the FPGA section and then they are given to driver section from which gives three outputs which is in turn given to the matrix inverter converter section. This matrix inverter has two main parts in it, rectifier and inverter section.[3][4] The rectifier is used to convert ac-dc and then in inverter section dc-ac due to this process lower order harmonics is eliminated. In this section the three inputs is converted into six outputs, which is given to the loads. Then a feedback is taken from the output and this value is compare with the desired value and then the difference is taken and given to the controller circuit and hence the PWM signals are generated according to the required value.

a) Matrix Converter

Variable-speed motor drive that uses an AC Drive has enjoyed widespread use because of its great energy-saving effect. What is yet unsolved are the suppression of a power harmonic current and the effective use of regenerative energy during deceleration. In order to fully solve these technical issues, we employ the Matrix converter technology, which directly converts from AC power source to AC output shown in fig 2

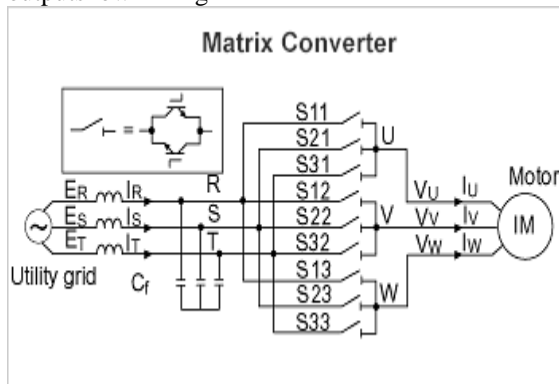


Fig 2 matrix converter

Fig 2 shows main circuit configurations of the matrix converter and the conventional voltage source PWM AC Drive. The main circuit of the matrix converter consists of small input filters, which consist of reactors and capacitors, and nine bi-directional switches. The bi-directional switches consist of the combination of IGBTs shown in Fig 2. On the other hand, the voltage source PWM AC Drive consists of a power AC Drive circuit with the combination of a rectifying circuit on the input side, a smoothing circuit with capacitors on the intermediate part, and IGBTs on the output side.

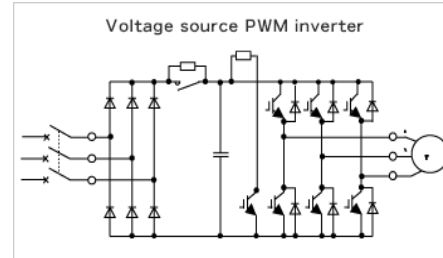


Fig 3 Main circuit configurations of matrix converter and voltage source PWM AC Drive
III. CONTROLLER UNIT SPARTAN FPGA FROM XILINX

FPGA contain programmable logic components called “logic blocks”, and a hierarchy of reconfigurable interconnects that allows the blocks to be “wired together” somewhat like many logic gates that can be inter wired in different configurations. Logic blocks can be configured to perform complex combinations logic blocks also include memory elements which may be flip-flops or more 29 [4] Complete blocks of memory functions, or merely simple logic gates like AND or XOR. Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA, designs employ very fast and bi-directional data busses it becomes a challenge to verify correct timing of valid data within set up time and hold time. Floor planning enables resources allocation within FPGA to meet this time constraints. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial reconfiguration of a portion of the design and the low non requiring engineering cost relative to an ASIC design, offer advantages for many applications.

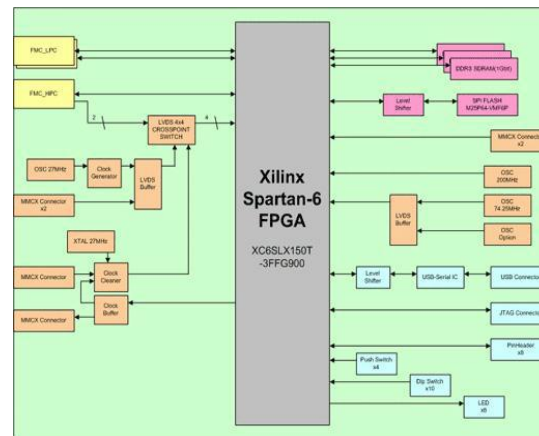


Fig 4 FPGA block diagram

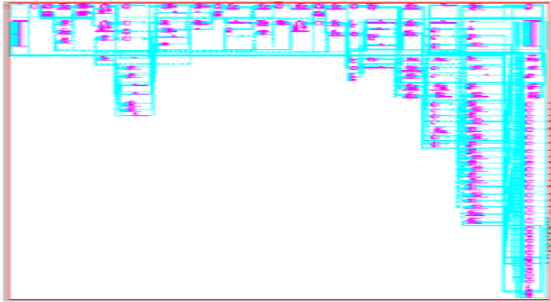


Fig 5 FPGA connection Board

The simulation of the proposed system is done in MATLAB; this explains the software working of the hardware. The PWM generation, then matrix converter and the overall hardware is done separately in simulated and the results are enclosed.

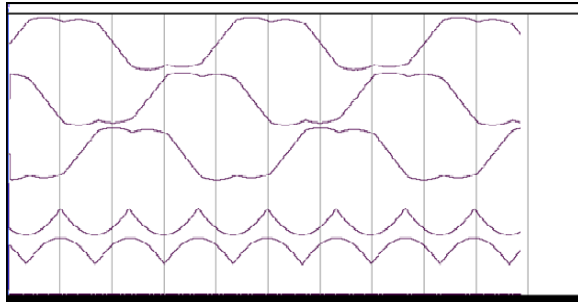


Fig 6 Space Vector Generation

The space vector signal is the reference signal for the production of carrier wave. They are generation in three different degree 0,120,240.

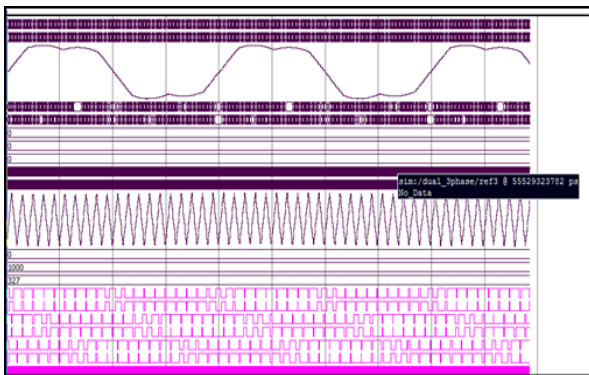


Fig 7 inverted Carrier Waveform

This figure explains the generated carrier wave, which is also a reference wave, which is used to generate the PWM, which is required to fire the MOSFETS

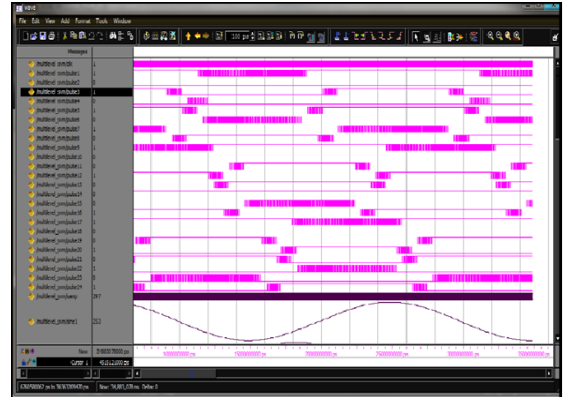


Fig 8 PWM generation

The PWM is generated by comparing the space Vector wave and the carrier wave. Then the signals are monoshooted in order to avoid firing of MOSFETS together.

IV SIMULATION CIRCUIT

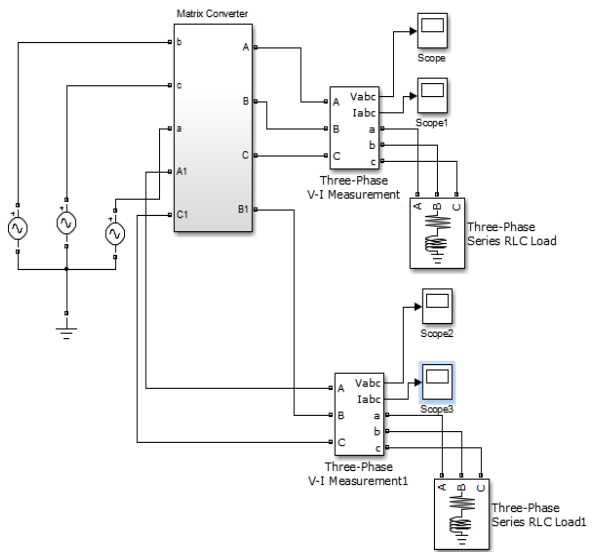


Fig 9 Simulation Circuit Diagram

Fig 9 explains the overall hardware and the pulses are generated and then they are given to the matrix converter in which the three input is converted into six output i.e. two three phase output. Hence, a single three-phase input is converted into two three-phase

output



Fig 10 simulation of matrix converter

Figure 10 Explains about the matrix converter structure. Here, the pulses are received from the pulse generator and the mosfets are fired. It is constructed in such a way that a single three phase input is converted to two three phase output.

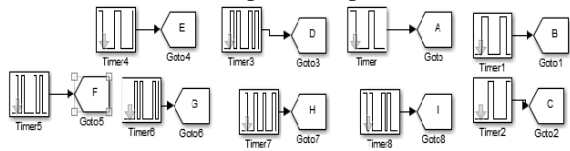


Fig 11 simulation of pwm pulse generations

Figure 11. Explains about the generation of pulses which is required to fire the mosfets present in the matrix converter

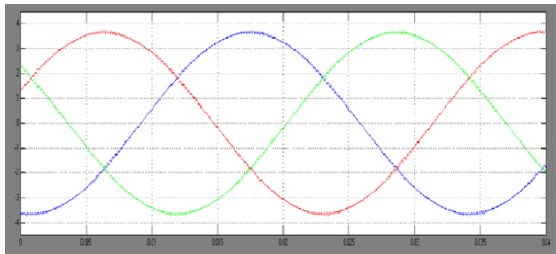


Fig 11 output current

Figure 11 is the output current of the matrix converter, which is given to motor

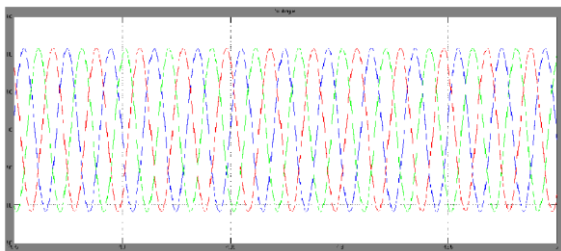


Fig 12 output voltage

Figure 12 is the output voltage of the matrix converter, which is given to motor

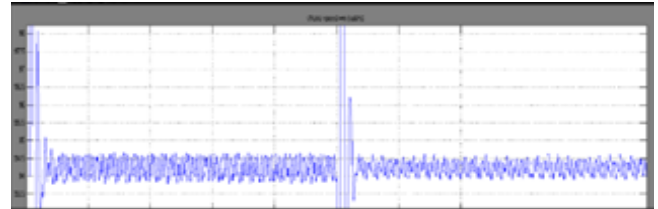


Fig 13 rotor speed

In the fig 13 is the waveform, which explains the speed of the rotor connected.

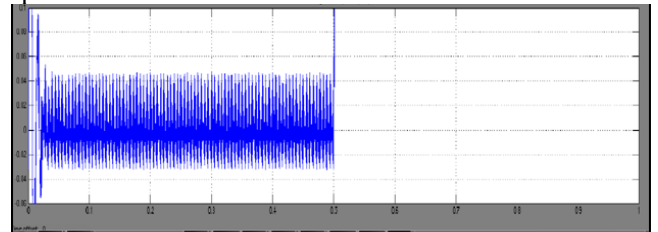


Fig 14 Electromagnetic torque

Fig 14 Electromagnetic torque, Rotation produced by electro magnetic force

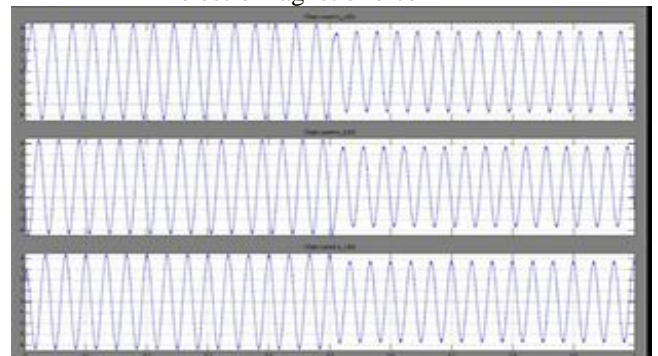


Fig 15 Stator current

Fig 15 Explains Stator current, the current is produced on the stator part of the motor.

V. HARDWARE DESIGN

The hardware consists of four main parts:

1. Power supply unit
2. PWM pulse generator unit
3. Driver circuit unit
4. Power Elementary circuit

A).Power Supply

- 0-12v supply in isolation section
- 0-24v MOSFET section
- 0-15v BLDC motor section

B) Design of Power Supply Unit

The following devices are used to design the power supply unit

1. Step down transformer (230/15v, 1A)
2. Diodes (DIN4007) - 4 NOS
3. Filter capacitor C1 = 2200Micro Farad
C2=C4=C5 = 0.1 Micro Farad
C3=C6 = 10 Micro Farad
4. Voltage regulator 7812 -1C.

5. LED

C) Design of Driver Circuit

The following devices are used to design the driver circuit unit

1. Photocoupler TLP250
2. Low bipolar transistor 2N2222
3. NPN silicon planar transistor CK100
4. Fast recovery rectifier FR107
5. Diode D3
6. Resistor $R1=R3=220$ ohms; $R2=100$ ohms

VI. HARDWARE MODEL

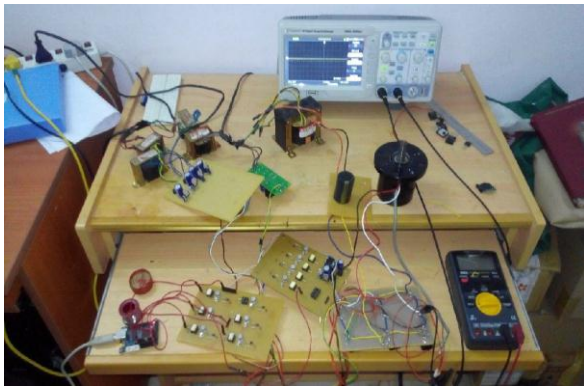


Fig 16 prototype of proposed system

Thus, the expected hardware components of proposed system is discussed in the fig. Thus this result we conclude sinusoidal pulse width modulation technique is efficient that fixed PWM modulation technique. Developing a modified converter to generate sine pulse for industrial voltage applications. Low harmonics with low switching frequency operation, higher efficiency operation with the lowest input voltage, lower input current ripple, and easy tuning with a highly nonlinear load is implemented.

VII. CONCLUSION

This paper explains the analysis and design of a dual three phase indirect matrix converter with carrier phase shift PWM method. This paper describes a new approach to provide dual three phase Sources for two three-phase loads based on IMC. The Proposed IMC topology reduces the number of power devices by two, and is useful and economical in multi drive applications. The proposed converter provides sinusoidal input/output Currents, and has all the advantages of the IMC, such as the possibility of soft switching commutation in the rectifier stage and the simple clamp circuit for safety operation. Also, the carrier based PWM method (which is derived from the relationship With SVPWM) is developed to control the proposed converter effectively to overcome the complexity of the SVPWM method. The algorithm uses only one carrier signal to generate the PWM Signals for all switches, including the

rectifier stage and the inverter Stage; therefore, it is easily implemented based on DSP. In the proposed IMC, the maximum output voltage transfer ratio for each inverter cannot be 0.866 simultaneously; the sum of two voltage transfer ratios is limited within 0.866. Simulation and experimental results demonstrate that the proposed IMC topology and modulation techniques provide the expected benefits.

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