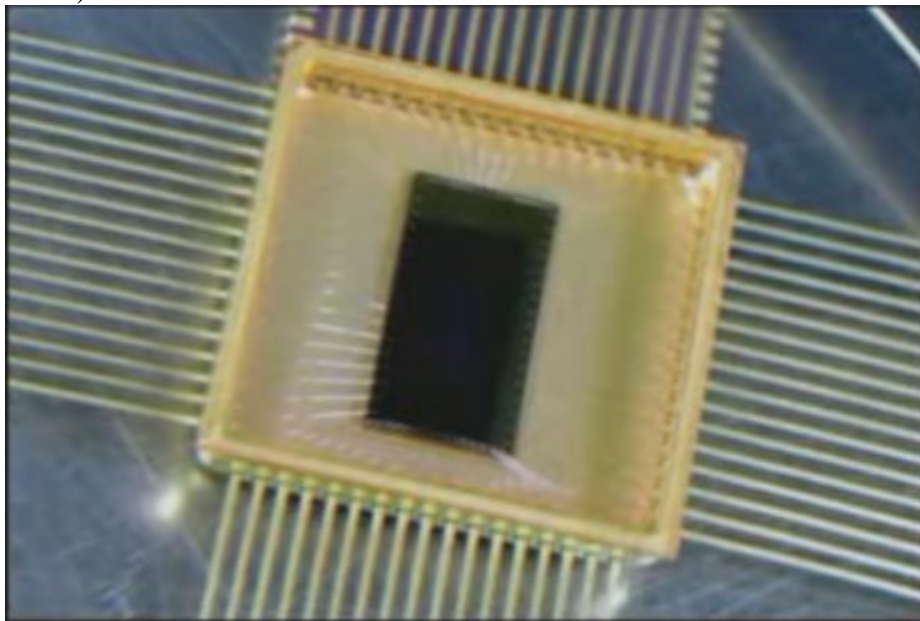


1. Basics of Electronic Design Automation (EDA), manufacturing and Design for Manufacturing (DFM)

1.1 Intro to EDA and DFM

A microsystem is a miniaturized electronic system that combine micro-passive structures, micro-sensors, micro-actuators and micro-processing units for performing tasks and activities. In addition, it is composed also of classical but very small passive and active SMDs and/or bare chips (dice), used to solve the specific tasks (watch the technical presentation from below, created by MEMS Industry Group, emphasizing the fundamentals of microsystems).



An introduction to MEMS (<http://www.youtube.com/watch?v=ZuE4oVrtEQY>)

The film points the essential aspects of developing microsystems/MEMS, as follows:

1. What are MEMS?

- tiny machines, nearly invisible to the human eye - micromachines;
- MicroElectroMechanical Systems describe both a category of devices and a technique of manufacturing;
- 2 categories: Sensors and Actuators;
- sensor devices gather information from their surroundings;
- actuators execute given commands or act generally on highly controlled movements.

2. How MEMS are made?

- thin layers of materials are deposited on a substrate and then are selectively etched away;
- the electrical elements on a chip process data while the mechanical ones act in response to that data = a complete system on a chip;
- the IC part does the thinking part of the system and the MEMS components complement these with active perception and control = MicroSystems Technology (MST).

3. How do MEMS work?

- there are two common examples in today's world: the automotive crash sensor = MEMS Accelerometer, and the digital micromirror device = DMD chip used in Video Projectors, Home Theater Systems, Television;
- in its simple form, the DMD is a light switch;
- one of its many mirrors corresponds to one dot or pixel in the projected image.

4. The future of MEMS

- they will continue to quietly improve life;
- MEMS technology is everywhere: they perform better, respond faster, and are more reliable.

The American term for the microsystem is MEMS, which stands for micro-electro-mechanical system and was started to use in 1980s in USA. The microsystem is a *system* because it have not only sensors and actuators, but also contain electronic circuitry inside which process the signals. Simply speaking, the microsystem is usually a chip/package which integrates electronics, mechanical elements, sensors, and actuators. Miniaturisation of mechanical parts using micro-machining technologies when selectively parts are etched away, it became possible to create mechanical structures on silicon base together with electronic devices.

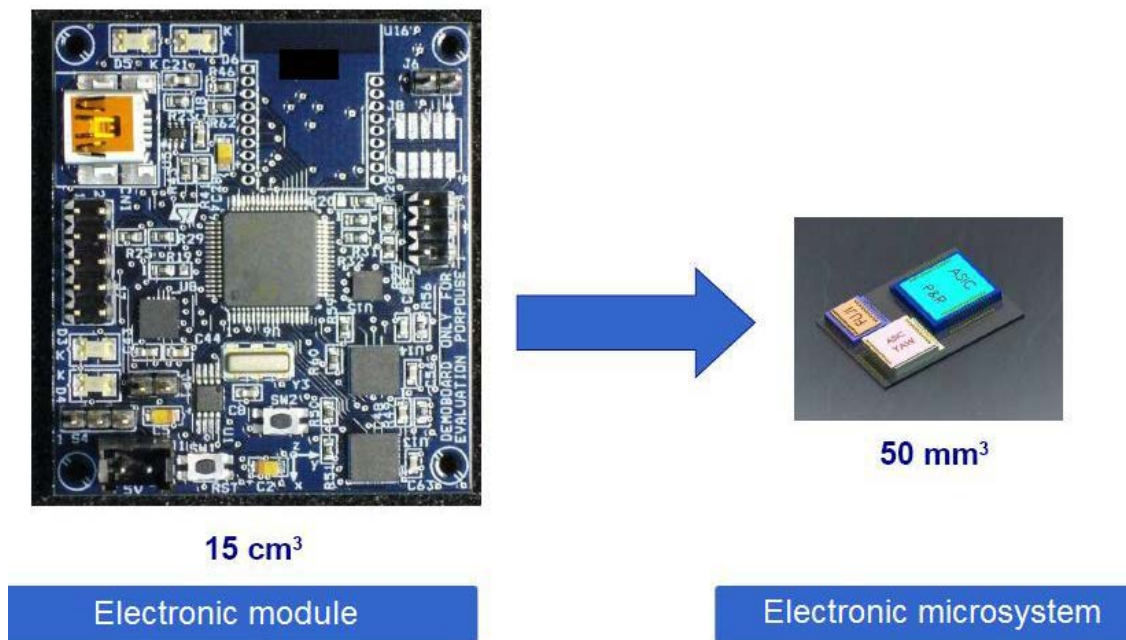
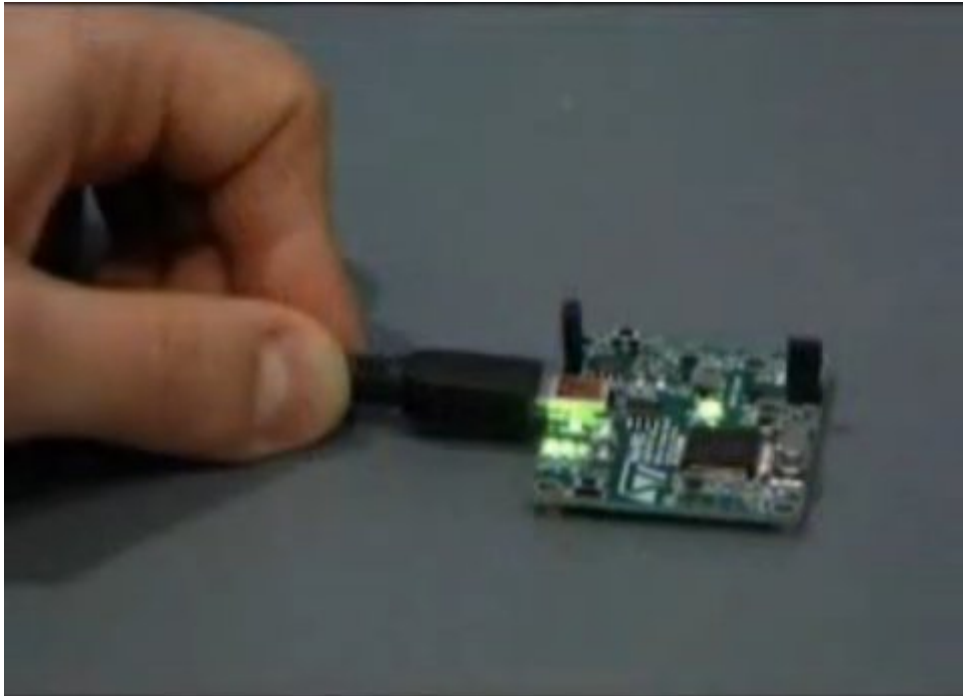


Fig. 1.1.1 The miniaturization from electronic modules to electronic microsystems (source: F. Pasolini, EMPC 2009, Rimini)

Microsystems are used everywhere today, including automotive, industrial even computer hard drives have microsystem sensors for shock protection. Ability to integrate mechanical sensors inside chip made possible to design compact accelerometers, gyroscopes, pressure sensors, sensors with integrated RF, and many more. Also the technology enables now to integrate more than one sensor inside the chip. One of examples may be 3-axis accelerometers (see the demonstration film from below, related to STMicroelectronics MEMS accelerometer family presentation).



STMicroelectronics 3-Axis digital MEMS accelerometers
(http://www.youtube.com/watch?v=BuboEe2D1_A)

Today's cars contain various microsystems inside. Thanks to them, for example, airbag systems can save lives. Micro-mechanical mirror systems exist and work today in optical communications. Figure 1.1.2 presents a zoom of some mechanical parts, placed vertically and horizontally, after the micro-machining process.

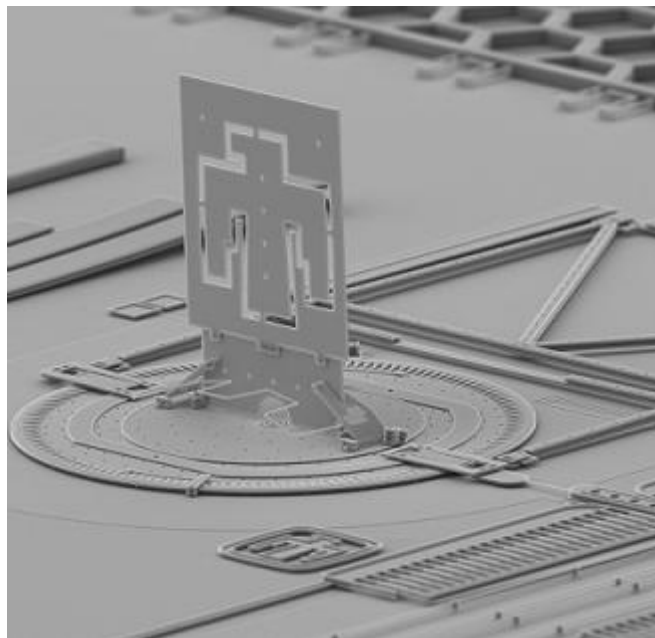


Fig. 1.1.2 Zoom of mechanical parts, placed vertically and horizontally, after the micro-machining process

Microsystems are shrinking today to smaller and smaller sizes from micro to nano scale. Now, there is a new term under focus: „nanosystem”, called also NEMS. The NEMS technology (or nanotechnology) operates in molecular and atomic level. For example, the most interesting area in these years is the self assembly or mimic molecular systems.

The world of electronic and electro-optical packaging is a complex, highly interdisciplinary one that continually faces the challenges of new devices and applications. Levels of integration are doubling on an almost annual basis. Integrated circuits dissipate more power, require more inputs and outputs, operate at ever-increasing speeds, and communicate not only by electrons but also by light. Dual- and quad-core computers operate at clock speeds above 3 GHz, with even higher speeds in laboratories. Systems are using combinations of circuit track, integrated light guides, and free-space optics. Electronic and electro-optical systems are getting smaller and smaller but with everexpanding capability. The commercial electronics and electro-optics market is driven by portability and the wireless interconnect.

In all cases, the systems require a set of fundamental technologies that include not only microelectronics but also photonics, microsystems, RF and wireless. For these functions to be integrated into systems, they have to be designed, fabricated, tested, cooled and reliability assured. In other words, they have to be system-packaged. In the picture 1.1.1 the miniaturization from electronic module to electronic microsystem is presented.

The "electronic packaging" is defined as the engineering and manufacturing science required to convert an electronic circuit into a manufactured product. The complexity degree of an electronic package goes from an integrated circuit package to Printed Circuit Boards and can be extended to all electronic subsystems and systems.

Packaging of microelectronics and microsystems is the science of establishing interconnections and an appropriate operating environment for predominantly electrical (and, in the case of microsystems, also electromechanical) circuits to process and/or store information. Packaging manifests itself in novel and unique creations that ingeniously reconcile and satisfy what seem to be mutually exclusive application requirements and constraints posed by the laws of nature and the properties of materials and processes. All applications can be summed up in three terms: performance, cost and reliability. Packaging can span from the consumer to midrange systems to the high performance/reliability applications. It must be noted that no sharp boundaries exist between the classes, only a gradual shift from optimization for parameters which control performance and cause the cost to increase. The packaging course that follows will summarize the primary package types that will likely apply to microsystems technology and the concerns that traditionally have concerned the microelectronics field.

A package (according to the Webster's dictionary) is a group or a number of things, boxed and offered as a unit. Microsystems packages can contain many electrical and mechanical components. To be useful to the outside world these components need interconnections. Alone, a MEM die sawed from a wafer is extremely fragile and must be protected from mechanical damage and hostile environments. To function, electrical circuits need to be supplied with electrical energy, which is consumed and transformed into mechanical and thermal energies. Because the system operates best within a limited temperature range, packaging must offer an adequate means for removal of heat (see the Thermal Management course in this project).

Electronics manufacturing and packaging technologies have become a significant sector in electronics industry. The fast developing microsystems industry creates today a big pressure to the conventional university and vocational education. The adjustment of the curriculum to provide qualified microsystems packaging knowledge for academia, vocational schools and

industry is a challenging task of the „Packaging Technologies” course. It introduces the fundamental issues of microsystems packaging, system-level technologies, and materials used in electronics industry. In addition, fundamentals of CAD design, modelling and simulation of various structures and computational techniques in packaging technologies shall be delivered. In the final part, the course shall introduce learners in assembling technologies, soldering and solderability, ecological materials and technologies based on RoHS & WEEE European Directives, and basics of nanopackaging.

High-volume, low-cost electronic packaging technologies are critical for many of today's electronics market. Control of electronic packaging technologies provides companies with the competitive capabilities to design and manufacture smaller and more sophisticated products. These products include personal computers, cell phones, microwave ovens, super computers, global positioning systems, automotive and space systems, etc. With innovative merging of semiconductors, packaging, and display technologies, also evolving are second- and third-generation technologies that will increasingly affect the design parameters of future products. Firms with capabilities in materials, equipment, design, and advanced manufacturing will be the future producers of low-cost electronic packages. In table 1.1.1 a worldwide distribution of electronics sectors based on innovation, design, manufacturing and utilisation classes is presented.

Sector	Innovation	Design	Manufacturing	Utilisation
Aerospace	USA	Europe	Europe	USA
Automotive	Europe	Europe	Asia	Europe
Broadcast	Europe	USA	Asia	Europe
Communications	Europe	USA	USA	USA
Computing	USA	USA	Asia	USA
Consumer	Asia	Asia	Asia	World wide
Industrial	Europe	USA	Asia	World wide
Medical	USA	Europe	Europe	Europe
Military	Europe	USA	Europe	USA
Security	Europe	USA	USA	USA

Tab. 1.1.1 Distribution of electronics sectors based on innovation, design, manufacturing and utilisation classes

In order to introduce the "next-generation" products, the companies have had to push the development of a number of advanced technologies:

- fine-pitch devices;
- advanced flex circuit designs;
- cost-effective flip chip technology;
- cost-effective high-density printed circuit boards;
- cost-effective connector technology;
- advanced flat panel display technology;
- small passive components and integrated passive components;
- small, low-cost package assembly equipment;
- high-speed pick and place equipment for ultrasmall components.

Package assembling involves attaching components to the next-level assembly, usually printed circuit boards. “Assembly” includes active plastic and ceramic components containing logic and memory dice as well as passive components as capacitors, resistors, and

inductors. The assembly itself involves either surface mount (SM) or through-hole (TH) attachment. The TH technology (THT) is today more expensive, space-consuming, and heavy compared to SMT. Given the need for both low cost and portability in products, many companies have invested very heavily in and have continually improved the technology to achieve assembly densities of 20 components/cm². Many today products require thin and lightweight packaging. Plastic packages such as QFP, that are surface-mounted onto PCB, have effectively met product requirements. The vision of next-generation products requires packages that are smaller and cheaper than in the past, roughly 50% smaller for each new generation. With the past investments in PCB and SMT technologies, and increased global cost-competitive pressures, the top class companies are expected to pursue the use of plastic packages to the ultimate limit. The ultimate limit accepted by Japan currently is 0.15 mm leadframe pitch, giving rise to 800 pins/30 mm² and 1000 pins/38 mm² sizes. The continued use of P-QFP beyond the current 0.4 mm pitch toward 0.15 mm pitch, however, requires major enhancements in SMT pick and placement tools, solder deposition technologies, reflow tools and technologies, inspection, solder repair for opens and shorts, and electromigration resistance of both the plastic package and the printed circuit board. With the demand for light weight, small size, high performance and low cost systems, the role of packaging is becoming now very important. This is leading to System-in-Package (SIP) and System-on-Package (SOP) technologies for packaging future systems.

As known, the „integrated circuit” (IC) is defined as a miniature or microelectronic device that integrates such elements as transistors, resistors, dielectrics, and capacitors into an electrical circuit, possessing a specific function. The "system" refers to all electronic products. "Packaging" is defined as the bridge that interconnects the ICs and other components into a system-level board to form electronic products (figure 1.1.3). The overlap of ICs and Packaging is referred to as Packaged Devices or IC Packaging.



Fig. 1.1.3 The overlap of “IC”, “system” and “packaging” areas

Finally, the overlap of ICs and systems can be referred to as sub-products. These are considered sub-products because they perform a partial function of a system, limited by the magnitude of integration at the IC level and yet they typically don't involve extensive packaging. These "sub" or complete products depend heavily on the high integration of ICs without a dependency on packaging in order to meet a variety of product functions. In the evolution of systems technology, one approach was evolved into systems-on-chip (SOC).

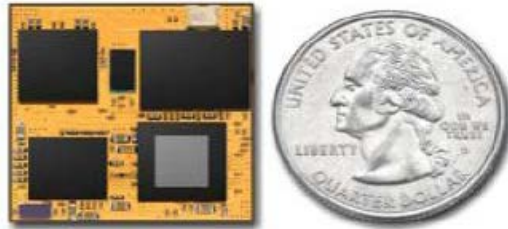


Fig. 1.1.4 The new paradigm called system-on-package-SOP or system-in-package-SIP (example: GSM EDGE i.275/Radio in Package, source: Freescale)

Most, if not all, products, however, are based on a number of packaged ICs and other components assembled onto a system-level board. This is referred to as system-on-board (SOB). A new paradigm called system-on-package (SOP), or system-in-package (SIP) is analogous to SOC, in that it is a single component, multi-function, multi-chip package providing all the needed system-level functions (figure 1.1.4).

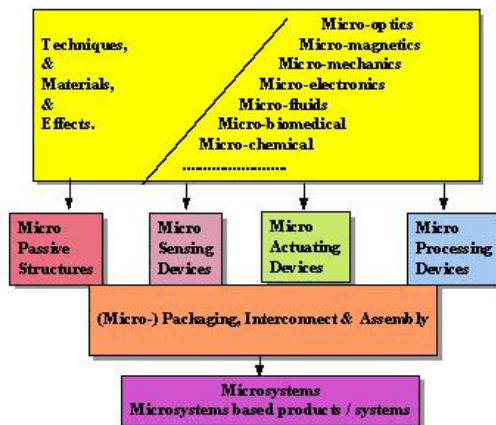


Fig. 1.1.5 The internal structure of a microsystem

Both SOC and SOP/SIP are today the leading „wave” of electronic products. The figure 1.1.5 presents a general internal structure of a microsystem, in which the micro-devices and structures exist and work together with various other bare dice and even SMDs to perform the necessary tasks.

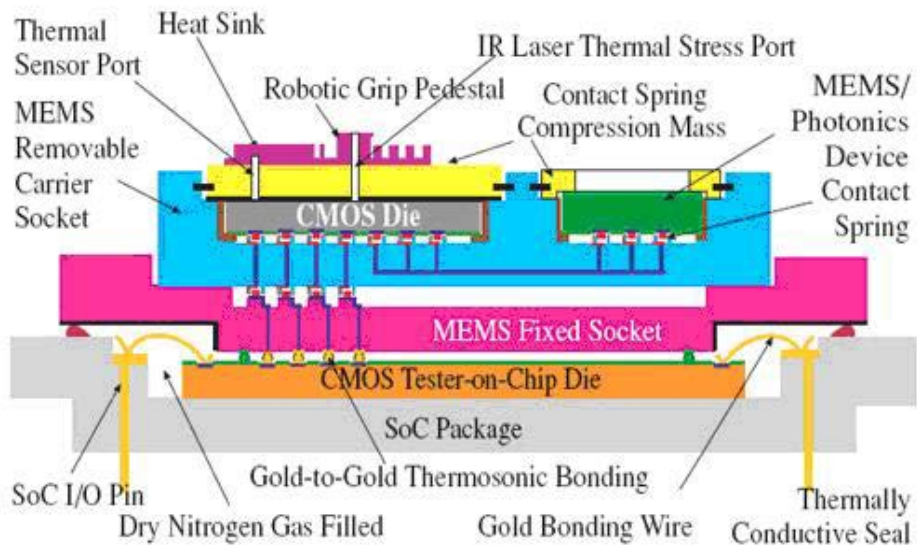


Fig. 1.1.6 Example of SOC microsystem

The figure 1.1.6 depicts a SOC microsystem, placed into a through-hole package, and having inside a stack containing a CMOS tester-on-chip die, and a microsystem (with a CMOS chip and a photonic device) placed into a MEMS fixed socket.

1.2 International standards used in industry. The packaging hierarchy

Microsystems packaging involves two major zones: one is the device (IC) zone, named „IC packaging”, and the other is the system-level, named „system packaging”, as shown in figure 1.2.1.

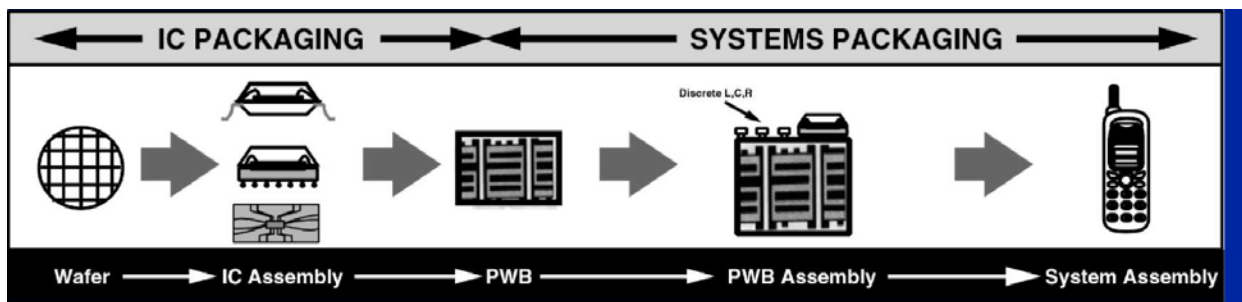


Fig. 1.2.1 IC and system packaging

At the IC level, it involves interconnecting, powering, cooling and protecting the IC. At this level, typically referred to as Level I, the packaging acts as an IC "carrier." The IC carrier, also called „IC package”, allows ICs to be shipped "certified" by IC manufacturers after "burn-in" and electrical tests, to be "ready" for assembling (mounting) onto a system-level board by end product or contract manufacturers. Packaging a single IC does not generally lead to a complete system since a typical system requires a number of different active and passive devices performing different functions. System-level packaging involves interconnection of all these components to be assembled on the system-level board, regardless of the type of component being assembled. The system-level board, also called "motherboard", not only carries these components on top and bottom, but also interconnects every component with printed or aerial wiring in order to form an interconnected system. This „board level” is referred as the 2nd level in the packaging hierarchy (figure 1.2.3).

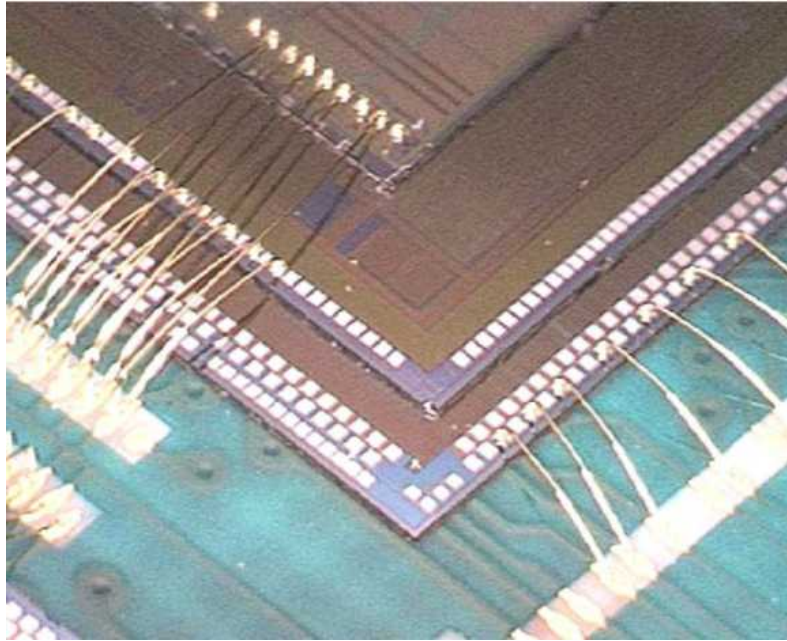


Fig. 1.2.2 Stacked dice (chips) connected with wire-bonding

In forming an electrically-wired system-level board with assembled components, there are two additional interconnections that need to be made. First, interconnection must occur at the IC level where the input/output (I/O) pads on the IC are connected to the first level of the packaging. This is typically done by wire bonding (figure 1.2.2) the components to a lead frame that has been fabricated to a specific shape in order to make it ready for interconnection to the next level of packaging. This is referred to as IC assembly.

The second interconnection is typically achieved by means of solder bonding between the lead frame of the first-level package and electrically conductive pads on the second-level package, which is typically a "board." This is referred to as board assembly. The system-level board, with components assembled on either or both sides, typically completes the system.

There are products, such as mainframes and supercomputers, that require a very large number of ICs. By today's standards, a single system-level board may not carry all the components necessary to form that total system, since some of these require several processors to provide the extremely high transactional throughput. These types of systems might be used to manage large amounts of data such as an airline reservation system or a corporate mainframe network, or process high-resolution imagery such as with certain types of medical equipment. In this case, connectors and cables typically connect the several boards necessary to make the entire system. This is referred to as 3rd level of packaging (figure 1.2.3).

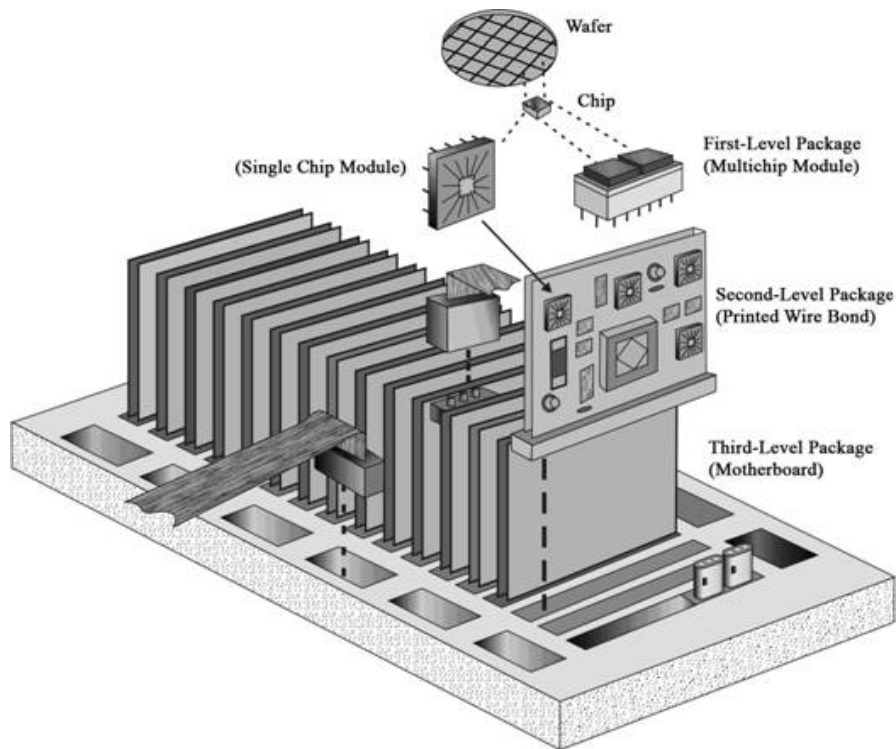


Fig. 1.2.3 The packaging hierarchy with 3 levels (based on R. Tummala concept)

In some references the hierarchy is expanded and consists of 5 levels (0: gate-to-gate interconnections on the chip; 1: chip-to-package interconnections; 2: board level interconnections (printed circuit board - PCB); 3: board-to-board or board-to-motherboard interconnections ; 4: electronic system). Usually, design for manufacturing (DFM) issues have to be implemented in all the levels in order to assure a high performance electronic product development and to match totally the design and the PCB/EMS manufacturing zones.

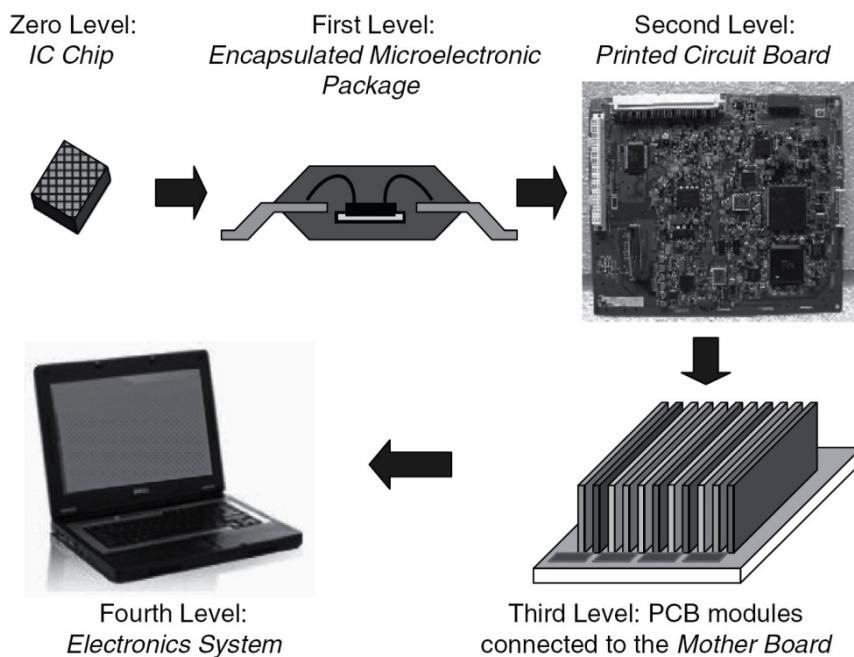


Fig. 1.2.4 The packaging hierarchy with 5 levels (based on M. Pecht concept)

1.3 Overview of DFM issues. Milestones in packaging

Electronic packaging is well over a century old if one includes the 1897 Braun Tube or CRT - Cathode Ray Tube and the vacuum tubes (first decade of 1900). World War II brought a substantial level of miniaturization as the hybrid circuit was perfected that still had to rely on vacuum electronics. But the ceramic technology developed was the basis for ceramic packages later. Vacuum electronics required hermetic packaging that would limit materials to glass, ceramics and metal. However, halfway through the century, the discovery of solid-state electronics would change the industry and packaging. The invention of the transistor, followed by integration leading to the IC, would enable nonhermetic packaging that would come to heavily rely on organic materials, especially plastics. Plastic encapsulation was first used around 1949. The age of plastic packaging allowed considerable innovation that continues, and even accelerates, today. Surface mount, for example, was introduced in the 1960's by IBM as flip chip, but such extreme density, while required for mainframe computers, was not that useful for consumer products. Ironically, the early surface mount flat packs were replaced by the through-hole DIP because the assembly technology was easier (see the documentation film from below, created by the Indian Institute of Technology Kharagpur, regarding MEMS and Microsystems).



Lecture on MEMS & Microsystems by Prof. Santiram Kal, Department of Electronics & Electrical Communication Engineering, I.I.T, Kharagpur
(<http://www.youtube.com/watch?v=j9y0gfN9WMg>)

The major milestones in packaging are as follows:

1. The **hermetic package** or envelope, started with gas-filled devices like the Geissler Tube, but was reduced to a practical product, the Braun Tube, the first CRT, in about 1897. Then came radio electronics that used the same principle and the 1907 Audion from De Forest, marked true electronics packaging because it was the first active device. The glass package evolved to metal and ceramic (figure 1.3.1) and this technology is considered now the modern hermetic package.

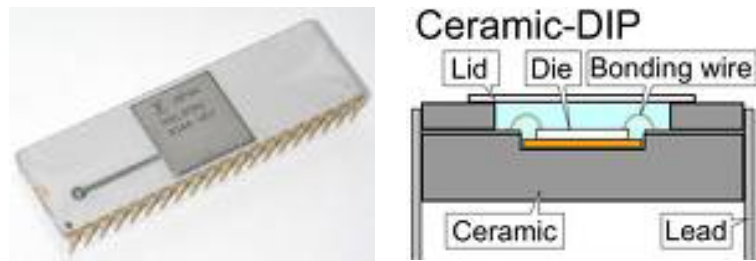


Fig. 1.3.1 The ceramic package (overview and cross section)

2. The **solid-state transistor** had a major impact on packaging. The earliest transistor packaging was a hermetic can, the TO, consisting of a ceramic header and metal cap. But this was really a tiny version of the metal vacuum tube. The next evolution was to replace the metal can with nonhermetic plastic, especially epoxies.

3. The **IC**, which firstly used ceramic hermetic enclosures and ceramic with flip chips. The transition to plastic was a significant event. The flat pack was first, but it was temporarily replaced by the DIP (Dual In-line Package) that became immensely popular since the feed-through format could be automated. Ironically, the surface mount flat pack, and modifications, would come back in the 1980's as part of the surface mount revolution.

4. The **P-DIP (Plastic Dual In-line Package)** format was the most important breakthrough in the entire packaging history, and is still the foundation of modern non-hermetic, low-cost packaging. While it is difficult to attribute the DIP to a single inventor, the earliest patent found was from 1964, being designed for multiple transistors rather than an IC. The DIP was the first low cost plastic package that could be used with ICs and the absolute reference of plastic packages for many decades.

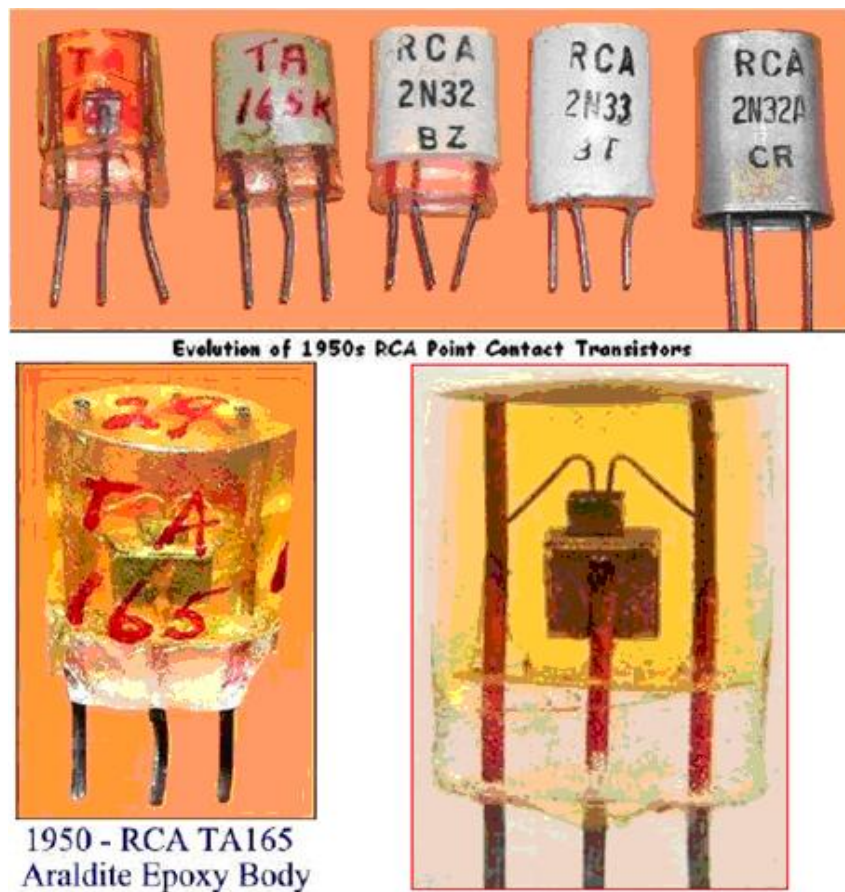


Fig. 1.3.2 The earliest packages of transistors (source: RCA archive)

The DIP (figure 1.3.3), SIP and quad-type versions dominated the industry until the SMT finally became the preferred style in the late 1980's. But, from time to time, the DIP leads were bent outward to enable SMT even before surface mount became popular. Texas Instruments used this idea for their calculators some time in the 1970's.



Fig. 1.3.3 The DIP package (in this case P-DIP)

5. **Flex-based package**, popularized as TAB package (because the process is called “Tape Automated Bonding” figure 1.3.4), was an important concept that began in the 1960's and is still a major packaging technology. While General Electric's Mini-mod was a true TAB, with a window and cantilevered beam leads, it was not the first in flex-based packaging.

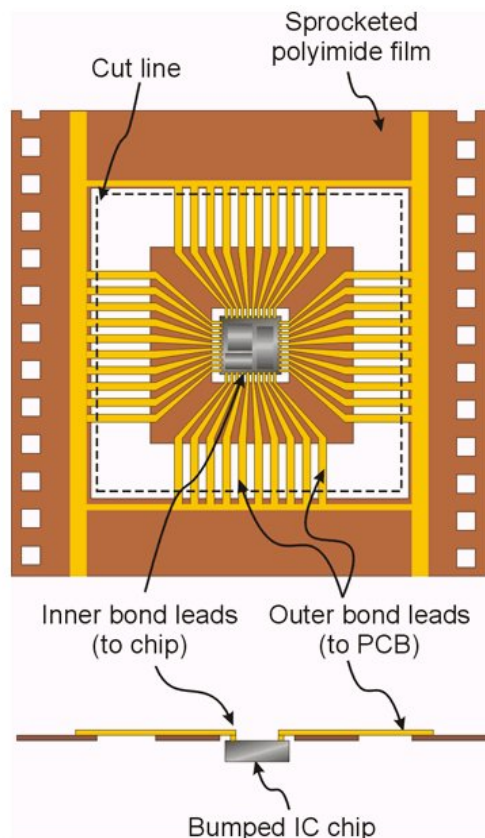


Fig. 1.3.4 The TAB, top view and side view (source: answers.com/ Computer Desktop Encyclopedia)

6. **Flip Chip**, a system that was not quite viewed as a package, was invented in the 1960's by IBM, but remained somewhat of a captive technology for mainframe computers. Today, it is considered a true package by many, but not all, and is playing an important role well beyond

computers. The first flip chip product was SLT (Solid Logic Technology) that was applied to the transistor in 1964 where copper balls were soldered to under bump metallization. While flip chip worked well for transistors, the introduction of the IC would require modification. The copper balls were replaced with solder balls that could be mass-applied by a vacuum-deposition process. The new flip chip design was called C4 (actually C⁴) for Controlled Collapse Chip Connection. Flip chip, now about 40 years old, is probably today's fastest growing method for high density. C4 appears to be the first WLP (Wafer Level Package).

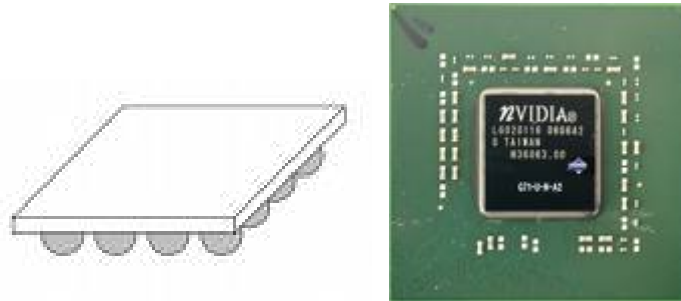


Fig. 1.3.5 The flip chip, overview and placement onto a PCB (for forming a BGA package)

7. **SMT (surface mount technology)** was the next big step as it moved the industry from less-efficient through-hole, but there are two distinct lines of technology. While the early 1980's marked the beginning of SMT in plastic packages, IBM's flip chip in the 1960's, was the first SMT. This is another time-was-right technical event that evolved from many sources and it's not easy to pin down a single inventor since there were early packages that were surface mounted, like IBM's flip chip and versions of flat packs from many companies.

8. The **Array Package** is the practical low-cost format. The plastic Ball Grid Array (PBGA) was one of the important events in packaging. The common perimeter style packages had reached a point where more I/Os in a smaller area was impractical. Introduced as Motorola's Ompak, this was the package that succeeded with the right density solution. Although area array footprints had been known for some time, it was Bruce Freyman who took the lead with plastic overmolded area array and made it happen. Freyman is considered a co-inventor on Motorola BGA patents.

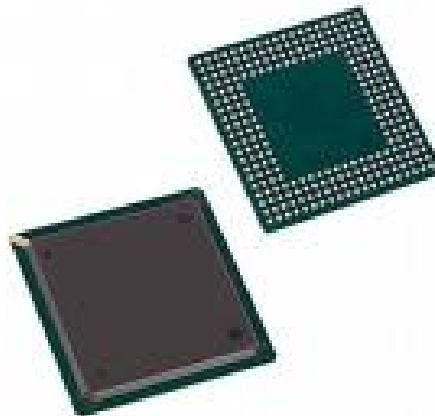


Fig. 1.3.6 The BGA package (top and bottom views)

9. The **CSP (Chip Scale Package)** launched as Tessera's **µBGA** (figure 1.3.7), marked another milestone. Both from IBM, they were well aware of the need for very high-density packaging. The breakthrough idea was to take the basic TAB (Tape Automated Bonding) concept, but remove the outer leads that were always a problem for assembly, and also took up too much area. Their idea was to use a fan-in geometry instead of the common fan-out

used in TAB and other packages. This would require a BGA interconnect. The original design used a single metal layer flex circuit construction with laser-drilled vias on the bottom. The first bumps were created by electroplating copper forming a post within the via and allowing the plating to continue until a mushroom bump had formed. Later, micro-spheres of solder were used to replace the copper. The successful product was the μ BGA that helped launch Chip Scale Packaging.



Fig. 1.3.7 The μ BGA package (source: tessera.com)

Modern packaging is more or less the continuing evolution of the earlier ideas from above. Packaging concepts that are now receiving considerable attention are:

- multichip packages;
- stacked dice;
- stacked packages (or package-on-package - POP);
- wafer-level packages.

All can be traced back to earlier times. Stacked packages and wafer-level methods, for example, were used in the 1960's by IBM. These SLT flip chips were mounted on ceramic chip carriers that were stacked. The bottom carrier had a Pin Grid Array (PGA) format. The flip chip under bump metallization and bumps were formed at wafer-level; the first WLP process. Some "newer" methods, like laser vias in ICs, are more or less the reapplication of mature technologies to new problems. **The industry needs to wait for nanoelectronics to mature before the next big event in packaging.**

Packages and technologies

The development of the IC and microsystem packages is a dynamic technology. Applications that were unattainable only a few years ago are today common place thanks to advances in packaging technologies. From mobile telecommunications and satellite broadcasting to aerospace and automotive applications, each imposes its own individual demands on the electronic package. To meet such a diverse range of application requirements, the package range encompasses over thirty different types, most of which are sub-divided into a number of outline versions. Basically, from the mounting/assembling technology of electronic components point of view, the packages are classified in **through-hole mounted packages/devices (THP/THD)** and **surface mounted packages/devices (SMP/SMD)**.

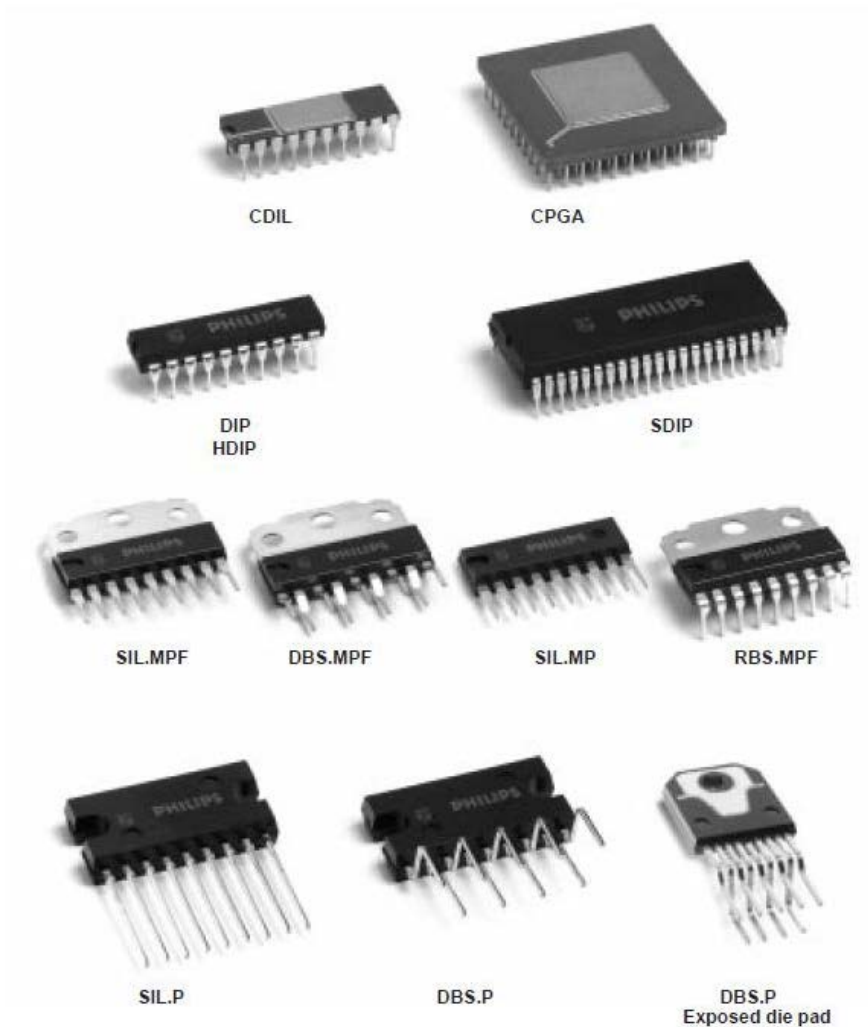


Fig. 1.4.1 Through-hole mounted packages/devices (THP/THD)

Through-hole technology (THT), also spelled "thru-hole", refers to the mounting technology that involves the use of terminals of components (THD) that are inserted into holes (PTH - Plated Through-Hole) drilled in the printed circuit board (PCB) and soldered to pads on the opposite side. While through-hole mounting provides strong mechanical bonds when compared to surface-mount technology (SMT), the additional drilling required makes the boards more expensive to produce today. Surface-mount technology was developed in the 1960s and became widely used in the late 1980s. Much of the pioneering work in this technology was by IBM. A SMT component is usually smaller than its through-hole counterpart because it has either smaller leads or no even no leads. It may have short terminals of various styles, flat contacts, a matrix of solder balls, or terminations on the body of the component. The electronic components (SMD) are mounted directly onto the surface of the printed circuit board.

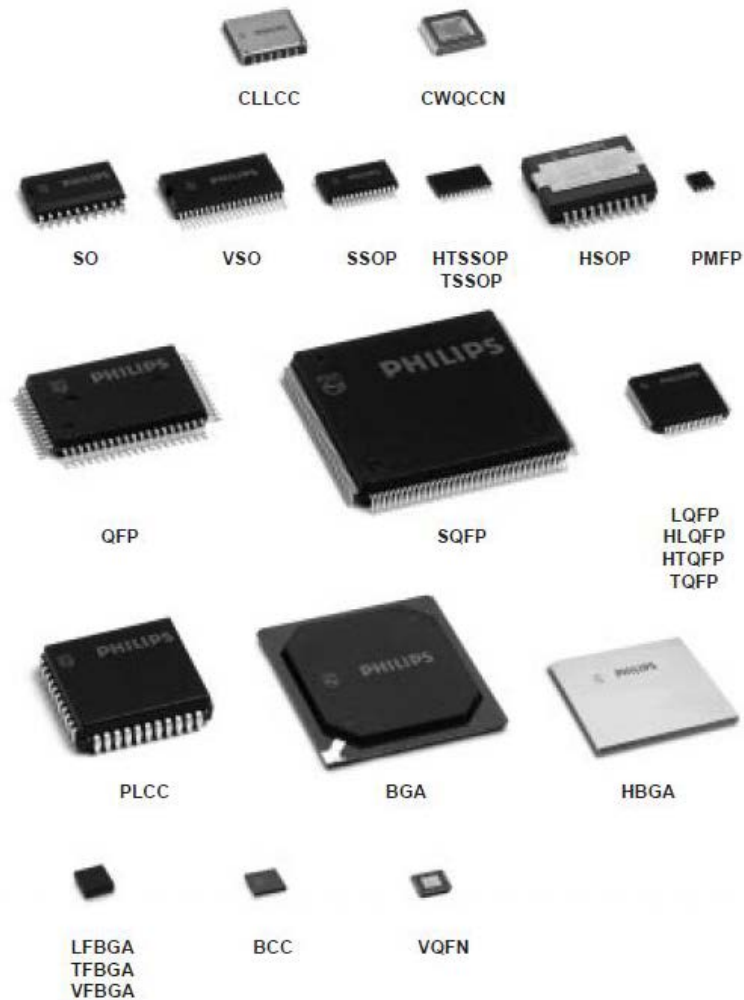


Fig. 1.4.2 Surface mounted packages/devices (SMP/SMD)

The package of a microsystem serves to integrate all of the components required for a system application in a manner that minimizes size, cost, mass and complexity. The package provides the interface between the components and the overall system. The four main functions of a microsystem package are the following:

1. mechanical protection;
2. environment protection;
3. electrical connection to other electronic components;
4. thermal support to evacuate the heat.

1. Mechanical protection

Due to the dimension of a microsystem, the requirements to support and protect it from thermal and mechanical shock, vibration, high acceleration, particles, and other physical damage (possibly radiation) during storage and operation of the part become critical. The mechanical stress endured depends on the application. The coefficient of thermal expansion (CTE) of the package should be equal to or slightly greater than the CTE of silicon for reliability, since thermal shock or thermal cycling may cause die cracking and delamination if the materials are unmatched or if the silicon is subject to tensile stress. Other important parameters are thermal resistance of the carrier, the material's electrical properties, and its chemical properties (resistance to corrosion, for example).

Once the microsystem is supported on a carrier, the wire bonds or other electrical connections are made, and the assembly must be protected from scratches, particles, and other physical damage. This is accomplished either by adding walls and a cover to the base or by encapsulating the assembly in plastic or other material. Since the electrical connections to the package are usually made through the walls, the walls are typically made from glass or ceramic. The glass or ceramic can also be used to provide electrical insulation of the leads as they exit through a conducting package wall (metal or composite materials). Although the CTE of the package walls and lid do not have to match the CTE of silicon based microsystems as they are not in intimate contact (unless an encapsulating material is used), it should match the CTE of the carrier or base to which they are connected.

Many microsystems are designed to measure something in the immediate surrounding environment. These devices range from biological sensors to chemical microsystems that measure concentrations of certain types of liquids. So the traditional hermeticity that is generally thought of protecting microelectronic devices may not apply to all microsystems. These might be directly mounted to a printed circuit board (PCB) or a hybrid-like ceramic substrate and have nothing but a “housing” to protect them from mechanical damage such as dropping or damages from the operator's thumb (watch the presentation film below, created by Koichi Tanaka, as an example application of MEMS).



Muscle wire actuator test (http://www.youtube.com/watch?v=MOldGcb_ZvA)

2. Environment protection : hermetic vs. non-hermetic

Many elements in the environment can cause corrosion or physical damage to the metal lines of the microsystem as well as other components in the package. The susceptibility of the microsystems to moisture damage is dependent on the materials used in manufacturing. For example, Al lines can corrode quickly in the presence of moisture, whereas Au lines degrade slowly, if at all, in moisture. Also, junctions of dissimilar metals can corrode in the presence of moisture. Moisture is readily absorbed by some materials used in the microsystems fabrication, die attachment, or within the package; this absorption causes swelling, stress, and possible delamination. To minimize these failure mechanisms, microsystems packages for high reliability applications may need to be hermetic with the base, sidewalls, and lid

constructed from materials that are good barriers to liquids and gases and do not trap gasses that are later released.

3. Electrical connection to other electronic structures and components

Because the package is the primary interface between the microsystem and the system, it must be capable of transferring DC power and signals. In addition, the package can be required to distribute the DC and signals to other components inside the package. The drive to reduce costs and system size by integrating more microsystems and other components into a single package increases the electrical distribution problems as the number of interconnects within the package increases.

When designs also require high frequency signals, the signals can be introduced into the package along metal lines passing through the package walls, or they may be electromagnetically coupled into the package through apertures in the package walls. Ideally, RF energy is coupled between the system and the microsystem without any loss in power, but in practice, this is not possible since perfect conductors and insulators are not available. In addition, power may be lost to radiation, by reflection from components that are not impedance matched, or from discontinuities in the transmission lines. The final connection between the microsystem and the DC and signal lines is made with wire bonds, flip-chip die attachment and multilayer interconnects (with thin dielectric).

4. Thermal support

Usually, for small signal circuits, the temperature of the device junction does not increase substantially during operation, and thermal dissipation is not a real issue. This was also the case for singular microsystem in the past. However, with the push to increase the integration and the power of microsystems, all within a single package, the temperature rise in the device junctions can be substantial and cause the circuits to operate in an unsafe region. Therefore, thermal dissipation requirements for power amplifiers, other large signal circuits, and highly integrated packages can place severe design constraints on the package design (see the “Thermal Management” course in this project).

Each microsystem application usually requires a specific package design in order to optimize its performance and to meet the requirements of the system. The main categories of are:

1. metallic packages;
2. ceramic packages;
3. plastic packages;
4. thin-film multilayer packages.

1. Metallic packages

Metallic packages are often used for RF/microwave multichip modules and hybrid circuits because they provide excellent thermal dissipation and excellent electromagnetic shielding. They can have a large internal volume while still maintaining mechanical reliability. The package can use either an integrated base and sidewalls with a lid or separated base, sidewalls, and lid. Inside the package, ceramic substrates or chip carriers are required for use with the feedthroughs.

The selection of the proper metal can be critical. CuW (10/90), Silvar™ (a Ni-Fe alloy), CuMo (15/85), and CuW (15/85) all have good thermal conductivity and a higher CTE than silicon, which makes them good choices. Kovar™, a Fe-Ni-Co alloy commonly. All of the

above materials, in addition to Alloy-46, may be used for the sidewalls and lid. Cu, Ag, or Au plating of the packages is commonly done.

Before final assembling, a bake is usually performed to drive out any trapped gas or moisture. This reduces the onset of corrosion-related failures. During assembling, the highest temperature curing epoxies or solders should be used first and subsequent processing temperatures should decrease until the final lid seal is done at the lowest temperature to avoid later steps damaging earlier steps. Au-Sn is a commonly used solder that works well when the two materials to be bonded have similar CTEs. Au-Sn solder joints of materials with a large CTE mismatch are susceptible to fatigue failures after temperature cycling. The AuSn intermetallics that form tend to be brittle and can accommodate only low amounts of stress.

Welding (using lasers to locally heat the joint between the two parts without raising the temperature of the entire part) is a commonly used alternative to solders. Regardless of the seal technology, no voids or misalignments can be tolerated since they can compromise the package hermeticity. Hermeticity can also be affected by the feedthroughs that are required in metal packages. These feedthroughs are generally made of glass or ceramic and each method (glass seal or aluminum feedthrough) has its weakness. Glass can crack during handling and thermal cycling. The conductor exiting through the ceramic feedthrough may not seal properly due to metallurgical reasons. Generally, these failures are due to processing problems as the ceramic must be metallized so that the conductor (generally metal) can be soldered (or brazed) to it. The metallization process must allow for complete wetting of the conducting pin to the ceramic. Incomplete wetting can show up as a failure during thermal cycle testing.

2. Ceramic Packages

Ceramic packages have several features that make them especially useful for microelectronics as well as microsystems. They provide low mass, are easily mass produced, can be low-cost, can be made hermetic, and can more easily integrate signal distribution lines and feedthroughs. They can be machined to perform many different functions. By incorporating multiple layers of ceramics and interconnect lines, electrical performance of the package can be tailored to meet design requirements. These types of packages are generally referred to as co-fired multilayer ceramic packages. Multilayer ceramic packages also allow reduced size and cost of the total system by integrating multiple microsystems and/or other components into a single, hermetic package. These multilayer packages offer significant size and mass reduction over metal-walled packages. Most of that advantage is derived by the use of 3 dimensions instead of 2 for interconnect lines. Co-fired ceramic packages are constructed from individual pieces of ceramic in the "green" (unfired) state. These materials are thin, pliable films. During a typical process, the films are stretched across a frame. On each layer, metal lines are deposited using thick-film processing (usually screen printing), and via holes for interlayer interconnects are drilled or punched. After all of the layers have been fabricated, the unfired pieces are stacked and aligned using registration holes and laminated together. Finally, the part is fired at a high temperature. The components are then attached into place (usually organically (epoxy) or metallurgically (solders), and wire bonds are made the same as those used for metal packages.

Several problems can affect the reliability of this package type. First, the green-state ceramic shrinks during the firing step. The amount of shrinkage is dependent on the number and position of via holes and cuts into each layer. Therefore, different layers may shrink more than others, creating stress in the final package. Second, because ceramic-to-metal adhesion

is not as strong as ceramic-to-ceramic adhesion, sufficient ceramic surface area must be available to assure a good bond between layers. This eliminates the possibility of continuous ground planes for power distribution and shielding. Instead, metal grids are used for these purposes. Third, the processing temperature and ceramic properties limit the choice of metal lines. To eliminate warping, the shrinkage rate of the metal and ceramic must be matched. Also, the metal must not react chemically with the ceramic during the firing process. The metals most frequently used are W and Mo. There is a class of Low Temperature Co-fired Ceramic (LTCC) packages. The conductors that are generally used are Ag, AgPd, Au, and AuPt. Ag migration has been reported to occur at high temperatures, high humidity, and along faults in the ceramic of LTCC.

3. Plastic Packages

Plastic packages have been widely used by the electronics industry for many years and for various applications because of their low manufacturing cost. High reliability applications are an exception because various reliability questions have been raised. Plastic packages are not hermetic, and hermetic seals are generally required for high reliability applications. The packages are also susceptible to cracking in humid environments during temperature cycling of the surface mount assembly of the package to the motherboard.

Most microsystem designs either have moving parts or do not allow for intimate contact of an encapsulating material such as in a traditional plastic package. Furthermore, plastic packages have not gained wide acceptance in the field of high reliability applications. Studies have shown that during the high-temperature soldering process encountered while mounting packaged semiconductor devices on circuit boards, moisture present in a plastic package can vaporize and exert stress on the package. This stress causes the package to crack and also causes delamination between the mold compound and the lead frame or die. This phenomenon is often referred to as „popcorn” cracking. These effects are most pronounced if the package has greater than 0.23% absorbed moisture before solder reflow. The cracks can provide a path for ionic contaminants to reach the die surface, and/or die delamination can cause wire-bond failure.

JEDEC defines five classes for moisture resistance of plastic packages and sensitivity to „popcorning”. Class 1 is defined as unlimited exposure to moisture and the package will still not exhibit delamination during the surface mount operation. Class 5 can tolerate minimal exposure to moisture before it needs to be dried (by baking in an oven set at ~125°C for a duration of 8...24 hours depending on the package). Classes 2 through 4 are defined as somewhere in between the extremes. Most commercial packages are classified as class 3 moisture resistant. To overcome the delamination problem, results derived from numerical simulation and experimental data can serve as a guide in the selection of suitable molding compound properties.

The last mechanisms by which a chip can fail in a plastic package are caused by bond-wire sweep and lift-off, which in turn are caused by the viscous flow of the molten plastic mold compound. The viscosity of the molten plastic is a function of the filler particle size and concentration. Research activities have shown that in the cases of three wire bonds placed at different positions of chip vs. board, the one with a raised chip experiences the largest maximum displacement. Further, the raised chip and the downset die experience maximum stress at the ball bonds. In these cases, plastic deformation of the ball bonds is a major cause of failure. In contrast, the wire bond for the double-downset die suffers only elastic

deformation. Thus, the double downset is the recommended device layout to minimize bond wire sweep.

4. Thin-Film Multilayer Packages

Within the broad subject of thin-film multilayer packages, two general technologies are used. One uses sheets of polyimide laminated together in a way similar to that used for the LTCC packages described above, except a final firing is not required. Each individual sheet is typically 25 μm and is processed separately using thin-film metal processing. The second technique also uses polyimide, but each layer is spun onto and baked on the carrier or substrate to form thick layers. In this method, via holes are either wet etched or reactive ion etched (RIE). The polyimide has $\epsilon_r = 2.8 - 3.2$. Since the permittivity is low and the layers are thin, the same characteristic impedance lines can be fabricated with less line-to-line coupling; therefore, closer spacing of lines is possible. In addition, the low permittivity results in low line capacitance and therefore faster circuits.

Advanced packages and assembling technologies for microsystems

The method used to attach a microsystem to a package is a general technology applicable to most integrated circuit devices. Generally, referred to as “chip (die) attach”, the function serves several critical functions. The main function is to provide good mechanical attachment of the microsystem structure to the package base. This ensures that the microsystem chip (if the microsystem is composed of only one chip) does not move relative to the package base. It must survive hot and cold temperatures, moisture, shock and vibration. The attachment may also be required to provide a good thermal path between the microsystem structure and the package base. Either the heat is generated by the microsystem or by the support circuitry, the attachment material should be able to conduct the heat from the chip to the package base. The heat can be conducted away from the chip and “spread” to the package base which is larger in size and has more thermal mass. This spreading can keep the device operating in the desired temperature range. If the support circuitry requires good electrical contact from the silicon to the package base, the attachment material should be able to accommodate the task. The stability and reliability of the attach material is largely dictated by the ability of the material to withstand thermomechanical stresses created by the differences of the thermal expansion coefficients between the microsystem silicon and the package base material. These stresses are concentrated at the interface between the microsystem silicon backside and the attach material and the interface between the die attach material and the package base. Silicon has a CTE of 2 ... 3 ppm/ $^{\circ}\text{C}$ while most package bases have higher CTE (6 ... 20 ppm/ $^{\circ}\text{C}$).

Voids in the die attach material cause areas of localized stress concentration that can lead to premature delamination. Presently, microsystem packages use solders, adhesives or epoxies for die attach. Each method has advantages and disadvantages that affect the overall microsystem reliability. Generally, when a solder is used, the silicon die would have a gold backing. Au-Sn (80-20) solder generally is used and forms an Au-Sn eutectic when the assembly is heated to approximately 250 $^{\circ}\text{C}$ in the presence of a forming gas. When this method is applied, one exists a single rigid assembled part with low thermal and electrical resistances between the microsystem device and the package. One problem with this attachment method is that the solder attach is rigid (and brittle) which means it is critical for the microsystem device and the package CTEs match since the solder cannot absorb the stresses.

Adhesives and epoxies are comprised of a bonding material filled with metal flakes. Typically, Ag flakes are used as the metal filler since it has good electrical conductivity and has been shown not to migrate through the die attach material. These die attach materials have the advantage of lower process temperatures. Generally, the material is cured between 100 and 200°C. They also have a lower built-in stress from the assembly process as compared to solder attachment. Furthermore, since the die attach does not create a rigid assembly, shear stresses caused by thermal cycling and mechanical forces are relieved to some extent. One particular disadvantage of the soft die attach materials are that they have a significantly higher electrical resistivity which is 10...50 times greater than solder and a thermal resistivity which is 5...10 times greater than solder. Lastly, humidity has been shown to increase the aging process of the die-attach material.

In the following pages the most advanced packages and structures are presented deeper (first, watch the presentation film from below, created by DIGINFO Video News, as an example application of MEMS).



MEMS Dust: No Batteries Required (<http://www.youtube.com/watch?v=aksrK17rRQ4>)

- **Flip Chip (Controlled Collapse Chip Connection)**

Flip Chip (FC) is an interconnect technology developed by IBM in the 1962 as an alternative to manual wire bonding. At the beginning, the name was Solid Logic Technology (SLT), being changed in 1970 in Controlled Collapse Chip Connection (C4). C4 is the today Flip Chip (FC) package and technology. It attaches a chip with the circuitry facing the substrate. FC uses solder bumps deposited through a Bump Mask onto wettable chip pads that connect to matching wettable substrate pads. The microsystems technology initially did not use flip chip packaging but the drive toward miniaturization necessitates today its incorporation into designs and products.

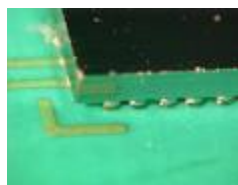


Fig. 1.4.3 Zoom of a flip chip mounted onto PCB

The "flipped" chips align to corresponding substrate metal patterns. Electrical and mechanical interconnects are formed simultaneously by reflowing the bumps. The FC joining process is self-aligning, e.g., the wetting action of the solder will align the chip's bumps pattern to the corresponding substrate pads. This action compensates for slight chip-to-substrate misalignment incurred during chip placement. An added feature of FC is the ability to rework. Several techniques exist that allow for removal and replacement of FCs without scrapping the chip or substrate. In fact, rework can be performed numerous times without degrading quality or reliability. For improved reliability, chip underfill is useful to be injected between the joined chip and substrate (figure 1.4.4). It should be underlined that any rework must be performed prior to application of chip underfill.

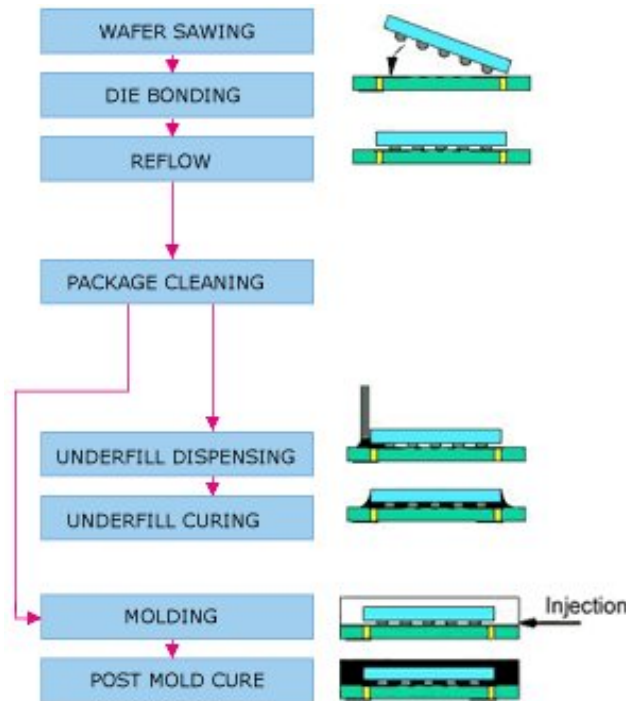


Fig. 1.4.4 The assembling technology of flip chip devices (source: stmicroelectronics.com)

It is important to recognize certain FC characteristics when deciding on an interconnect technology. While application, size, performance, reliability and cost all must be factored in the selection process. However, these factors cannot be applied to the chip or product only. The overall impact at the system level must be considered for an equivalent comparison. The advantages of FC include: size and weight reduction, applicability for existing chip designs, increased I/O capability, performance enhancement, increased production capability, rework/chip replacement. Based on these, it is clear that FC provides performance, size and I/O density improvements, the entire chip surface being used for interconnect pad locations. Theoretically, a FC can have more than 2500 bumps, today chips with over 1500 bumps being in production.

From the interconnection design and manufacturing, FC enables increased density. Signals, clock and power connections can be placed almost anywhere on the chip creating minimum noise and skew, current capacity and lines length. Additionally, on-chip wiring can be reduced since z-axis escapes are available where needed.

The reliability of FC contacts is determined by the difference in the CTE between the chip and the ceramic substrate or the organic printed circuit board (PCB). Knowing the CTE of

silicon from above, one must note that for 96%-alumina it is 6.4 ppm/°C and for PCB is around 20...25 ppm/°C. The CTE mismatch between the chip and the carrier induces high thermal and mechanical stresses and strain at the contact bumps. The highest strain occurs at the corner joints, whose distance is the largest from the distance neutral point (DNP) on the chip. For example, the DNP for a 2.5 x 2.5 mm chip is 1.7 mm. The thermomechanical stress and strain cause the joints to crack (when cracks become large, the contact resistance increases significantly). The tradeoff in selecting the bump height is that large bumps introduce a series inductance that degrades high-frequency performance and increases the thermal resistance from the device to the carrier, if that is the primary heat path.

The reliability of the bump joints is improved if, after reflow, a bead of encapsulating epoxy resin is dispensed near the chip and drawn by capillary action into the space between the chip and the carrier. The epoxy is then cured to provide the final flip-chip assembly. The epoxy-resin underfill mechanically couples the chip and the carrier and locally constrains the CTE mismatch, thus improving the reliability of the joints. The most essential characteristic of the encapsulant is a good CTE match with the z-expansion of the solder or the bump material. Underfilling also allows packaging of larger chips by increasing the allowable DNP. In some cases, the encapsulant acts as a protective layer on the active surface of the chip. Good adhesion among the underfill material, the carrier, and the chip surface is needed for stress compensation. The adhesion between the surfaces can be lost and delamination can take place if contaminants, such as post-reflow flux residue, are present. For this reason, a fluxless process for flip-chip assembly is desirable. Unfortunately, flip-chip bonding on PCB requires the use of flux. However, on ceramic carriers with gold, silver, and palladium-silver thick-film patterns and via metallizations, fluxless flipchip thermocompression bonding with gold-tin bumps has demonstrated high reliability.

Finally, one should be taken that the encapsulant or underfill covers the entire underside without air pockets or voids, and forms complete edge fillets around all four sides of the chip. Voids create high-stress concentrations and may lead to early delamination of the encapsulant. After assembly, a scanning acoustic microscope can be used to locate voids in the encapsulant. The encapsulant should also be checked for microcracks or surface flaws, which have a tendency to propagate with thermal cycling and environmental attacks, eventually leading to chip failure.

- **Ball-Grid-Array (BGA)**

Ball Grid Array is a surface mount chip package that uses a grid of solder balls as its connectors. It is noted for its compact size, high lead count and low inductance, which allows lower voltages to be used. BGAs come in plastic and ceramic varieties, having the components placed on only one side.

There is one other common packaging for integrated circuits and this is the PGA or Pin Grid Array. The BGA looks physically similar to a Pin Grid Array package. Both are one-sided, having only one side of the semi-conducting substrate used for printing and mounting of circuit components. Moreover, both have an obvious grid-like pattern. However, the Pin Grid Array uses pins - thus, the name - whereas the BGA uses solder balls. It essentially has evolved from the C4 technology whereas more I/Os can be utilized in the same area as in a peripherally leaded package (or chip). The CBGA and PBGA are not truly Chip Scale Packaging but the evolution to the μ BGA has come out of the experience the industry has gained from the CBGA and PBGA packages.

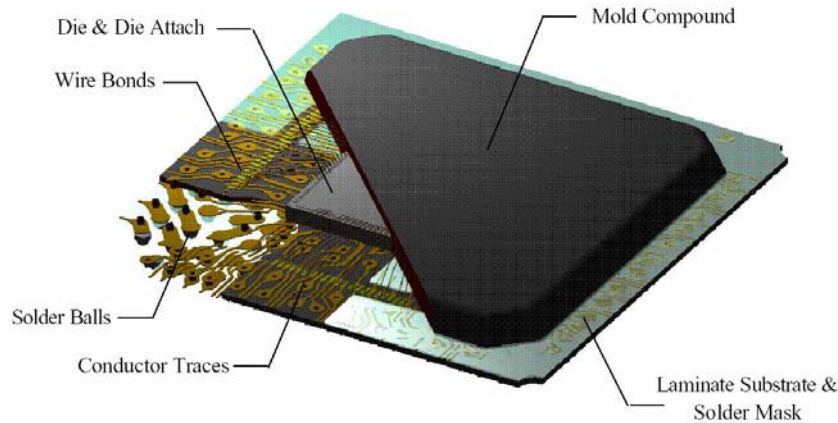


Fig. 1.4.5 Overview of a plastic BGA (Ball Grid Array)

The classical Plastic Ball-Grid-Array (PBGA) is based on the same chip-and-wire technology and has moisture sensitivity (e.g., susceptible to „popcorn” cracking during solder reflow) issues just like plastic packaging. It is different in that it is built on a printed circuit board substrate rather than a leadframe (metal) material. The attach method (to the motherboard) is accomplished by soldering solder balls (bumps). One advantage this technology has over conventional plastic packaging is that the printed circuit board material (FR4, polyimide, BT resin, etc.) can be a simple 2 layer board or be made of multiple layers. Additional layers allow for power and ground planes.

The wire-bonded **MAPBGA** (Molded Array Process Ball Grid Array) is an excellent package for low-performance to mid-performance devices that require packaging with low inductance, ease of surface mounting, low cost, small footprint and excellent package reliability, having the following features: custom substrate designs / ball maps for maximum flexibility and electrical performance; custom ball patterns / full array / depopulated arrays available; 0.5 mm to 1.0 mm pitch; substrates with standard PCB manufacturing technology; 2L and 4L (L-layer) substrates available; high I/O with smaller footprints available; maximum thickness from 1.00 mm to 2.65 mm; RoHS capability (till 260°C reflow); Pb-free solder balls available.

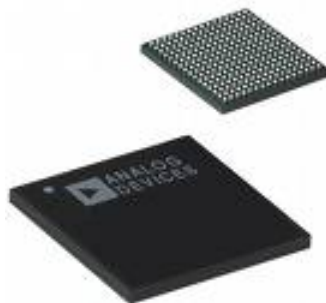


Fig. 1.4.6 Overview of a wire-bonded MAPBGA (Molded Array Process Ball Grid Array)

The wire-bonded **PBGA** (Plastic Ball Grid Array) package is a good option for mid- to high-performance devices that require low inductance, ease of surface mounting, relatively low cost, and excellent package reliability. Additional copper layers in the substrate allow for increased power dissipation capability with the Thermally Enhanced PBGA (TEPBGA). The features are practically similar to MAPBGA. In the **TEBGA** a thermally enhanced substrate

acts to spread and draw heat from the chip (die) to the customer board. For further power dissipating capability, a heat spreader is placed on top of the die, within the mold compound of a PBGA, drawing heat to the surface of the package. Its features are: PBGA process; overall substrate thickness increased over two-layer; additional epoxy dispense, heat spreader placement, epoxy cure steps needed; substrate design must account for heat spreader design to allow for attachment area; high reliability in industrial environments RoHS capability (till 260°C reflow); Pb-free solder balls available.

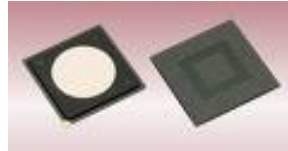


Fig. 1.4.7 Overview of a wire-bonded TEPBGA (Thermally Enhanced PBGA)

The **TBGA** (Tape Ball Grid Array) is a mid- to high-end BGA packaging solution for applications needing excellent thermal performance without an external heatsink. Its features are almost the same as in the case of PBGA but it offers an improved thermal performance over std PBGA packages $<15^{\circ}\text{C}/\text{W}$. The **FCPBGA** (Flip Chip Plastic Ball Grid Array) is a laminate-based BGA packaging solution. The FCPBGA provides competitive solutions for higher performance applications with improved board level solder joint reliability and lower cost compared to FC CBGA (the ceramic BGA). The substrates use standard organic PCB manufacturing and HDI laminate technologies, the FCPBGA footprint being a drop-in replacement (PCB design and board assembly) for WB PBGA for the same ball diameter and pitch.

Ceramic Ball-Grid-Array (CBGA)

Originally designed by IBM, the CBGA was developed to complement their flip chip technology. The package is comprised of a ceramic (alumina) substrate and a FC and an aluminum lid. Aluminum covers that have typically been used with the C4 technology have been bonded with a silicone adhesive (Sylgard 577) to provide a non-hermetic seal. With the flip-chip technology this is usually adequate for most applications. A hermetic seal can be accomplished by designing a seal ring into the ceramic and using a Ni/Fe cover plate for soldering. The package has a cavity which would allow for typical chip-and-wire technology to be utilized.

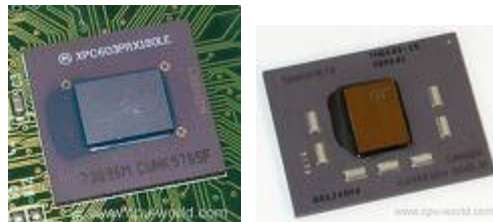


Fig. 1.4.8 Overview of ceramic BGAs (source: cpu-world.com)

Micro-Ball-Grid-Array (μBGA)

μBGA is a true "Chip Scale Package" (CSP) solution (see figure 1.3.7), only slightly larger than the chip itself (chip + 0.5mm). It is the ideal package for all memory devices such as Flash, DRAM and SRAM. μBGA packages enable broad real-estate reductions of typically 50-80 percent over existing packages. End use applications include cell phones, sub-notebooks, PDAs, camcorders, disk drives, and other space-sensitive applications. This package is also an excellent solution for applications that require a smaller, thinner, lighter or electrically enhanced package. The μBGA package is constructed utilizing a thin, flexible

circuit tape for its substrate and low stress elastomer for die attachment. The die is mounted face down and its electrical pads are connected to the substrate in a method similar to TAB bonding. After bonding these leads to the die, the leads are encapsulated with an epoxy material for protection. Solder balls are attached to pads on the bottom of the substrate, in a rectangular matrix similar to other BGA packages. The backside of the die is exposed allowing heat sinking if required for thermal applications. Ball pitches used usually are 0.50, 0.75, 0.80, and 1.0 mm. Other features and benefits include: 0.9 mm mounted height and excellent electrical and moisture performance.

The advantages of BGA type packages are as follows:

- precise alignment and mounting possible. Before the Ball grid Array packaging, a single circuit board would sometimes require hundreds of pins. This presented a lot of positioning problems. When the assembly was heated, adjacent pins would sometimes get soldered together or form unplanned bridges.
- good heat conduction; BGA has less thermal resistance so heat flows readily from the mounted circuit components to the printed circuit board. This reduces the risk of overheating.
- contact points (point of contact between the surface solder balls and the printed circuit board itself) are not readily apparent. This means greater data and application security.

The disadvantage is that the BGA package is rather inflexible and mechanical stress at the integrated circuit level may cause the balls or the contact points/joints to break off.

- **MCM/HDI and COF/HDI**

Multichip packaging of microsystems can be a viable means of integrating microsystems with other microelectronic technologies such as CMOS. One of the primary advantages of using multichip packaging as a vehicle for microsystems and microelectronics is the ability to efficiently host die from different or incompatible fabrication processes into a common substrate. High performance multichip module (MCM) technology has progressed rapidly in the past decade, which makes it attractive for use with microsystems.

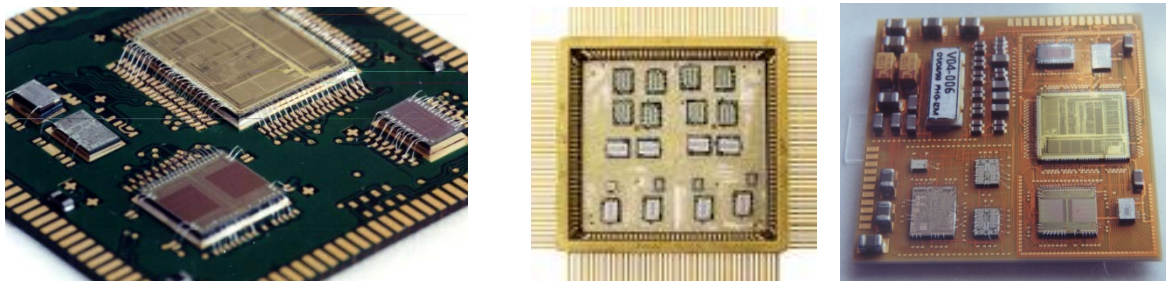


Fig. 1.4.9 Examples of MCMs (from left to right: laminated, ceramic, deposited)

The Chip-on-Flex (COF) process has been adapted for the packaging of microsystems. One of the primary areas of the work was reducing the potential for heat damage to the microsystem devices during laser ablation. Additional processing has also been added to minimize the impact of incidental residue on the die.

COF is an extension of the HDI technology developed in the late 1980's. The standard HDI "chips first" process consists of embedding bare die in cavities milled into a ceramic substrate

and then fabricating a layered thin-film interconnect structure on top of the components. Each layer in the HDI interconnect overlay is constructed by bonding a dielectric film on the substrate and forming via holes through laser ablation. The metallization is created through sputtering and photolithography.

COF processing retains the interconnect overlay used in HDI, but molded plastic is used in place of the ceramic substrate. Unlike HDI, the interconnect overlay is prefabricated before chip attachment. After the chip(s) have been bonded to the overlay, a substrate is formed around the components using a plastic mold forming process such as transfer, compression, or injection molding. Vias are then laser drilled to the component bond pads and the metallization is sputtered and patterned to form the low impedance interconnects.

For microsystems packaging, the COF process is augmented by adding a processing step for laser ablating large windows in the interconnect overlay to allow physical access to the microsystem devices. Additional plasma etching is also included after the via and large area laser ablations to minimize adhesive and polyimide residue which accumulates in the exposed windows.